Titanium Packaging User Guide

UG-TI-PKG-v5.4
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www.efinixinc.com

Contents

Introduction

Efinix offers Titanium FPGAs in packages that are designed for the devices' maximum number of user's I/O pins. This document describes the Titanium FPGAs' pin and package specifications as well as solder reflow guidelines.

Learn more: Refer to the following documents for more information:
FPGA pinout specification
FPGA data sheet for pin definitions

Available Package Options

Table 1: Titanium Package Options

Package	Pitch (mm)	Size (mm)	Ti35	Ti60	Ti90	Ti120	Ti135	Ti180	Ti200	Ti375
64-ball WLCSP	0.4	3.5x3.4		✓						
100-ball FBGA	0.5	5.5x5.5	✓	✓						
225-ball FBGA	0.65	10x10	✓	✓						
361-ball FBGA	0.65	13x13			✓	✓		✓		
400-ball FBGA	0.8	16x16			✓	✓		✓		
484-ball FBGA	0.8	18x18			✓	✓		✓		
529-ball FBGA	0.8	19x19			✓	✓	✓	✓	✓	✓

Refer to the FPGA data sheet for information on the number of GPIO and other resources in each FPGA/package combination.

Device Pinout File

Efinix provides pinout files for Titanium FPGAs. For each device/package combination, these files contain the pin name, I/O bank number for each pin, configuration function, and pin location.

Download: Download the pinout files from the Documentation page in the Support section of the Efinix® web site (www.efinixinc.com/support)

Pinout Description

The following tables describe the pinouts for power, ground, configuration, and interfaces.

Table 2: Power and Ground Pinouts

xx indicates the bank location.

Function	Description
VCC	Core power supply.
VCCA_*xx*	PLL analog power supply.
VDD_SOC	Hardened RISC-V block power supply.
VCCAUX	1.8 V auxiliary power supply.
VCCIO33_*xx*	HVIO bank power supply.
VCCIO33_*xx_yy_zz*	Power for HVIO banks that are shorted together. *xx*, *yy*, and *zz* are the bank locations. For example: VCCIO33_BR1_BR2 shorts banks BR1 and BR2.
VCCIO*xx*	HSIO bank power supply.
VCCIO*xx_yy_zz*	Power for HSIO banks that are shorted together. *xx*, *yy*, and *zz* are the bank locations. For example: VCCIO1B_1C shorts banks 1B and 1C
VQPS	1.8 V supply for security fuse. During configuration and normal operation, keep this pin at 0 V. When you want to blow the security fuses, power this pin up to 1.8 V.
GND	Ground.

Table 3: GPIO Pinouts

x indicates the location (T, B, L, or R); *xx* indicates the bank location; *n* indicates the number; *yyyy* indicates the function.

Function	Direction	Description
GPIO*x_n*	I/O	HVIO for user function. User I/O pins are single-ended.
GPIO*x_n_yyyy*	I/O	HVIO or multi-function pin.
GPIO*x*_N_*n* GPIO*x*_P_*n*	I/O	HSIO transmitter, receiver, or both.
GPIO*x*_N_*n_yyyy* GPIO*x*_P_*n_yyyy*	I/O	HSIO transmitter, receiver, both, or multi-function.

Function	Direction	Description
REF_RES_*xx*	–	REF_RES is a reference resistor to generate constant current for the related circuits. For Ti35/Ti60: Connect the following REF_RES pins to ground through a 10 kΩ resistor with a tolerance of ±1% : • REF_RES_ 2A and REF_RES_4A pins must be connected. • REF_RES pin of the particular bank, if pins in the bank are used as LVDS TX or MIPI TX lane. • REF_RES_3A pin, if internal oscillator is used. • REF_RES_3A pin, if blowing of fuses for FPGA security is required. You can leave the REF_RES pins floating if none of the above are applicable. For Ti90/Ti120/Ti180: Connect the following REF_RES pins to ground through a 10 kΩ resistor with a tolerance of ±1% : • REF_RES_ 2A, REF_RES_2C, REF_RES_4A, and REF_RES_4C pins must be connected. • REF_RES pin of the particular bank, if pins in the bank are used as LVDS TX or MIPI TX lane. • REF_RES_3A pin, if the internal oscillator is used. • REF_RES_3A pin, if blowing of fuses for FPGA security is required. You can leave the REF_RES pins floating if none of the above are applicable. For Ti135/Ti200/Ti375: Connect all REF_RES pins to ground through a 10 kΩ resistor with a tolerance of ±1%.

Table 4: Alternate Function Pinouts

n is the number.

Function	Direction	Description
CLK*n*	Input	Single ended input for global clock and control network resource. The number of inputs is package dependent.
CLK*n*_P/N	Input	Differential input pair for global clock and control network resource. P pins can access to global clock and control network resource if it is in single-ended configuration.
EXTFB	Input	PLL external feedback CLKIN.
PLLIN*n*	Input	PLL reference clock resource. The number of reference clock resources is package dependent.

Configuration Pins

Some configuration pins are dedicated, and some are dual-purpose.

- Dedicated pins cannot be used as general purpose I/O.
- During configuration, use dual-purpose pins as described in this document for the configuration mode you are using. After configuration (in user mode), you can use these pins as general-purpose I/O.

Table 5: Dedicated Configuration Pins

These pins cannot be used as general-purpose I/O after configuration.

All the pins are in internal weak pull-up during configuration mode except for `TCK` and `TDO`.

Calculate the resistor value as described in **Resistors in Configuration Circuitry** in **AN 033: Configuring Titanium FPGAs**.

Pins	Direction	Description	External Weak Pull Up/ Pull Down Requirement
CDONE	I/O	Configuration done status pin. CDONE is an open drain output; connect it to an external pull-up resistor to VCCIO. When CDONE = 1, the configuration is complete and the FPGA enters user mode. You can hold CDONE low and release it to synchronize the FPGAs entering user mode.	Pull up
CRESET_N	Input	Active-low FPGA reset and re-configuration trigger. Pulse CRESET_N low for a duration of t_{creset_N} before releasing CRESET_N from low to high to initiate FPGA re-configuration. This pin does not perform a system reset.	Pull up
TCK	Input	JTAG test clock input (TCK). The rising edge loads signals applied at the TAP input pins (TMS and TDI). The falling edge clocks out signals through the TAP TDO pin.	Pull up
TMS	Input	JTAG test mode select input (TMS). The I/O sequence on this input controls the test logic operation . The signal value typically changes on the falling edge of TCK. TMS is typically a weak pull-up; when it is not driven by an external source, the test logic perceives a logic 1.	Pull up
TDI	Input	JTAG test data input (TDI). Data applied at this serial input is fed into the instruction register or into a test data register depending on the sequence previously applied at TMS. Typically, the signal applied at TDI changes state following the falling edge of TCK while the registers shift in the value received on the rising edge. Like TMS, TDI is typically a weak pull-up; when it is not driven from an external source, the test logic perceives a logic 1.	Pull up
TDO	Output	JTAG test data output (TDO). This serial output from the test logic is fed from the instruction register or a test data register depending on the sequence previously applied at TMS. The shift out content is based on the issued instruction. The signal driven through TDO changes state following the falling edge of TCK. When data is not being shifted through the device, TDO is set to an inactive drive state (e.g., high-impedance).	Pull up

(1) CDONE has a drive strength of 12 mA at 1.8 V.

Pins	Direction	Description	External Weak Pull Up/ Pull Down Requirement
JTAG_VCCIO_SEL	Input	JTAG voltage select pin. This pin affects the BR4 bank voltage, or any banks merged with the BR4 bank. Supply VCCIO33_BR4 with 1.8 V and connect an external resistor between this pin and ground to use JTAG at 1.8 V. Leave this pin floating to use the default JTAG at 3.3 V or 2.5 V. Available on Ti135, Ti200, and Ti375 FPGAs only.	Floating or pull down

Table 6: Dual-Purpose Configuration Pins

In user mode (after configuration), you can use these dual-purpose pins as general I/O.

Calculate the resistor value as described in **Resistors in Configuration Circuitry** in **AN 033: Configuring Titanium FPGAs**.

Pins	Direction	Description	External Weak Pull Up/ Pull Down Requirement
CBSEL[1:0]	Input	Multi-image configuration selection pin. This function is not applicable to single-image bitstream configuration or internal reconfiguration (remote update). Connect CBSEL[1:0] to the external resistors for the image you want to use: 00 for image 1 01 for image 2 10 for image 3 11 for image 4 0: Connect to an external weak pull down. 1: Connect to an external weak pull up.	Pull up or pull down
CCK	I/O	Passive SPI input configuration clock or active SPI output configuration clock.	Optional pull up if required by external load
CDI*n*	I/O	Data input for SPI configuration. *n* is a number from 0 to 31 depending on the SPI configuration data width. CDI0 is an output in x1 active configuration mode and is a bidirectional pin in all other active configuration modes. CDI4 is a bidirectional pin in x8 active configuration mode. In a multi-bit daisy chain connection, CDI*n*[31:0] connects to the data bus in parallel.	Optional pull up if required by external load
CSI	Input	Chip select. 0: The FPGA is not selected or enabled and will not be configured. 1: Select the FPGA for allSPI configuration modes. Ti35 and Ti60 FPGAs require this setting for JTAG configuration mode. This pin is not bonded out in some of the smaller packages, such as the F100.	Pull up
CSO	Output	Chip select output. Asserted after configuration is complete. Connect this pin to the chip select pin of the next FPGA for daisy chain configuration.[2] This pin is not bonded out in some of the smaller packages, such as the F100.	–
NSTATUS	Output	Indicates a configuration error. When the FPGA drives this pin low, it indicates an ID mismatch, the bitstream CRC check has failed, or remote update has failed.	–

[2] Cascaded configuration is not supported in the F100S3F2 package.

Pins	Direction	Description	External Weak Pull Up/ Pull Down Requirement
SSL_N	I/O	SPI configuration mode select. The FPGA senses the value of SSL_N when it comes out of reset (i.e., CRESET_N transitions from low to high). 0: Passive mode; connect to external weak pull down. 1: Active mode; connect to external weak pull up. In active configuration mode, SSL_N is an active-low chip select to the flash device (CDI0 - CDI3).	Pull up or pull down
SSU_N	Output	Active-low chip select to the upper flash device (CDI4 - CDI17) in active x8 configuration mode (dual quad mode). Not available on W64 and F100 packages.	Optional pull up if required by external load
EXT_CONFIG_CLK	Input	Alternative clock in active configuration mode.	Optional pull up if required by external load
TEST_N	Input	Active-low test mode enable signal. Set to 1 to disable test mode. During all configuration modes, rely on the external weak pull-up or drive this pin high.	Pull up

Dedicated DDR Pinout

Table 7: Dedicated DDR Pinout

n indicates the number.

Function	Direction	Description
DDR_A[*n*]	Output	Address signals to the memories.
DDR_CKE	Output	Active-high clock enable signals to the memories.
DDR_CK DDR_CK_N	Output	Differential clock output pins to the memories.
DDR_CS_N	Output	Active-low chip select signals to the memories.
DDR_DQ[*n*]	I/O	Data bus to/from the memories.
DDR_DM[*n*]	Output	Active-high data-mask signals to the memories.
DDR_DQS[*n*] DDR_DQS_N[*n*]	I/O	Differential data strobes to/from the memories.
DDR_RST_N	Output	Active-low reset signals to the memories.
DDR_CAL	Input	240 Ω to ground reference resistor port.
VDD_PHY_DDR*n*	–	DDR digital power supply.
VDDQ_PHY_DDR*n*	–	DDR I/O power supply.
VDDQX_PHY_DDR*n*	–	DDR I/O pre-driver power supply.
VDDPLL_MCB_TOP_PHY_DDR*n*	–	DDR PLL power supply.
VDDQ_CK_PHY_DDR*n*	–	DDR I/O power supply for clock.

Table 8: Dedicated LPDDR4x DRAM Pinout

n indicates the number.

Function	Direction	Description
VDD1	Input	Core 1 power for LPDDR4X SDRAM.
VDD2	Input	Core 2 power/input buffer for LPDDR4X SDRAM.
VDDQ	Input	I/O buffer power for LPDDR4X SDRAM.
ZQ	Input	Calibration resistor pin. This pin calibrates the drive strength and termination resistance. Connect the ZQ pin to VDDQ through a 240 Ω ± 1% resistor

Dedicated MIPI D-PHY Pinout

Table 9: Dedicated MIPI D-PHY Pinout

m and *n* indicates the number. *L* indicates the lane

Function	Direction	Description
VCC18A_MIPI*m*_*n*_TX	–	Power supply for the MIPI D-PHY block. *m* and *n* are the MIPI channel numbers. For example: VCC18A_MIPI0_1_TX displays the power of MIPI D-PHY TX channel 0 and channel 1 being shorted together.
VCC18A_MIPI*m*_*n*_RX	–	Power supply for the MIPI D-PHY block. *m* and *n* are the MIPI interface numbers. For example: VCC18A_MIPI0_1_RX displays the power of MIPI D-PHY RX channel 0 and channel 1 being shorted together.
MIPI*n*_TXDP*L* MIPI*n*_TXDN*L*	I/O	MIPI differential transmit data lane.
MIPI*n*_RXDP*L* MIPI*n*_RXDN*L*	I/O	MIPI differential receive data lane.

Table 10: Dedicated MIPI D-PHY Pinouts

n indicates the number. *L* indicates the lane

Function	Direction	Description
VCC18A_MIPI*n*_TX	–	Power supply for the MIPI D-PHY block.
VCC18A_MIPI*n*_RX	–	Power supply for the MIPI D-PHY block.
MIPI*n*_TXDP*L* MIPI*n*_TXDN*L*	Output	MIPI differential transmit data lane.
MIPI*n*_RXDP*L* MIPI*n*_RXDN*L*	Input	MIPI differential receive data lane.

Dedicated Transceiver Pinout

Table 11: Dedicated Transceiver Pinout

n indicates the bank number; *L* indicates the lane; *nn* indicates the merged transceiver bank numbers.

Function	Direction	Description
VCC_SERDES*nn*	–	Transceiver digital PCS and PCIe controller power supplies.
VDDA_C_Q*nn*	–	Transceiver analog bias power supply.
VDDA_D_Q*nn*	–	Transceiver digital and analog data path power supplies.
VDDA_H_Q*nn*	–	Transceiver analog power supply for I/O.
PERST_Q*n*_N	Input	Active-low PCIe reset pin.
Q*n*_CAL_RES	Input	Transceiver calibration resistor. Connect an external resistor between this pin and ground. The resistor value is 3.01 kΩ with 1% tolerance.
Q*n*_REFCLK*n*_N Q*n*_REFCLK*n*_P	Input	Transceiver differential external reference clock input. REFCLK0: Main clock. REFCLK1: Alternative clock.
Q*n*_RXDP*L* Q*n*_RXDN*L*	Input	Transceiver differential receive serial data inputs. Q0 and Q2 include the PCIe controller.
Q*n*_TXDP*L* Q*n*_TXDN*L*	Output	Transceiver differential transmitter serial data inputs Q0 and Q2 include the PCIe controller.

64-Ball WLCSP Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

Figure 1: 64-Ball WLCSP Pinout Diagram

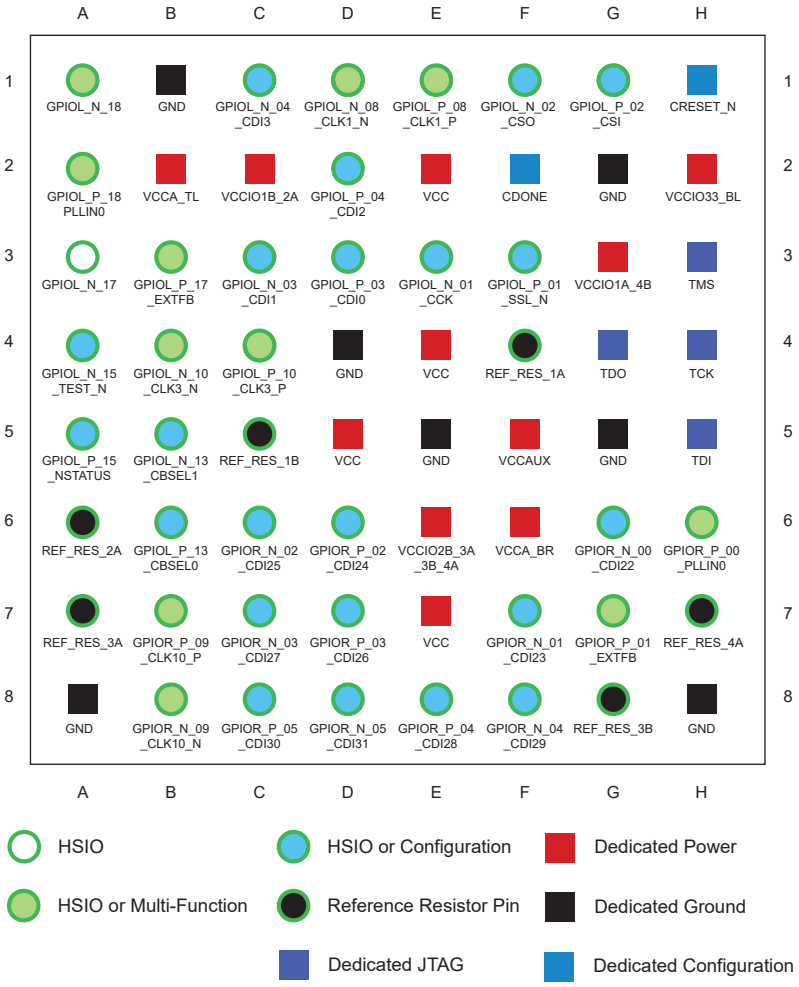


Figure 2: 64-Ball WLCSP I/O Bank Diagram

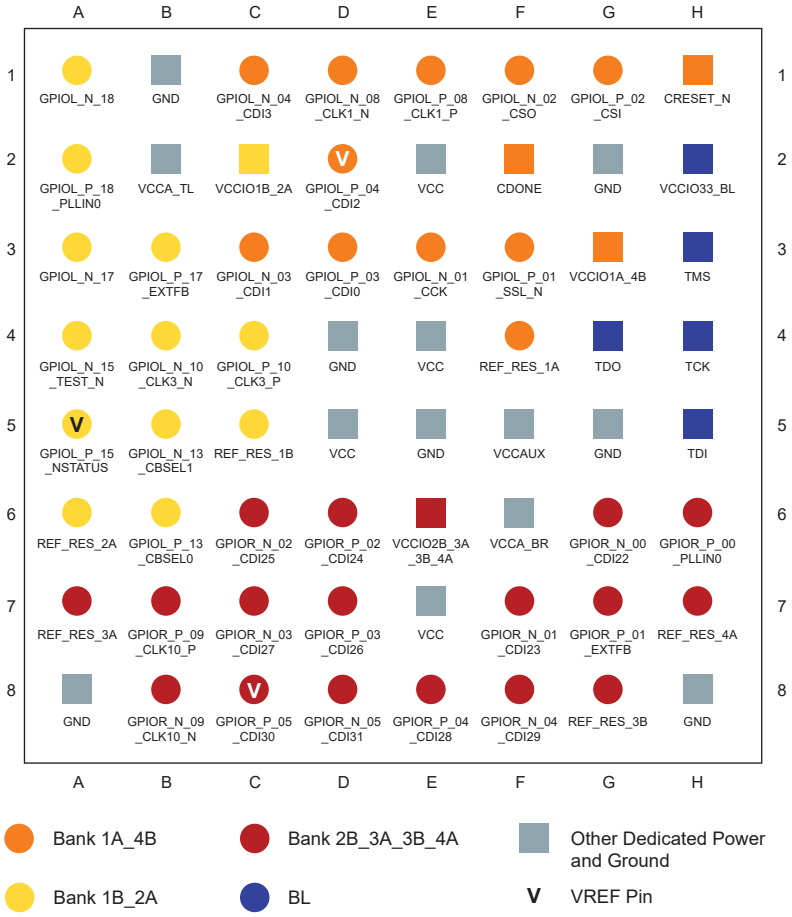


Figure 3: 64-Ball WLCSP Emulated MIPI RX Groups

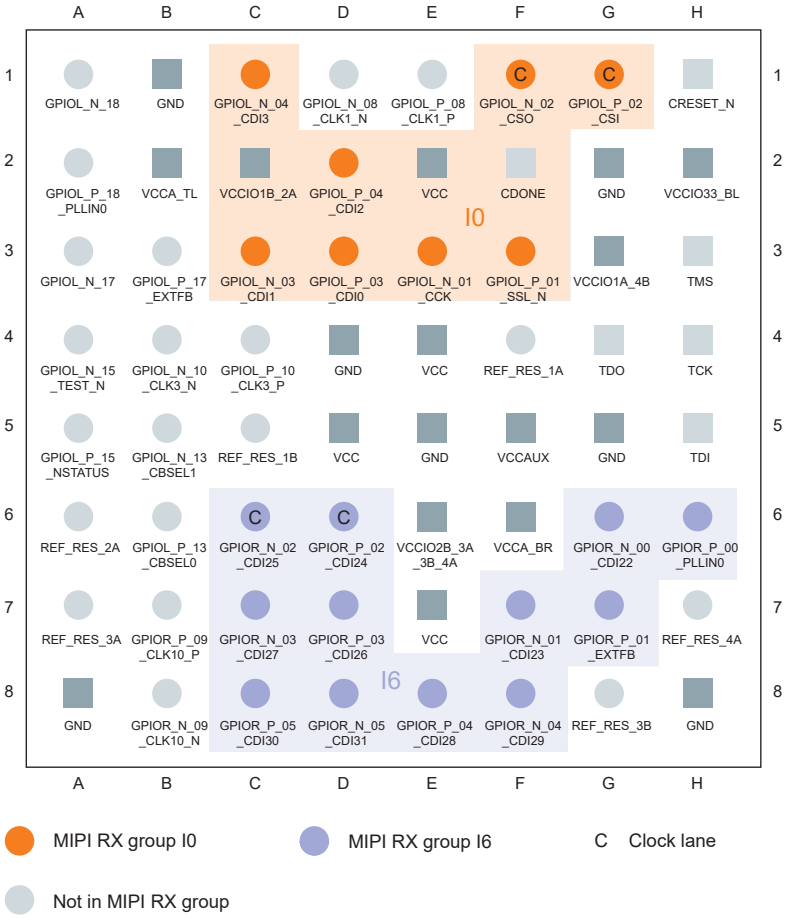


Figure 4: 64-Ball WLCSP Package Marking

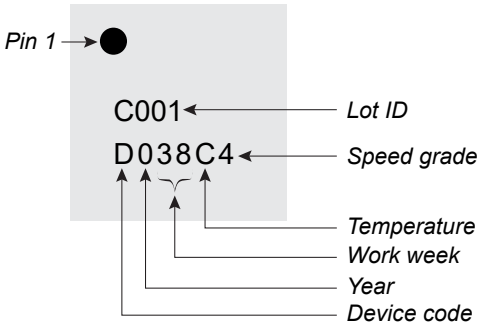
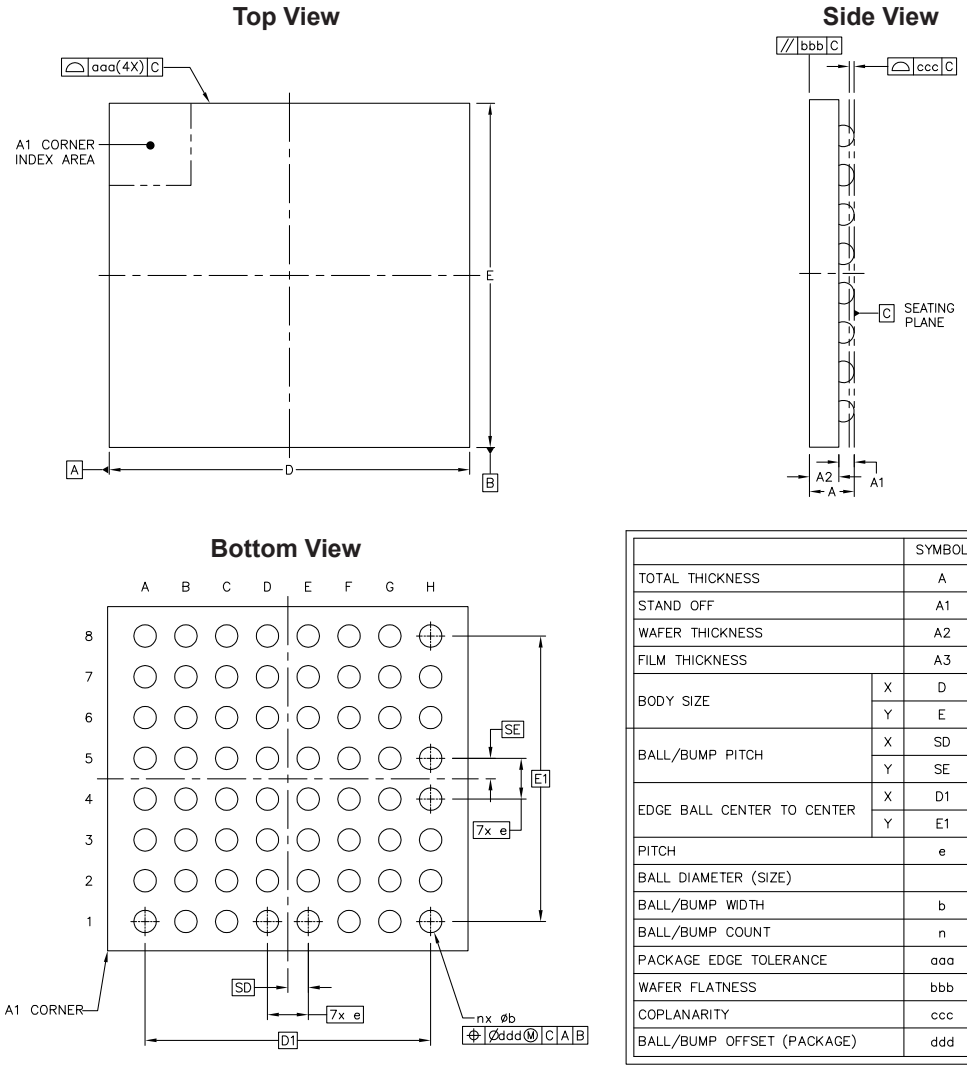


Figure 5: 64-Ball WLCSP Package Outline

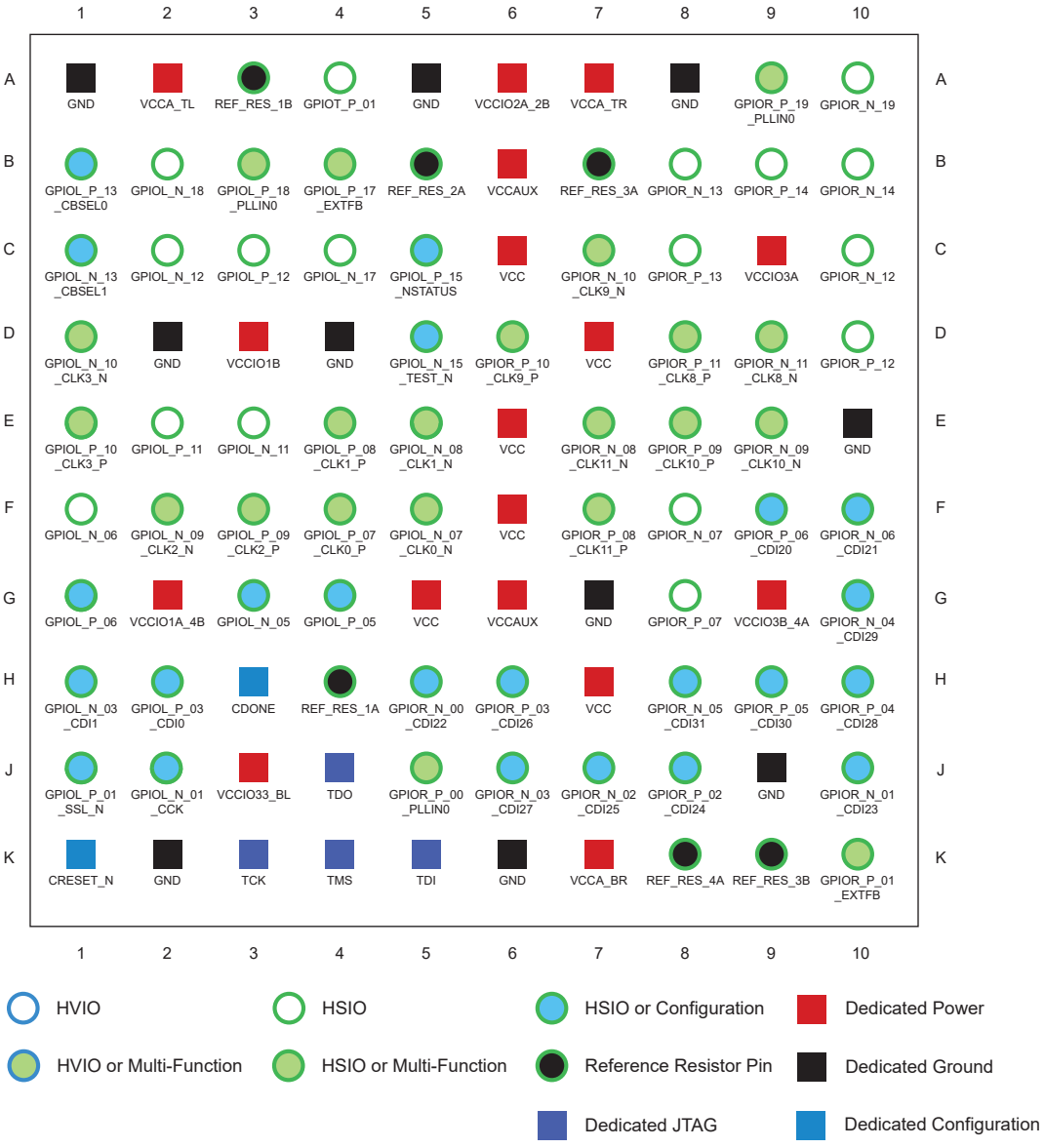


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.405	0.455	0.505
STAND OFF		A1	0.125	---	0.185
WAFER THICKNESS		A2	0.28	0.3	0.32
FILM THICKNESS		A3	---	---	---
BODY SIZE	X	D	3.5353		
	Y	E	3.3753		
BALL/BUMP PITCH	X	SD	0.2		BSC
	Y	SE	0.2		BSC
EDGE BALL CENTER TO CENTER	X	D1	2.8		BSC
	Y	E1	2.8		BSC
PITCH		e	0.4		BSC
BALL DIAMETER (SIZE)			0.2		
BALL/BUMP WIDTH		b	0.19	---	0.25
BALL/BUMP COUNT		n	64		
PACKAGE EDGE TOLERANCE		aaa	0.03		
WAFER FLATNESS		bbb	0.06		
COPLANARITY		ccc	0.05		
BALL/BUMP OFFSET (PACKAGE)		ddd	0.015		

100-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

Figure 6: 100-Ball FBGA Pinout Diagram



HVIO
HSIO
HSIO or Configuration
Dedicated Power
HVIO or Multi-Function
HSIO or Multi-Function
Reference Resistor Pin
Dedicated Ground
Dedicated JTAG
Dedicated Configuration

Figure 7: 100-Ball FBGA I/O Bank Diagram

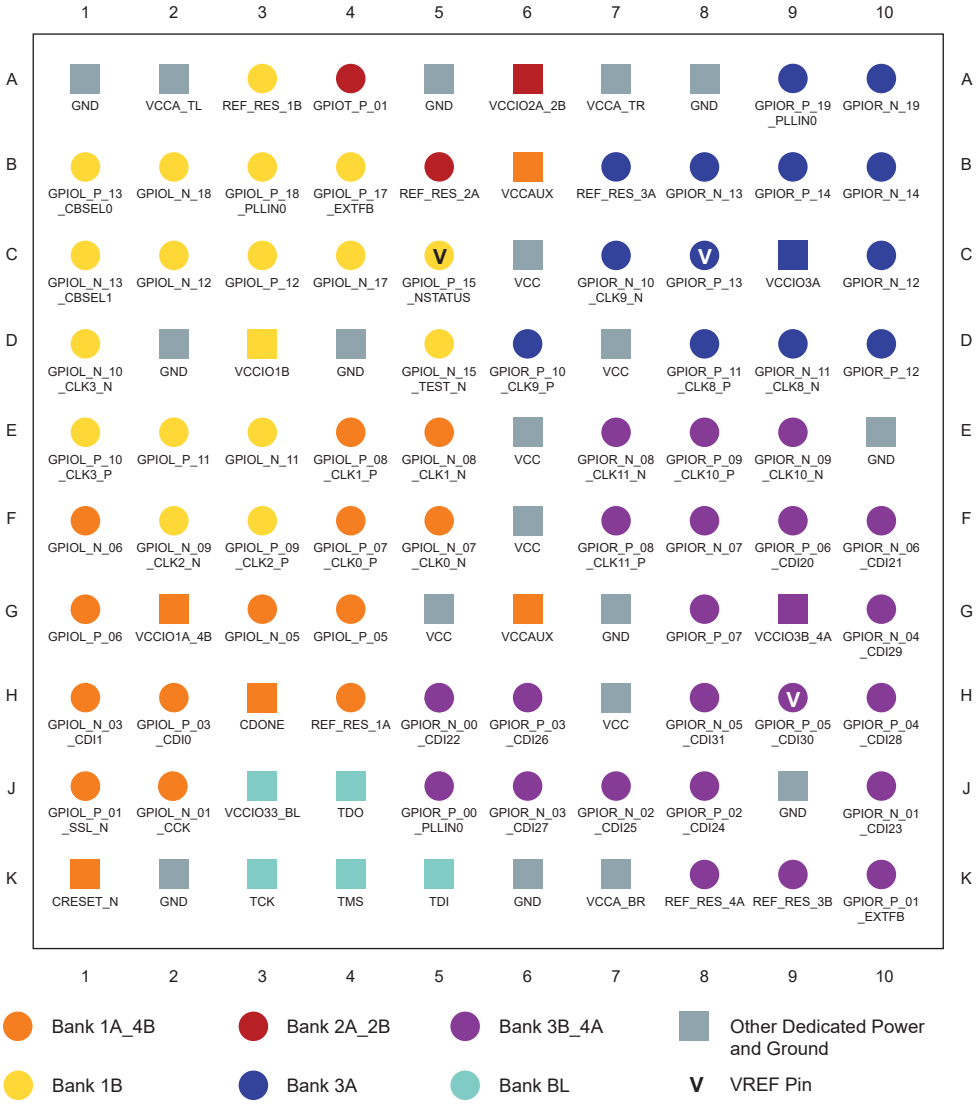


Figure 8: 100-Ball FBGA Emulated MIPI RX Groups

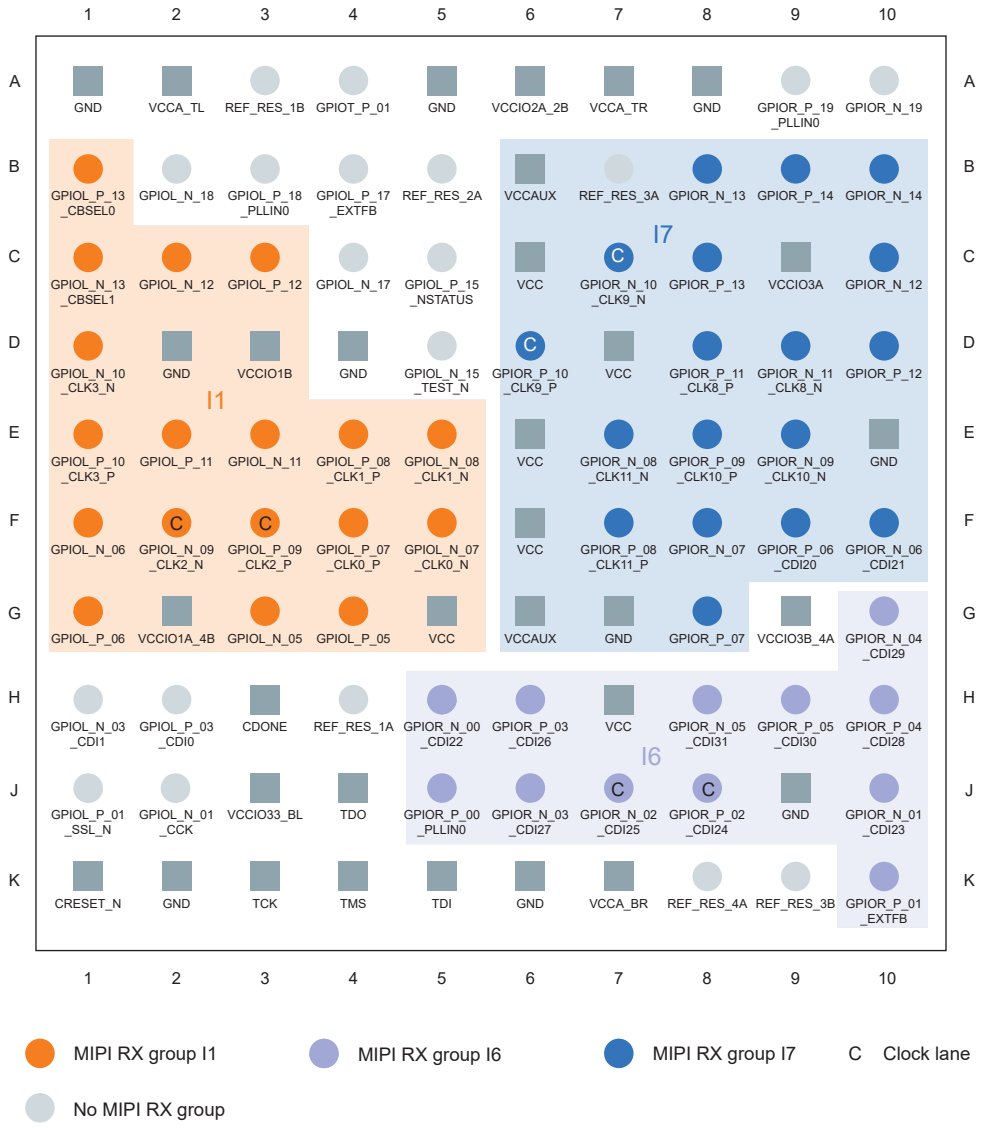


Figure 9: 100-Ball FPGA Package Marking

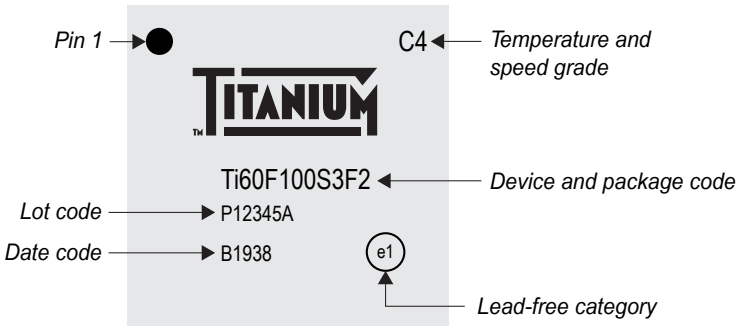
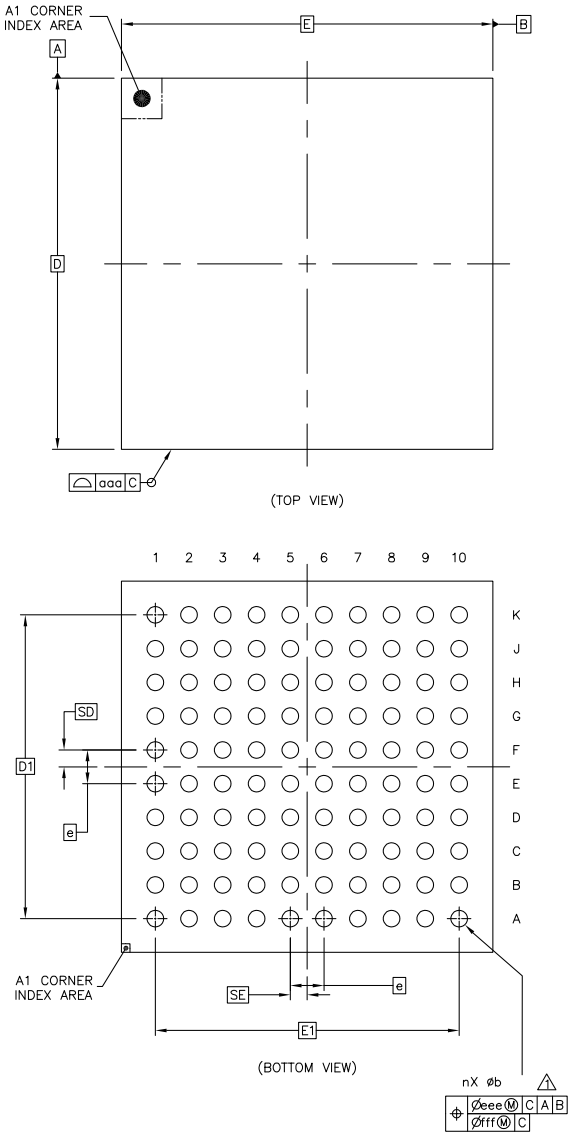


Figure 10: 100-Ball FBGA Package Outline



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1.1
STAND OFF	A1	0.11	---	0.21
SUBSTRATE THICKNESS	A2		0.105	REF
MOLD THICKNESS	A3		0.7	REF
BODY SIZE	D		5.5	BSC
	E		5.5	BSC
BALL DIAMETER			0.25	
BALL OPENING			0.25	
BALL WIDTH	b	0.2	---	0.3
BALL PITCH	e		0.5	BSC
BALL COUNT	n		100	
EDGE BALL CENTER TO CENTER	D1		4.5	BSC
	E1		4.5	BSC
BODY CENTER TO CONTACT BALL	SD		0.25	BSC
	SE		0.25	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

225-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

Note: Refer to the F225 Escape Routing on page 65 for an escape routing example.

Figure 11: 225-Ball FBGA Pinout Diagram

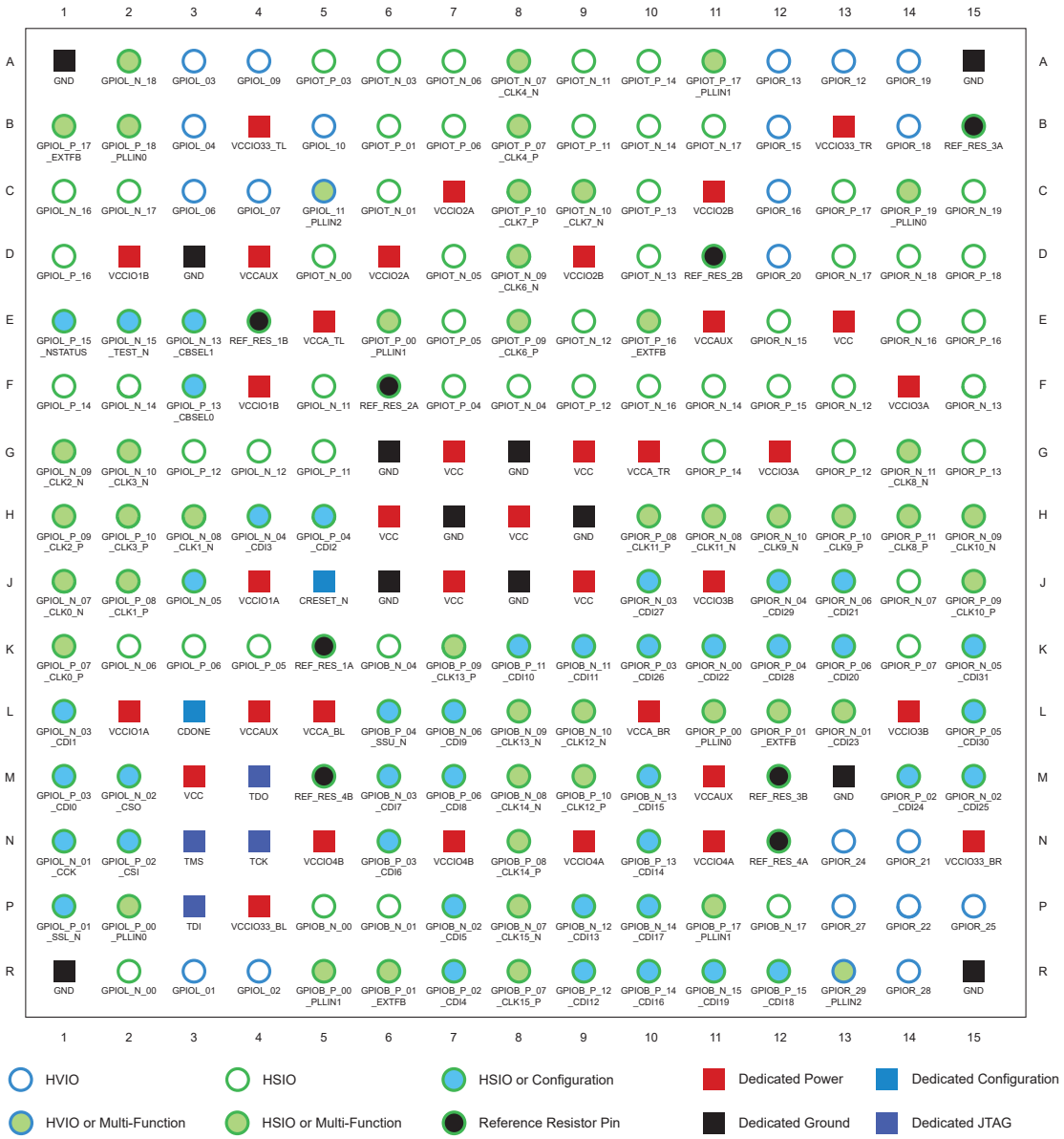


Figure 12: 225-Ball FBGA I/O Bank Diagram

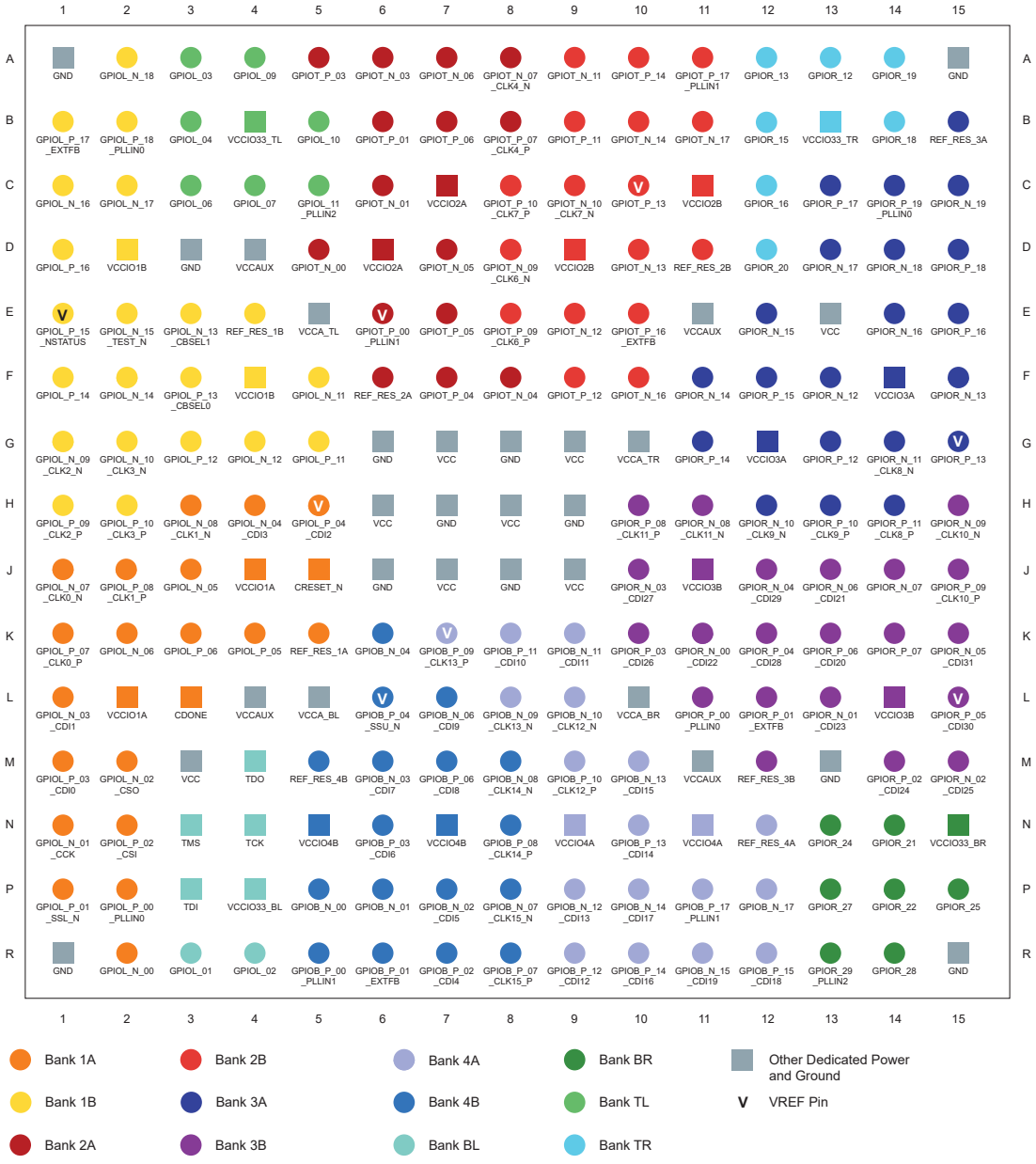


Figure 13: 225-Ball FBGA Emulated MIPI RX Groups

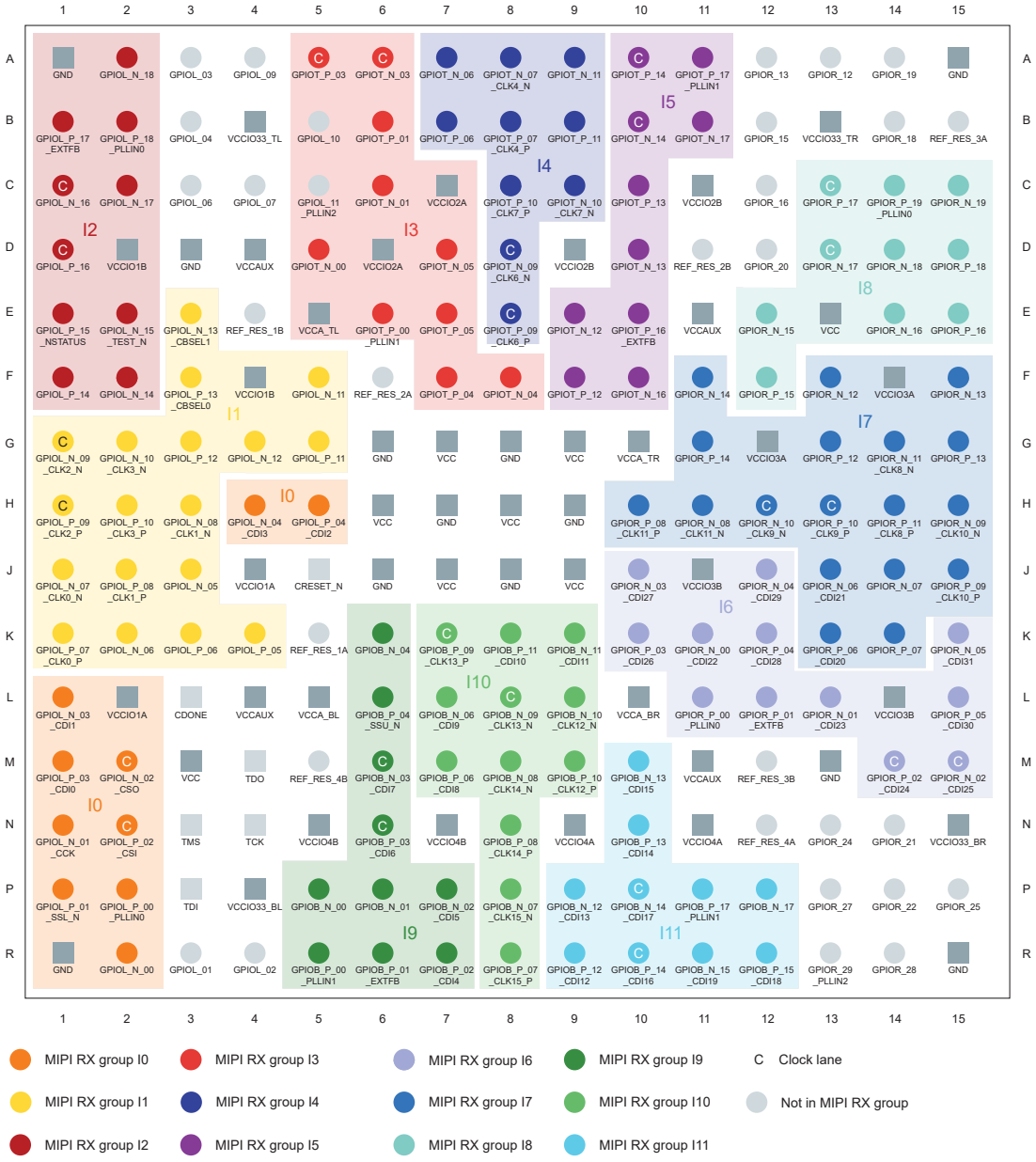


Figure 14: 225-Ball FPGA Package Marking

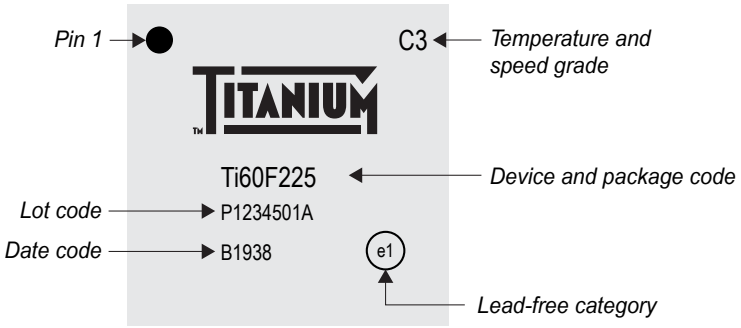
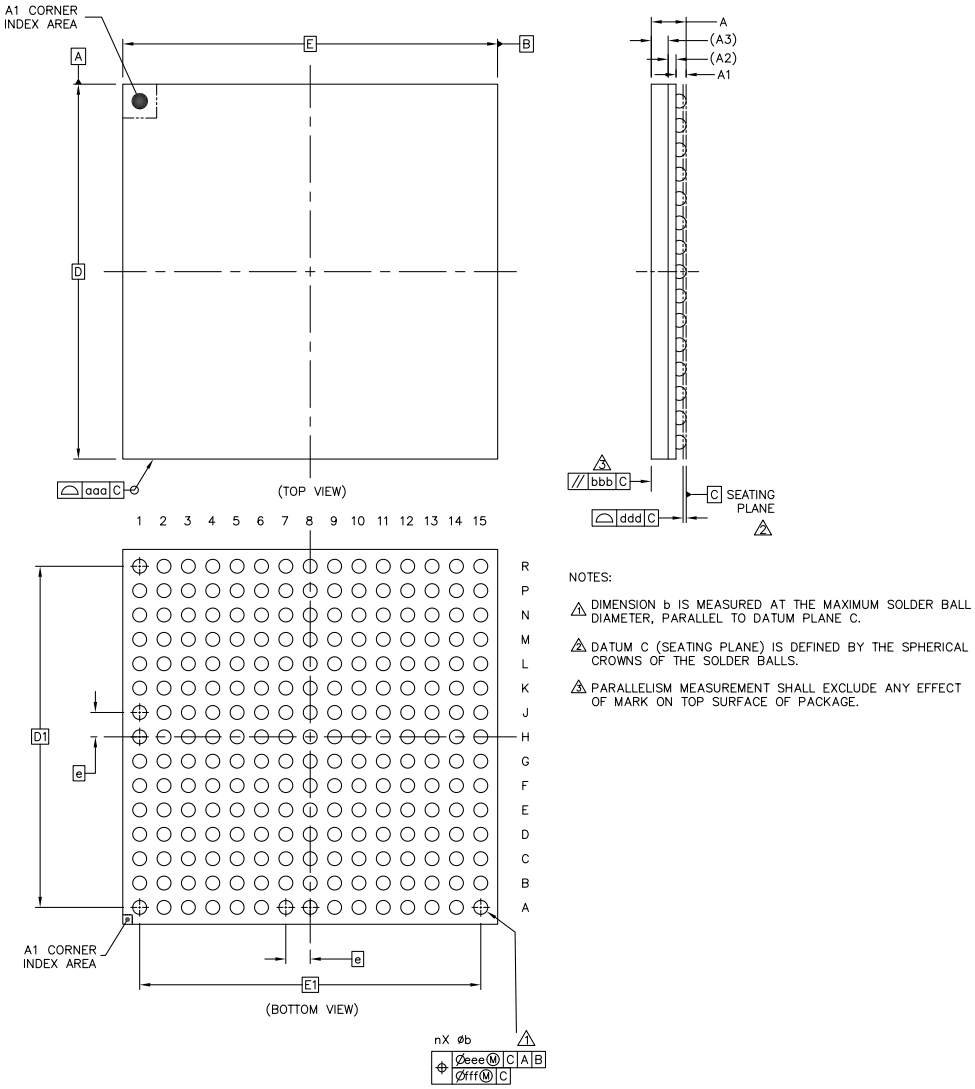


Figure 15: 225-Ball FBGA Package Outline



NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

For Lot Number: 'CXXXXXX' and 'SXXXXXX'

	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1.1
STAND OFF	A1	0.22	---	0.32
SUBSTRATE THICKNESS	A2		0.21	REF
MOLD THICKNESS	A3		0.54	REF
BODY SIZE	D		10	BSC
	E		10	BSC
BALL DIAMETER			0.35	
BALL OPENING			0.3	
BALL WIDTH	b	0.32	---	0.42
BALL PITCH	e		0.65	BSC
BALL COUNT	n		225	
EDGE BALL CENTER TO CENTER	D1		9.1	BSC
	E1		9.1	BSC
BODY CENTER TO CONTACT BALL	SD		---	BSC
	SE		---	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

For Other Lot Numbers

	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1
STAND OFF	A1	0.22	---	0.32
SUBSTRATE THICKNESS	A2		0.21	REF
MOLD THICKNESS	A3		0.45	REF
BODY SIZE	D		10	BSC
	E		10	BSC
BALL DIAMETER			0.35	
BALL OPENING			0.3	
BALL WIDTH	b	0.32	---	0.42
BALL PITCH	e		0.65	BSC
BALL COUNT	n		225	
EDGE BALL CENTER TO CENTER	D1		9.1	BSC
	E1		9.1	BSC
BODY CENTER TO CONTACT BALL	SD		---	BSC
	SE		---	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

361-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

361-Ball (J) FBGA Package Specifications

Figure 16: 361-Ball (J) FBGA Pinout Diagram

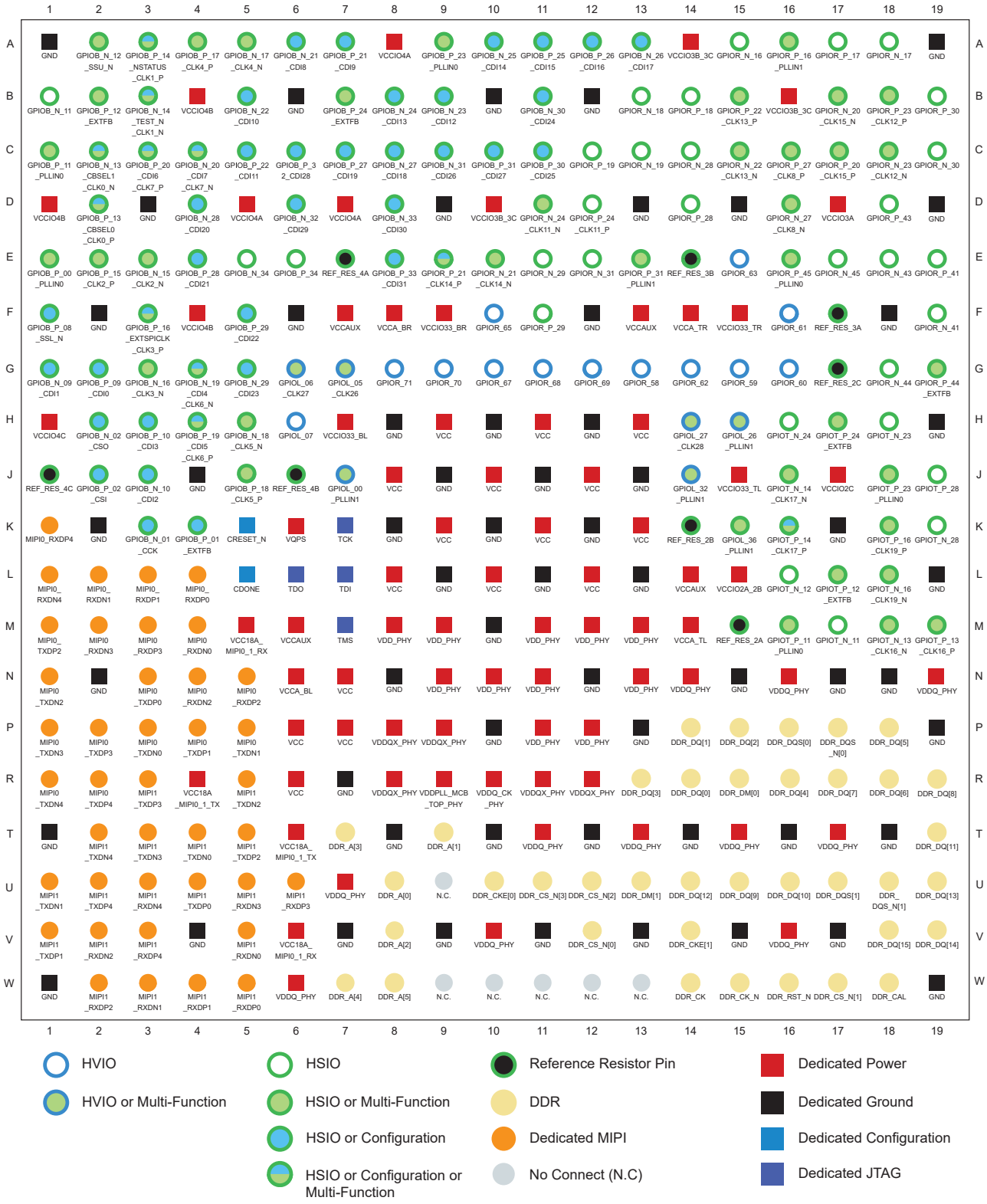


Figure 17: 361-Ball (J) FBGA I/O Bank Diagram

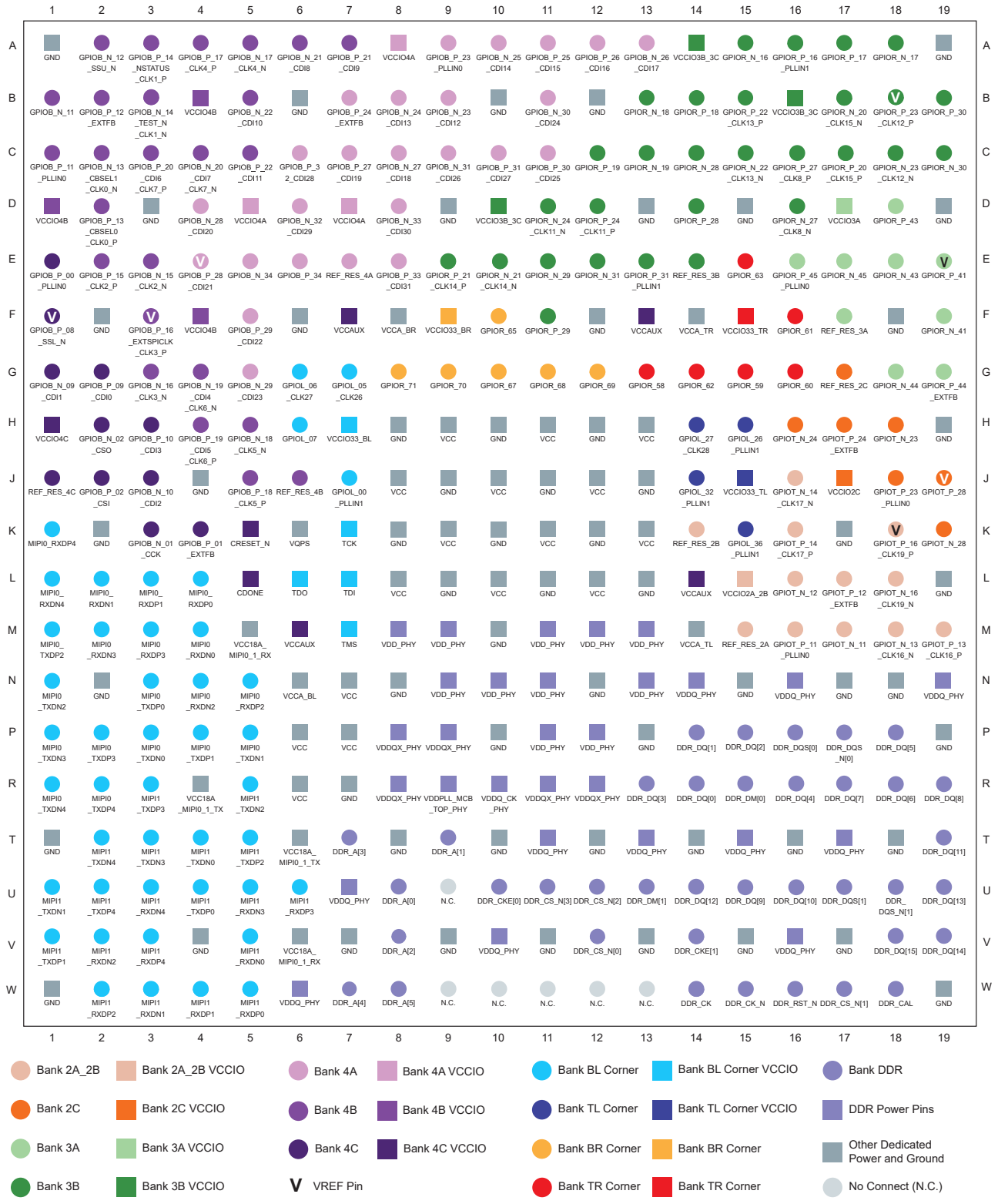


Figure 18: 361-Ball (J) FBGA Emulated MIPI RX Groups

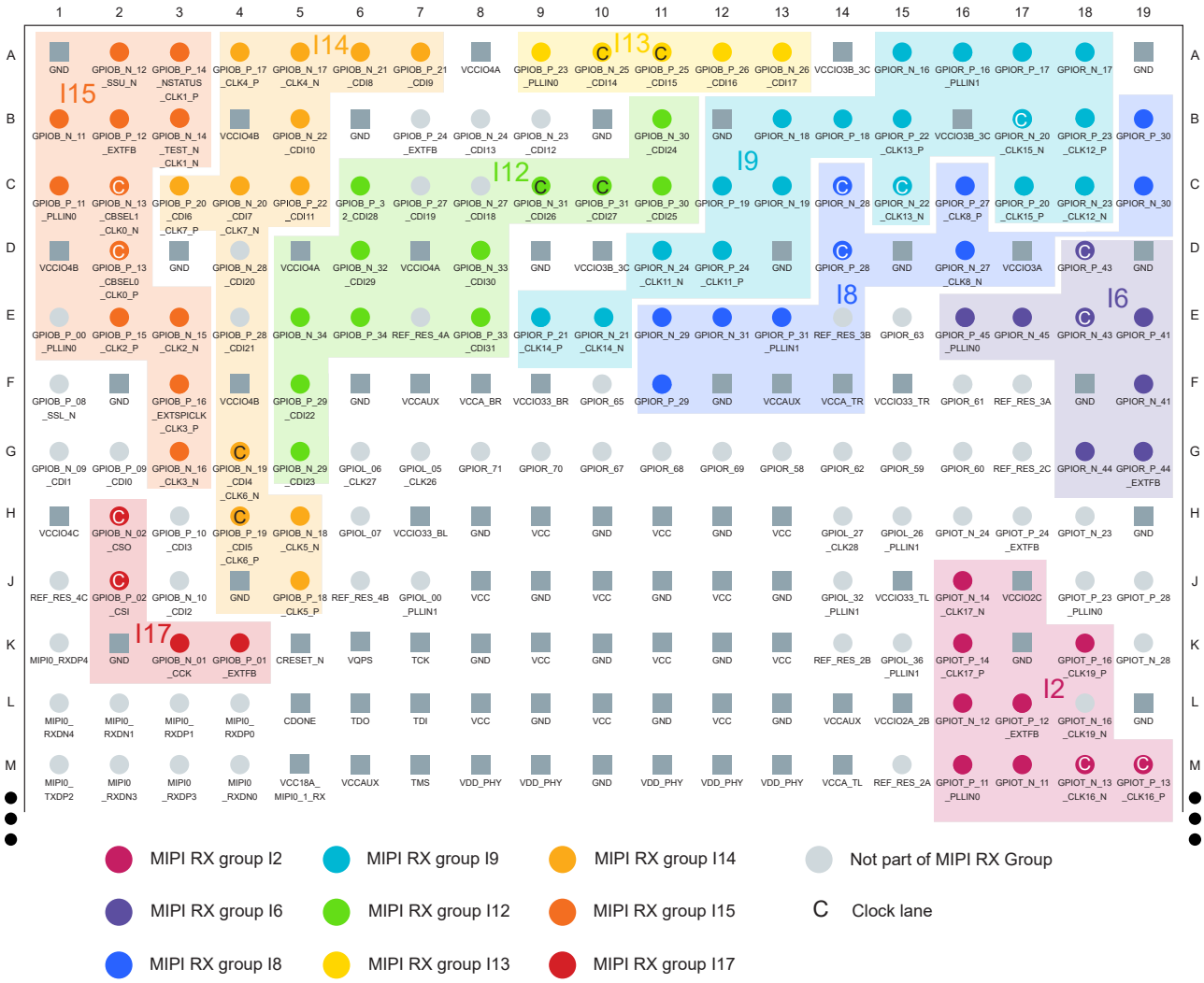


Figure 19: 361-Ball (J) FPGA Package Marking

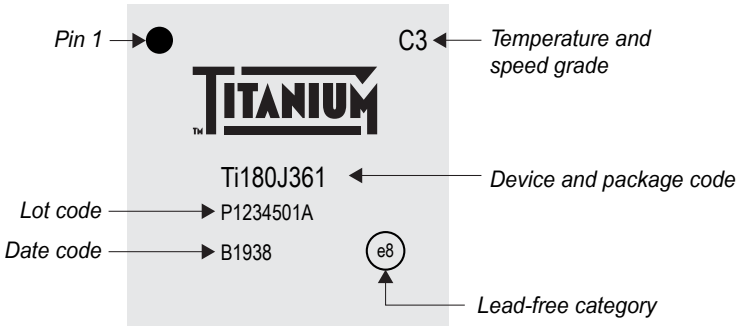
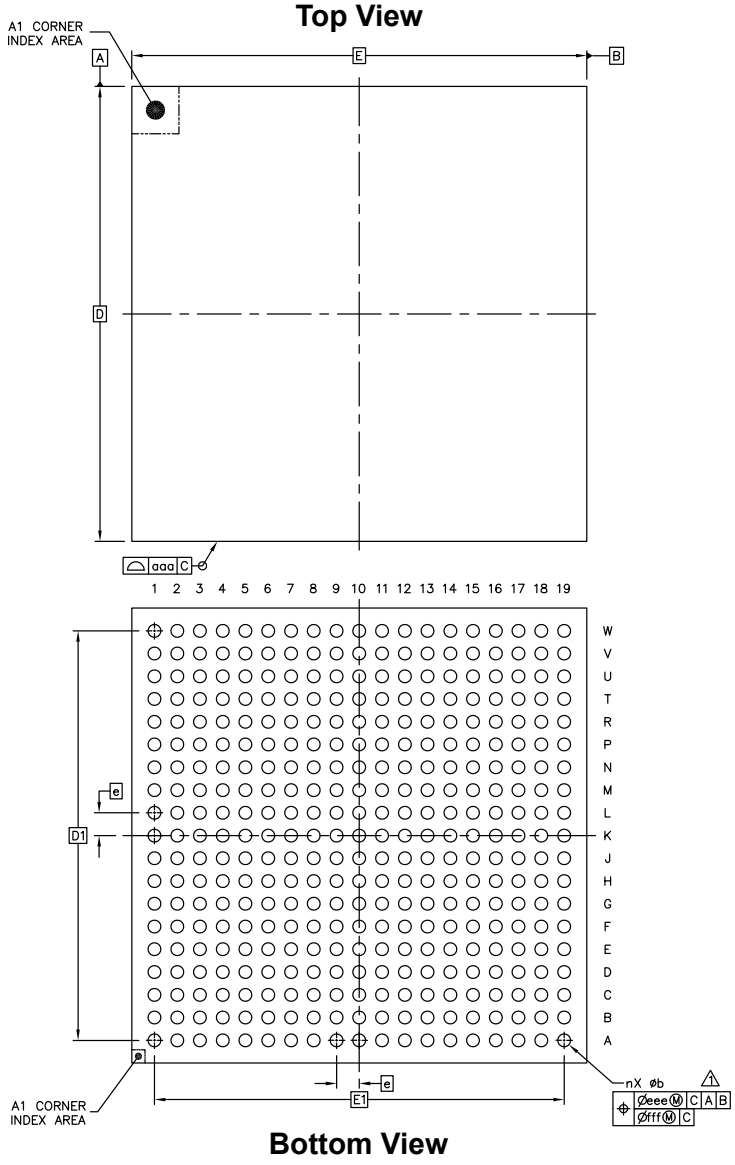
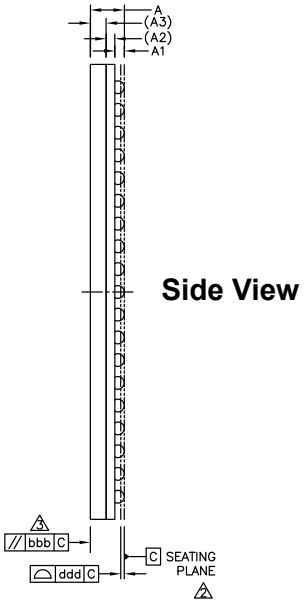


Figure 20: 361-Ball (J) FBGA Package Outline





	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	0.893	0.968	1.1
STAND OFF	A1	0.22	0.27	0.32
SUBSTRATE THICKNESS	A2		0.248	REF
MOLD THICKNESS	A3		0.45	REF
BODY SIZE	D		13	BSC
	E		13	BSC
BALL DIAMETER			0.35	
BALL OPENING			0.3	
BALL WIDTH	b	0.32	0.37	0.42
BALL PITCH	e		0.65	BSC
BALL COUNT	n		361	
EDGE BALL CENTER TO CENTER	D1		11.7	BSC
	E1		11.7	BSC
BODY CENTER TO CONTACT BALL	SD		---	BSC
	SE		---	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.1	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

400-Ball (G) FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

Figure 21: 400-Ball (G) FBGA Pinout Diagram

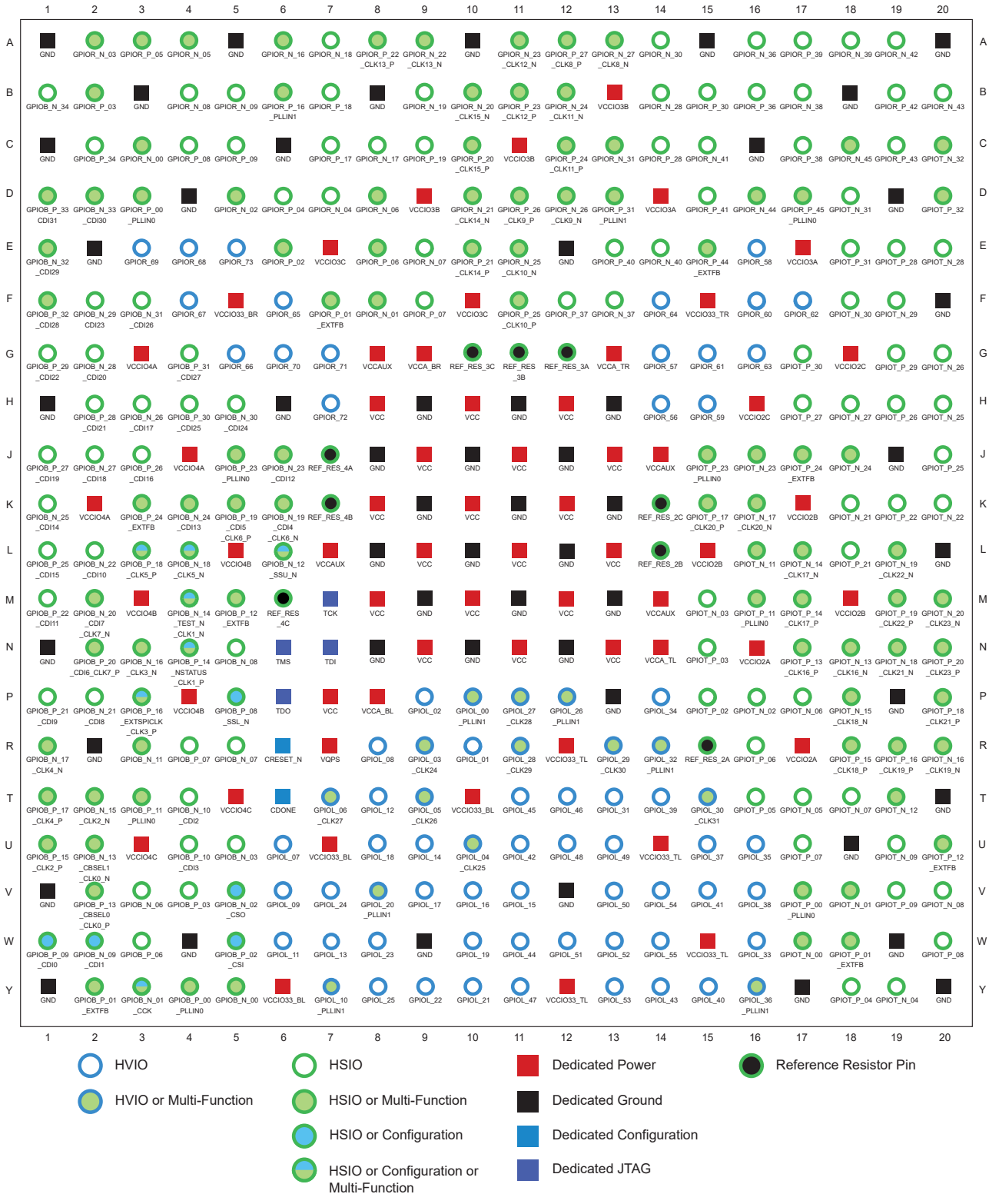


Figure 22: 400-Ball (G) FBGA I/O Bank Diagram

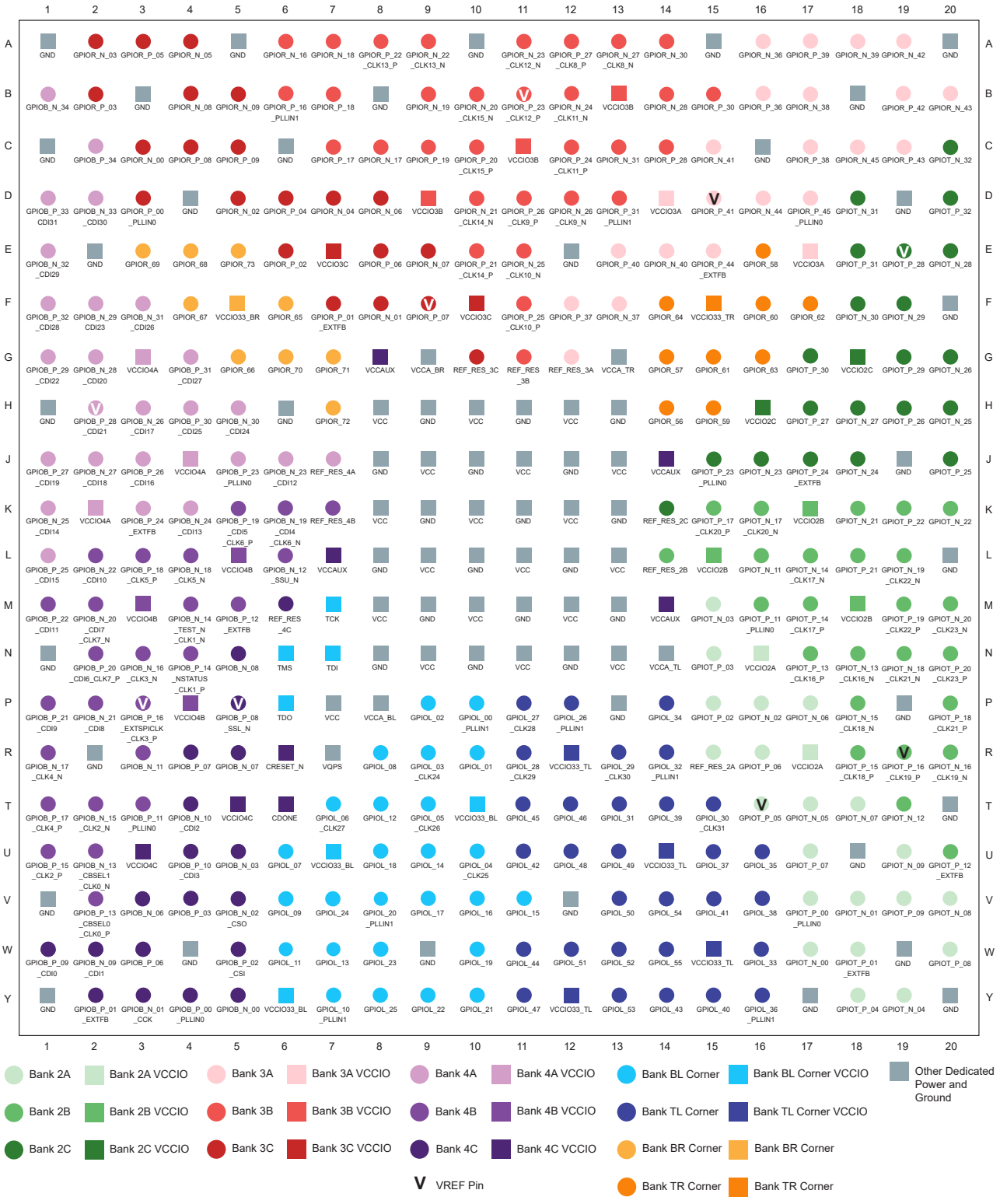


Figure 23: 400-Ball (G) FBGA Emulated MIPI RX Groups

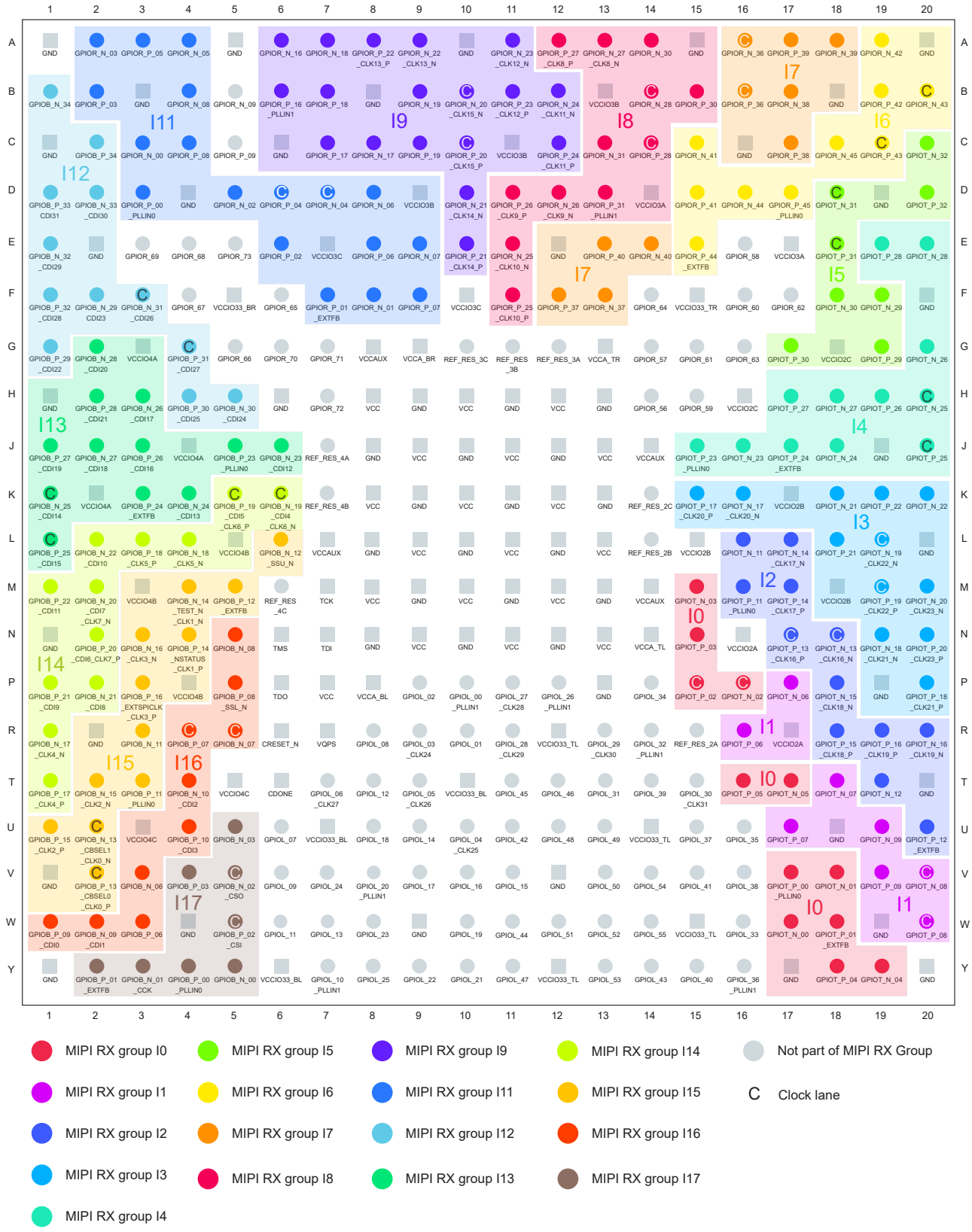


Figure 24: 400-Ball (G) FPGA Package Marking

Preliminary.

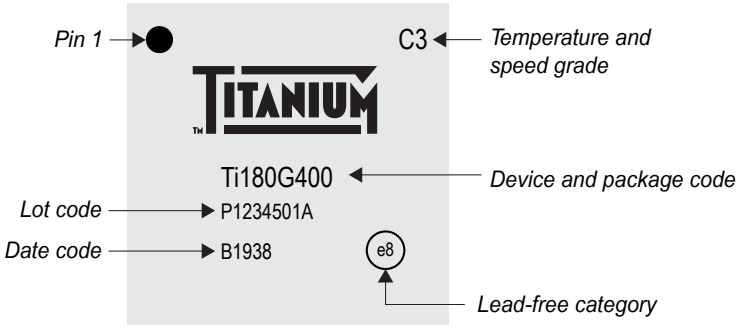
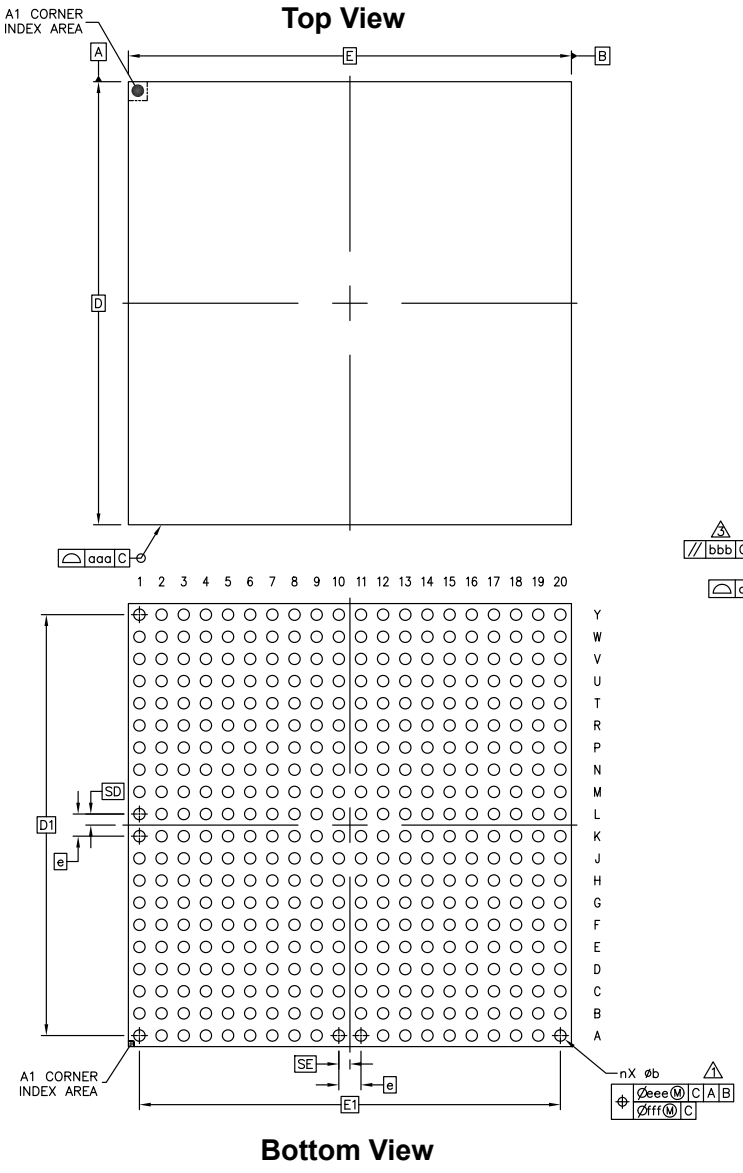


Figure 25: 400-Ball (G) FBGA Package Outline



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	1.103	1.178	1.3
STAND OFF	A1	0.27	---	0.37
SUBSTRATE THICKNESS	A2		0.328	REF
MOLD THICKNESS	A3		0.53	REF
BODY SIZE	D		16	BSC
	E		16	BSC
BALL DIAMETER			0.4	
BALL OPENING			0.35	
BALL WIDTH	b	0.36	---	0.46
BALL PITCH	e		0.8	BSC
BALL COUNT	n		400	
EDGE BALL CENTER TO CENTER	D1		15.2	BSC
	E1		15.2	BSC
BODY CENTER TO CONTACT BALL	SD		0.4	BSC
	SE		0.4	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.15	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

484-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

484-Ball (J) FBGA Package Specifications

Figure 26: 484-Ball (J) FBGA Pinout Diagram

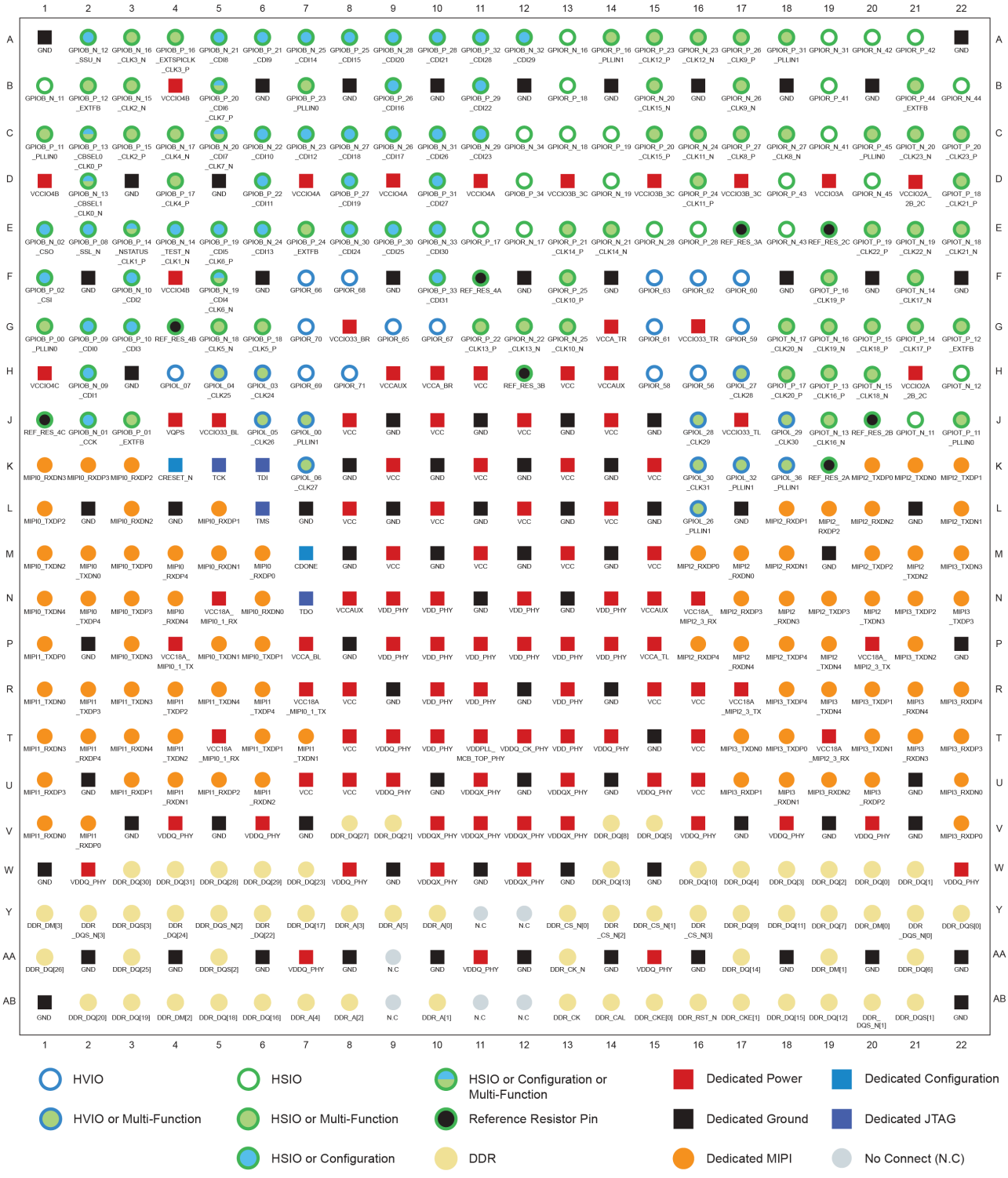


Figure 27: 484-Ball (J) FBGA I/O Bank Diagram

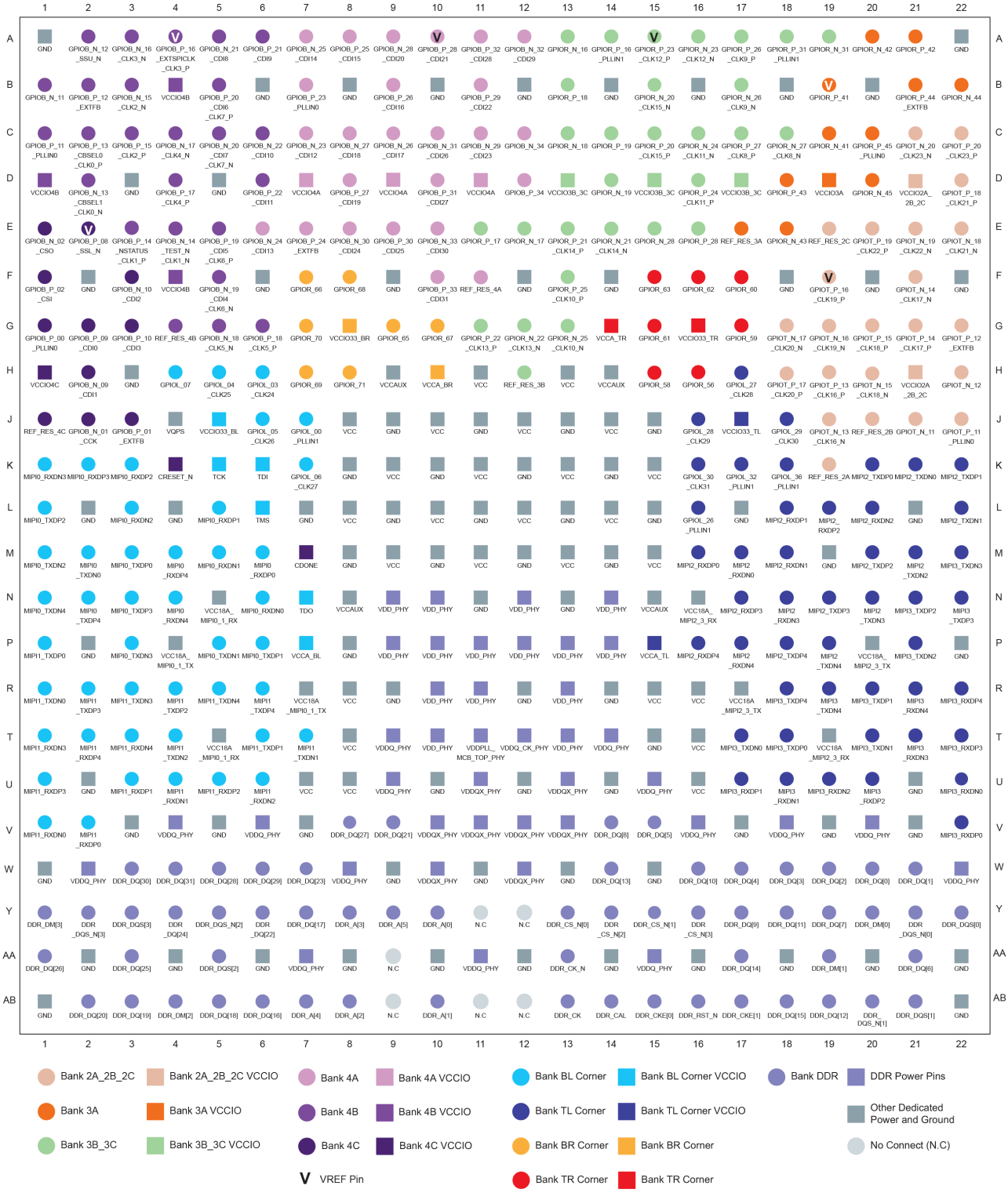


Figure 28: 484-Ball (J) FBGA Emulated MIPI RX Groups

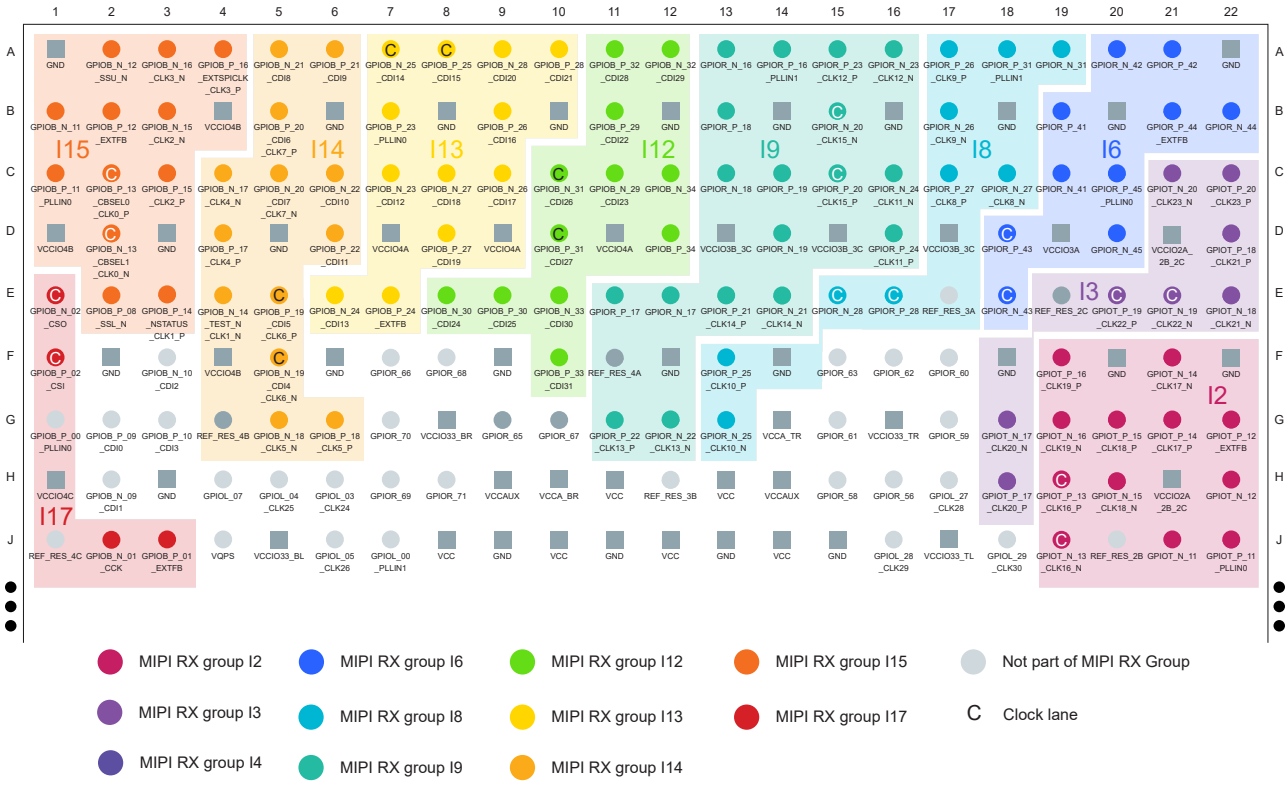


Figure 29: 484-Ball (J) FBGA Package Marking

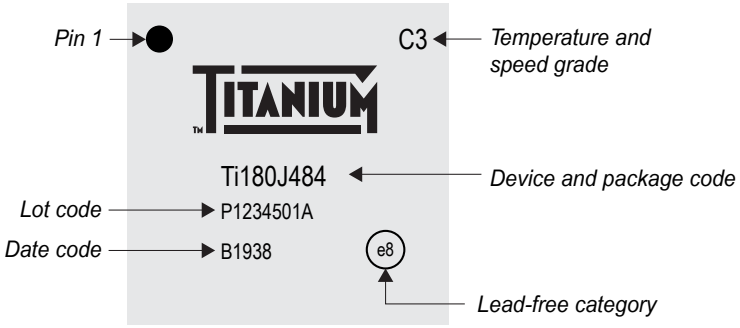
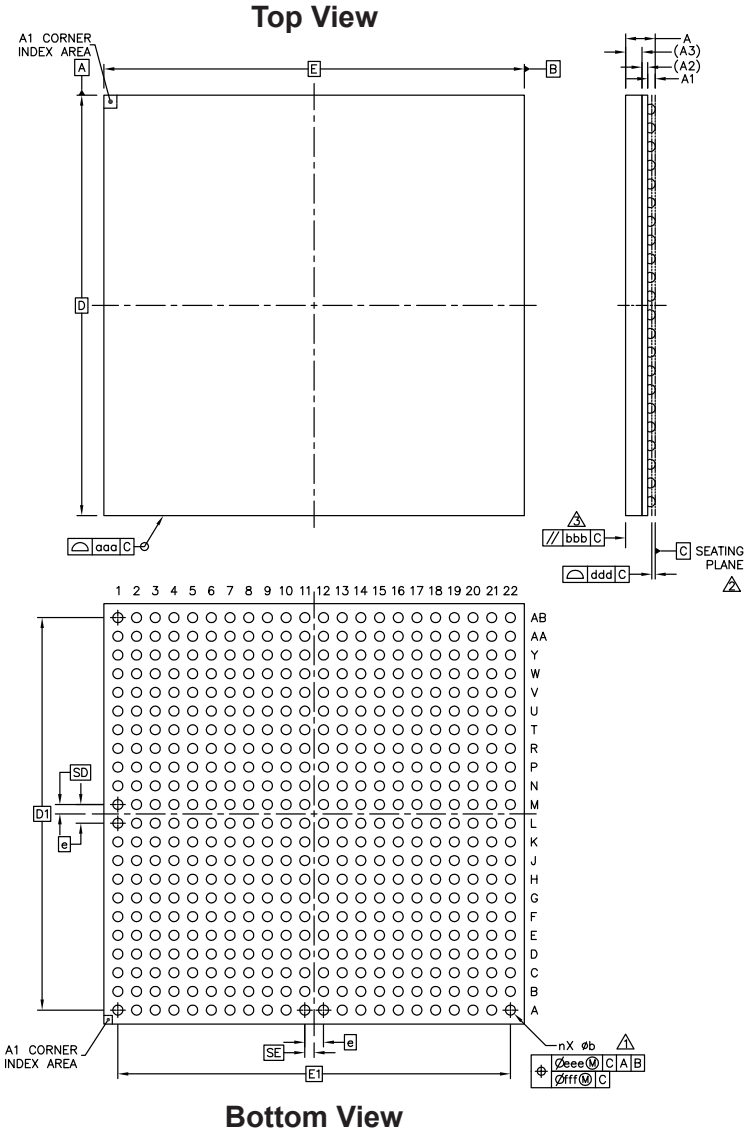


Figure 30: 484-Ball (J) FBGA Package Outline



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	1.193	1.268	1.4
STAND OFF	A1	0.27	0.32	0.37
SUBSTRATE THICKNESS	A2		0.248	REF
MOLD THICKNESS	A3		0.7	REF
BODY SIZE	D		18	BSC
	E		18	BSC
BALL DIAMETER			0.4	
BALL OPENING			0.35	
BALL WIDTH	b	0.38	0.43	0.48
BALL PITCH	e		0.8	BSC
BALL COUNT	n		484	
EDGE BALL CENTER TO CENTER	D1		16.8	BSC
	E1		16.8	BSC
BODY CENTER TO CONTACT BALL	SD		0.4	BSC
	SE		0.4	BSC
PACKAGE EDGE TOLERANCE	aaa		0.15	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.15	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

484-Ball (L) FBGA Package Specifications

Figure 31: 484-Ball (L) FBGA Pinout Diagram

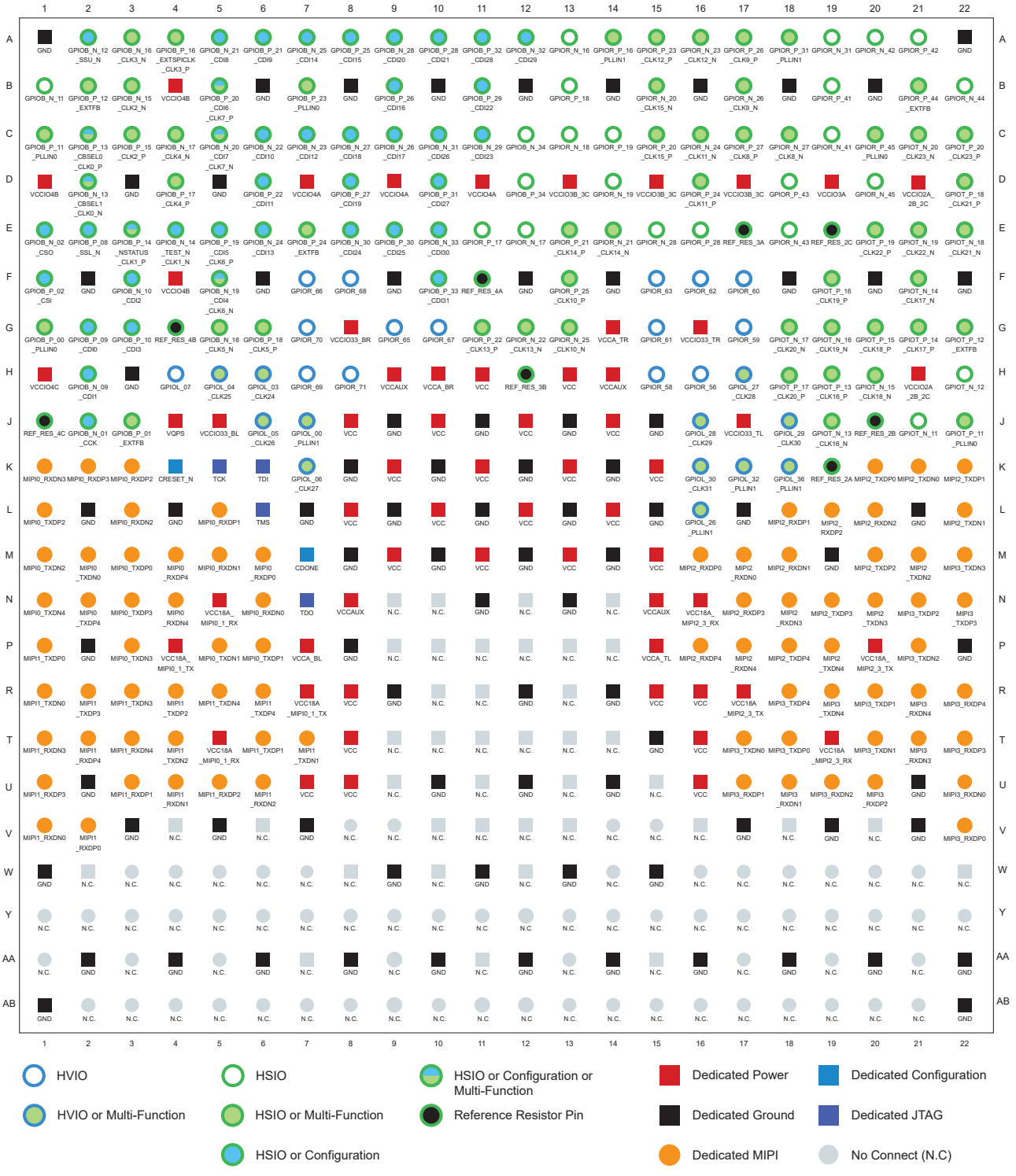


Figure 32: 484-Ball (L) FBGA I/O Bank Diagram

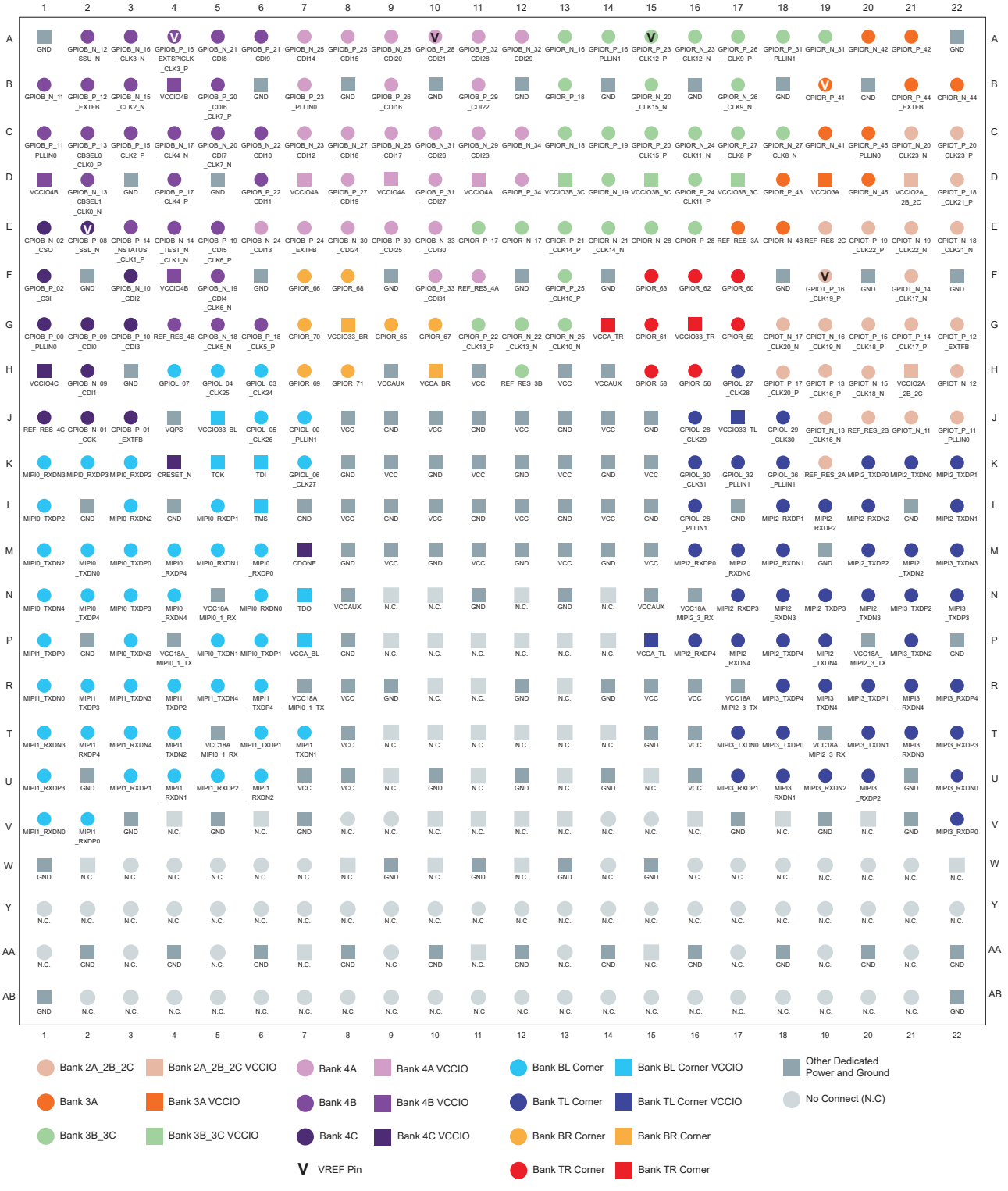


Figure 33: 484-Ball (L) FBGA Emulated MIPI RX Groups

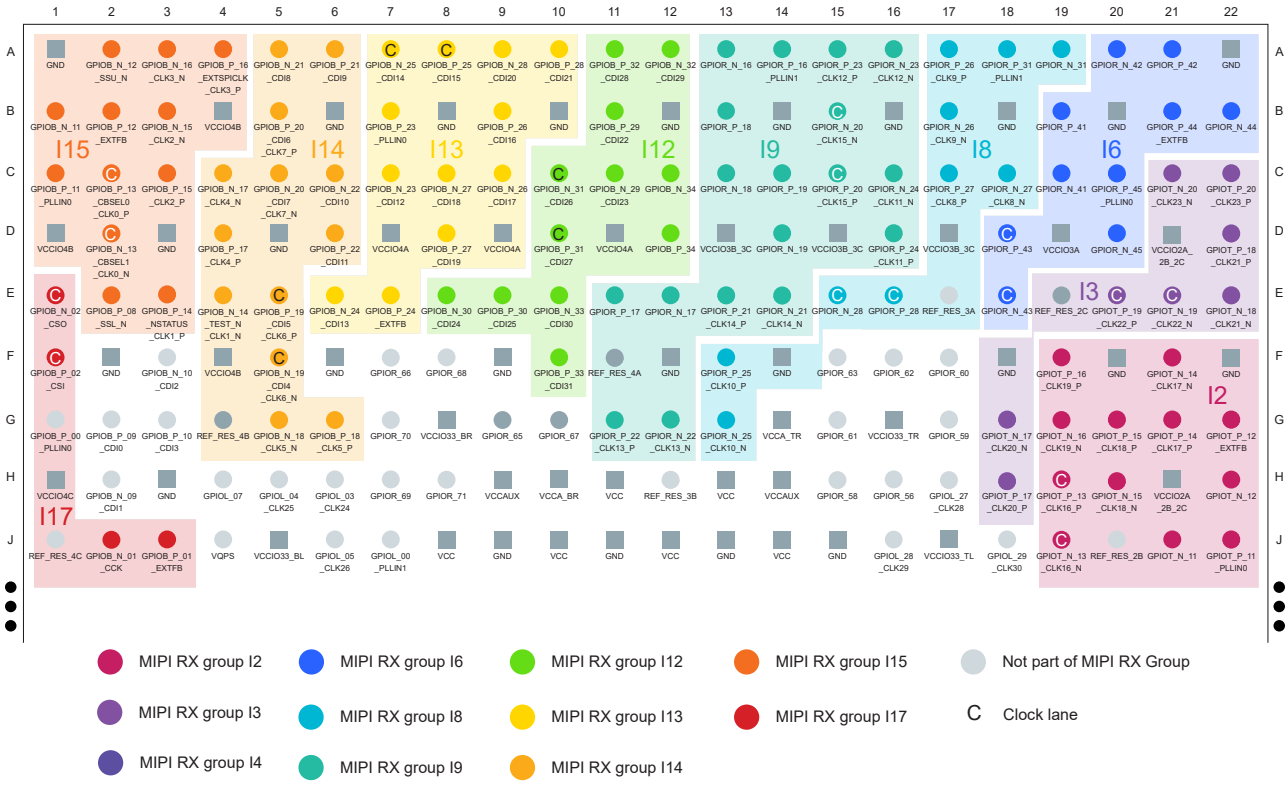


Figure 34: 484-Ball (L) FBGA Package Marking

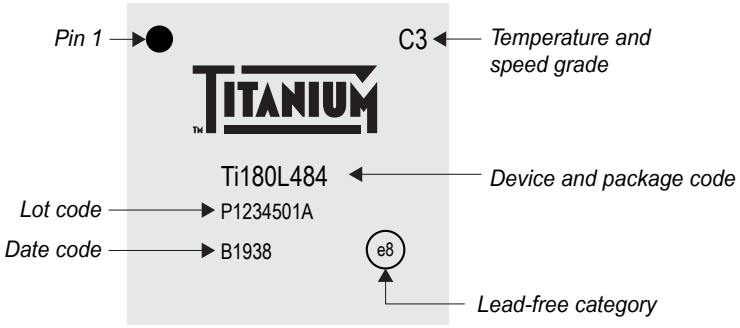
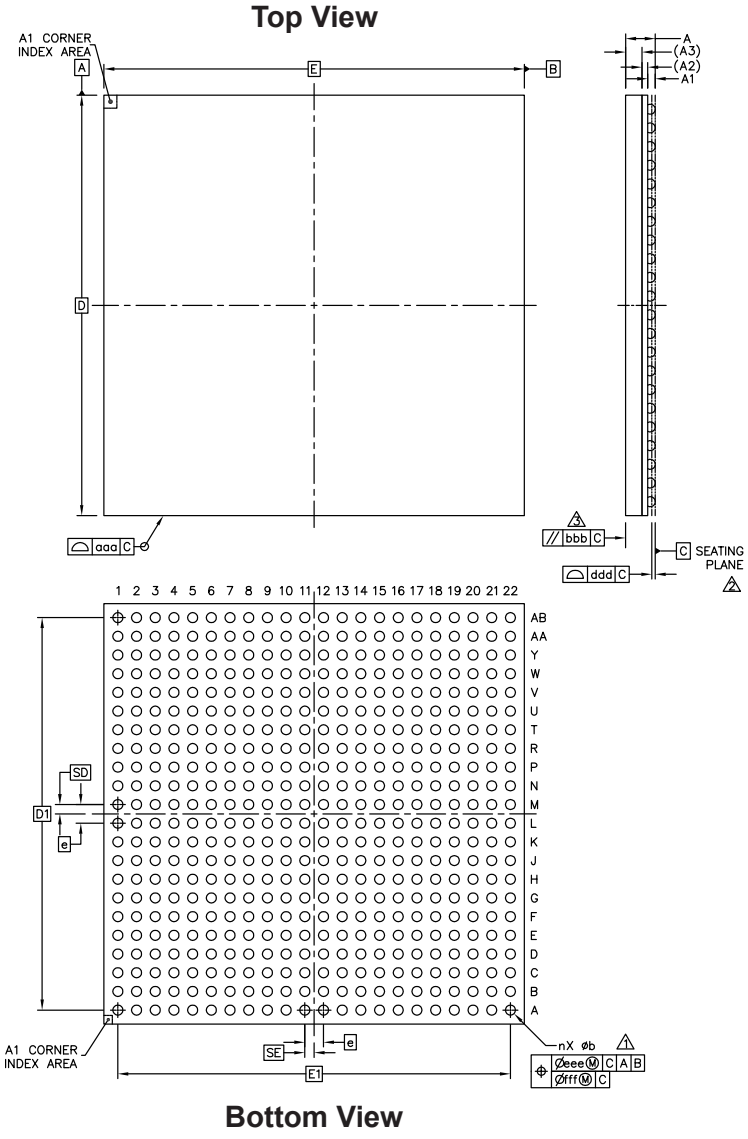


Figure 35: 484-Ball (L) FBGA Package Outline



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	1.193	1.268	1.4
STAND OFF	A1	0.27	0.32	0.37
SUBSTRATE THICKNESS	A2		0.248	REF
MOLD THICKNESS	A3		0.7	REF
BODY SIZE	D		18	BSC
	E		18	BSC
BALL DIAMETER			0.4	
BALL OPENING			0.35	
BALL WIDTH	b	0.38	0.43	0.48
BALL PITCH	e		0.8	BSC
BALL COUNT	n		484	
EDGE BALL CENTER TO CENTER	D1		16.8	BSC
	E1		16.8	BSC
BODY CENTER TO CONTACT BALL	SD		0.4	BSC
	SE		0.4	BSC
PACKAGE EDGE TOLERANCE	aaa		0.15	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.15	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

484-Ball (M) FBGA Package Specifications

Figure 36: 484-Ball (M) FBGA Pinout Diagram

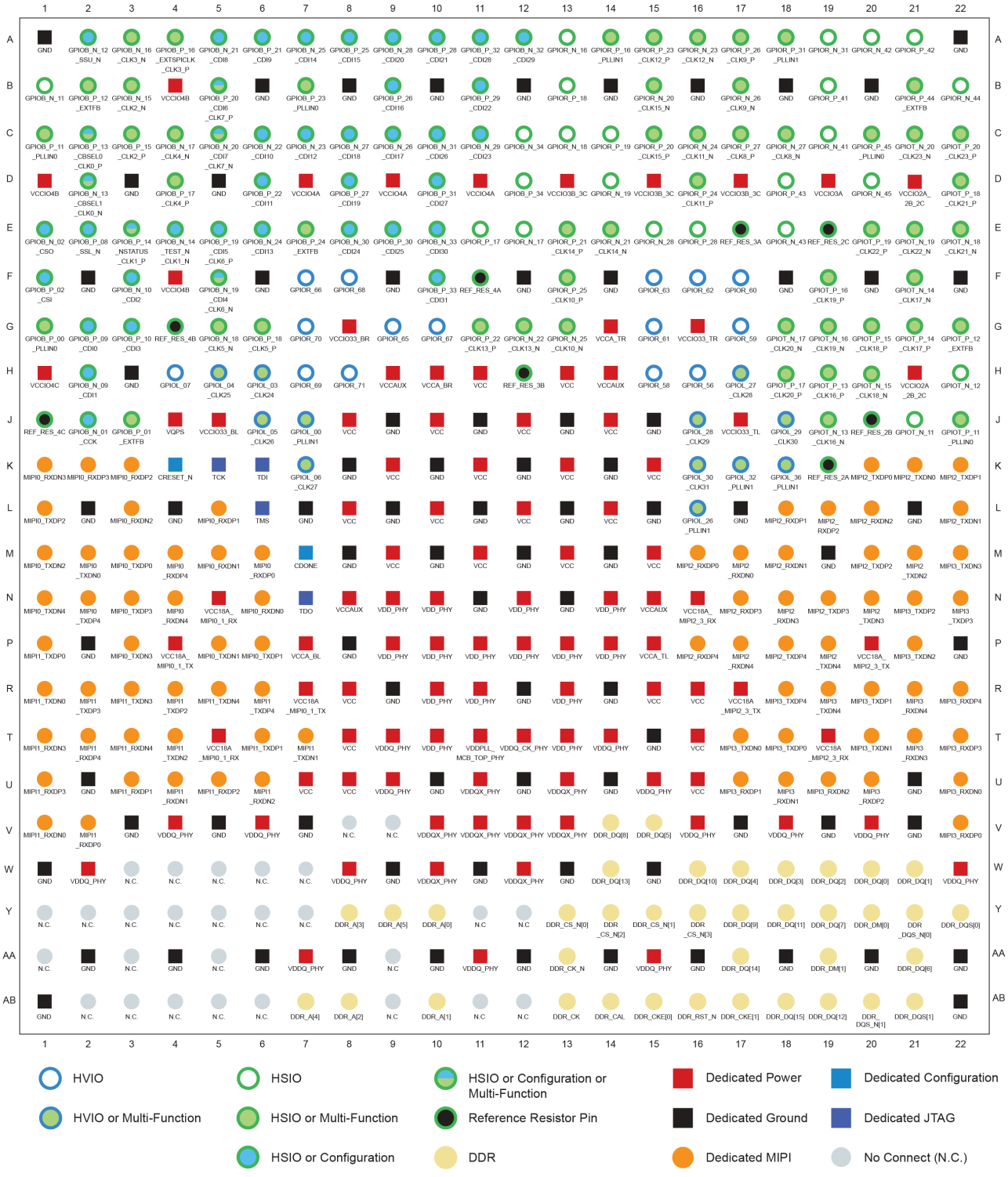


Figure 37: 484-Ball (M) FBGA I/O Bank Diagram

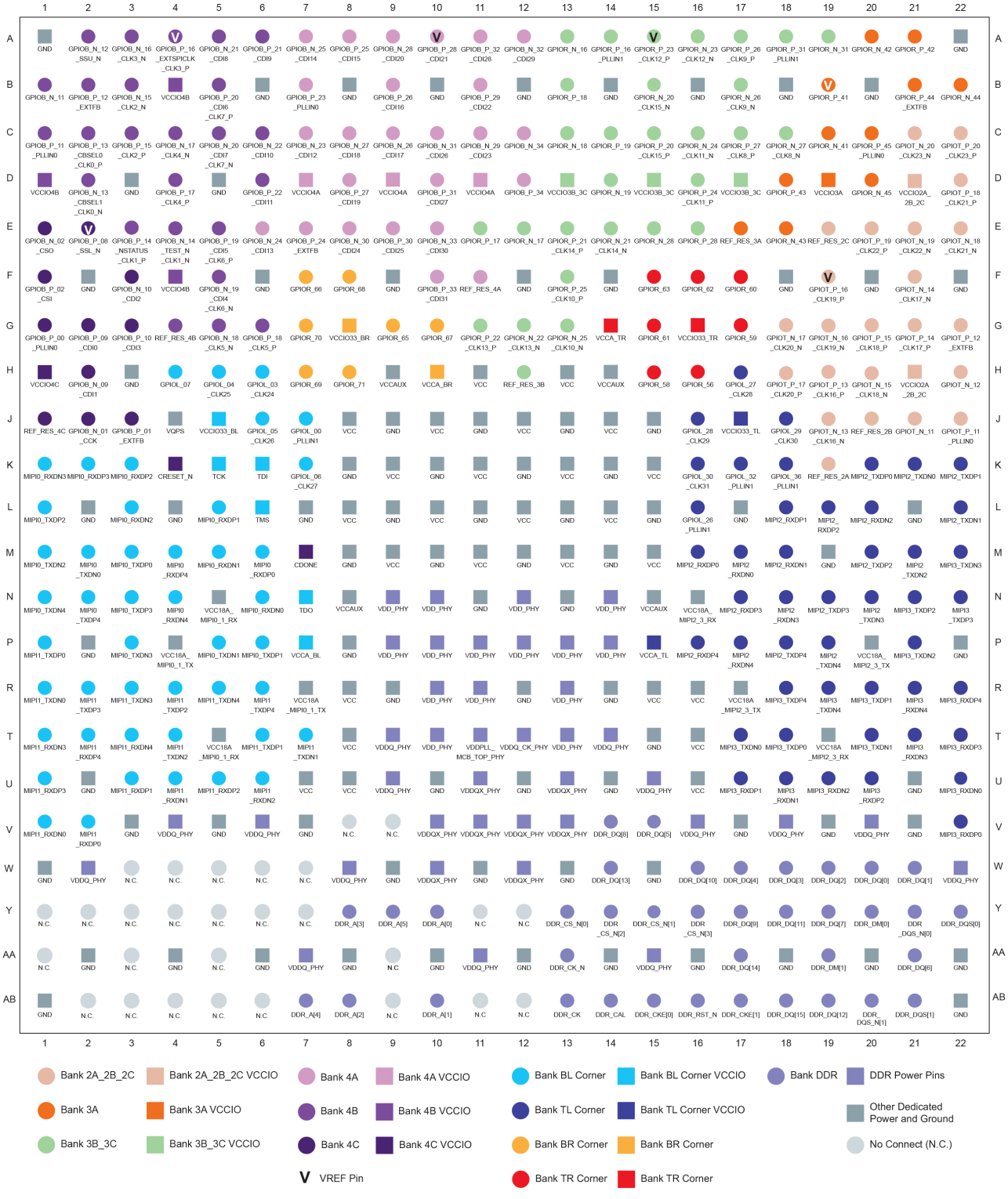


Figure 38: 484-Ball (M) FBGA Emulated MIPI RX Groups

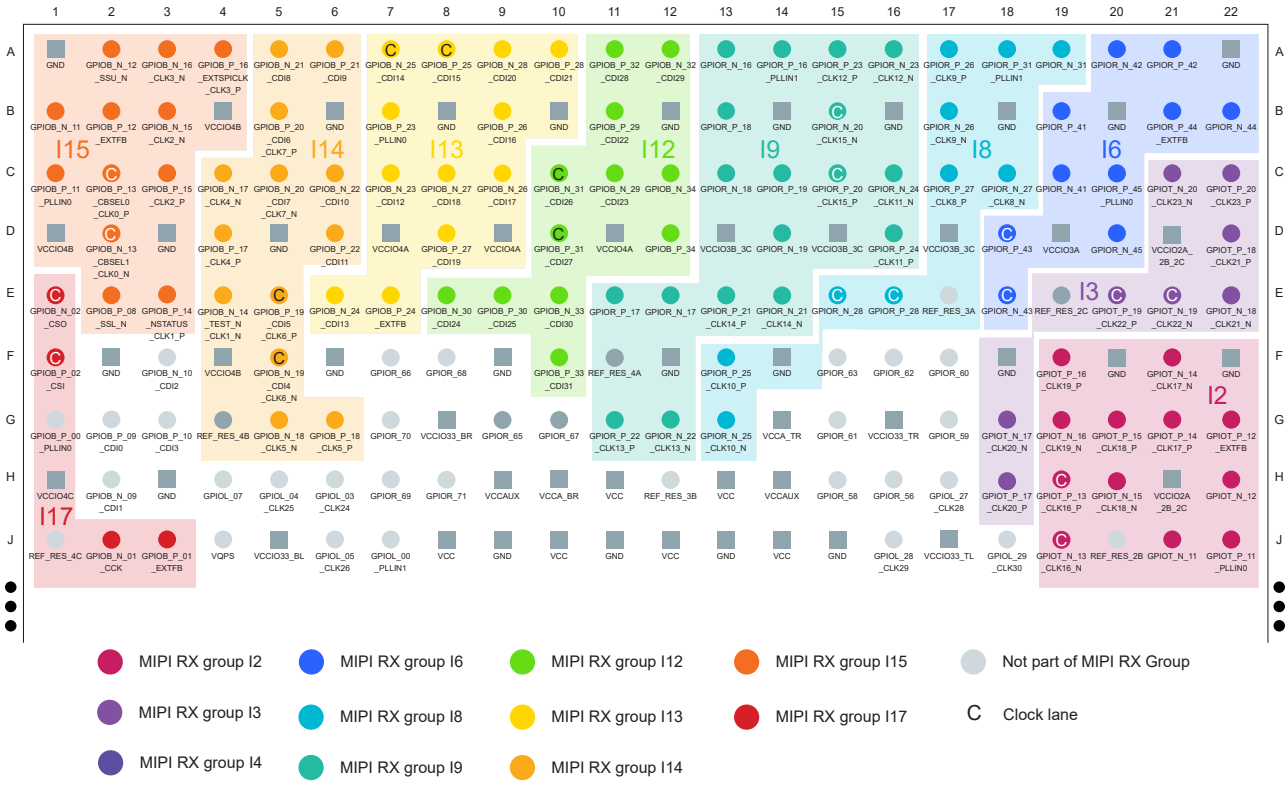


Figure 39: 484-Ball (M) FBGA Package Marking

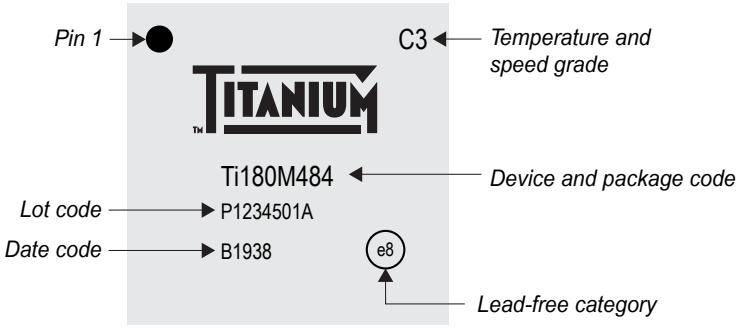
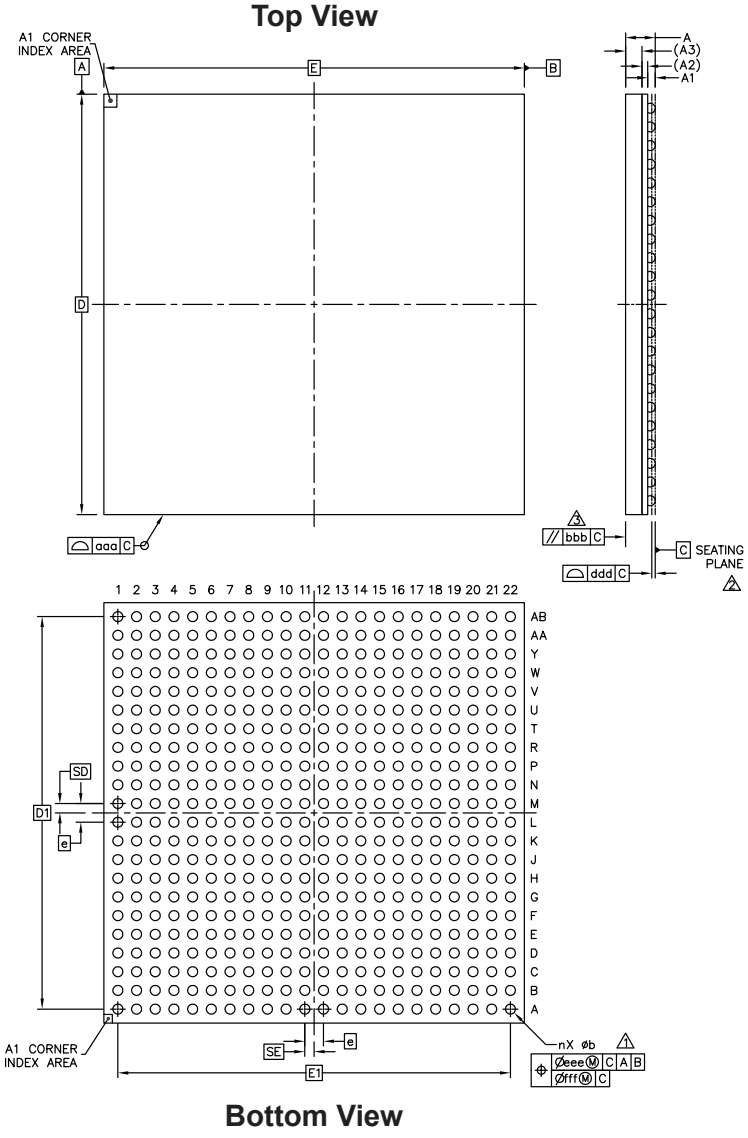


Figure 40: 484-Ball (M) FBGA Package Outline



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	1.193	1.268	1.4
STAND OFF	A1	0.27	0.32	0.37
SUBSTRATE THICKNESS	A2		0.248	REF
MOLD THICKNESS	A3		0.7	REF
BODY SIZE	D		18	BSC
	E		18	BSC
BALL DIAMETER			0.4	
BALL OPENING			0.35	
BALL WIDTH	b	0.38	0.43	0.48
BALL PITCH	e		0.8	BSC
BALL COUNT	n		484	
EDGE BALL CENTER TO CENTER	D1		16.8	BSC
	E1		16.8	BSC
BODY CENTER TO CONTACT BALL	SD		0.4	BSC
	SE		0.4	BSC
PACKAGE EDGE TOLERANCE	aaa		0.15	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.15	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

529-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

529-Ball (G) FBGA Package Specifications

Figure 41: 529-Ball (G) FBGA Pinout Diagram

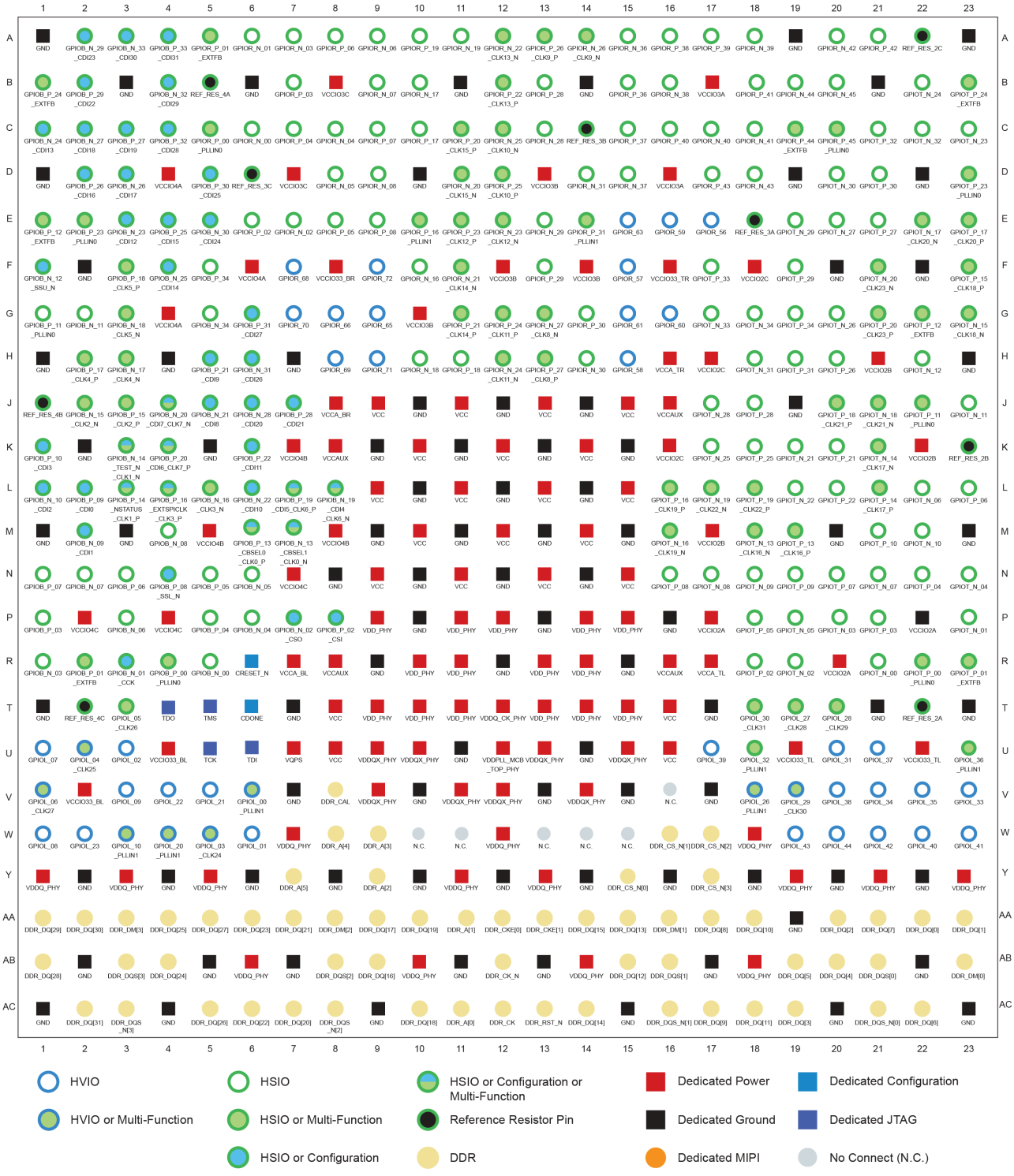


Figure 42: 529-Ball (G) FBGA I/O Bank Diagram

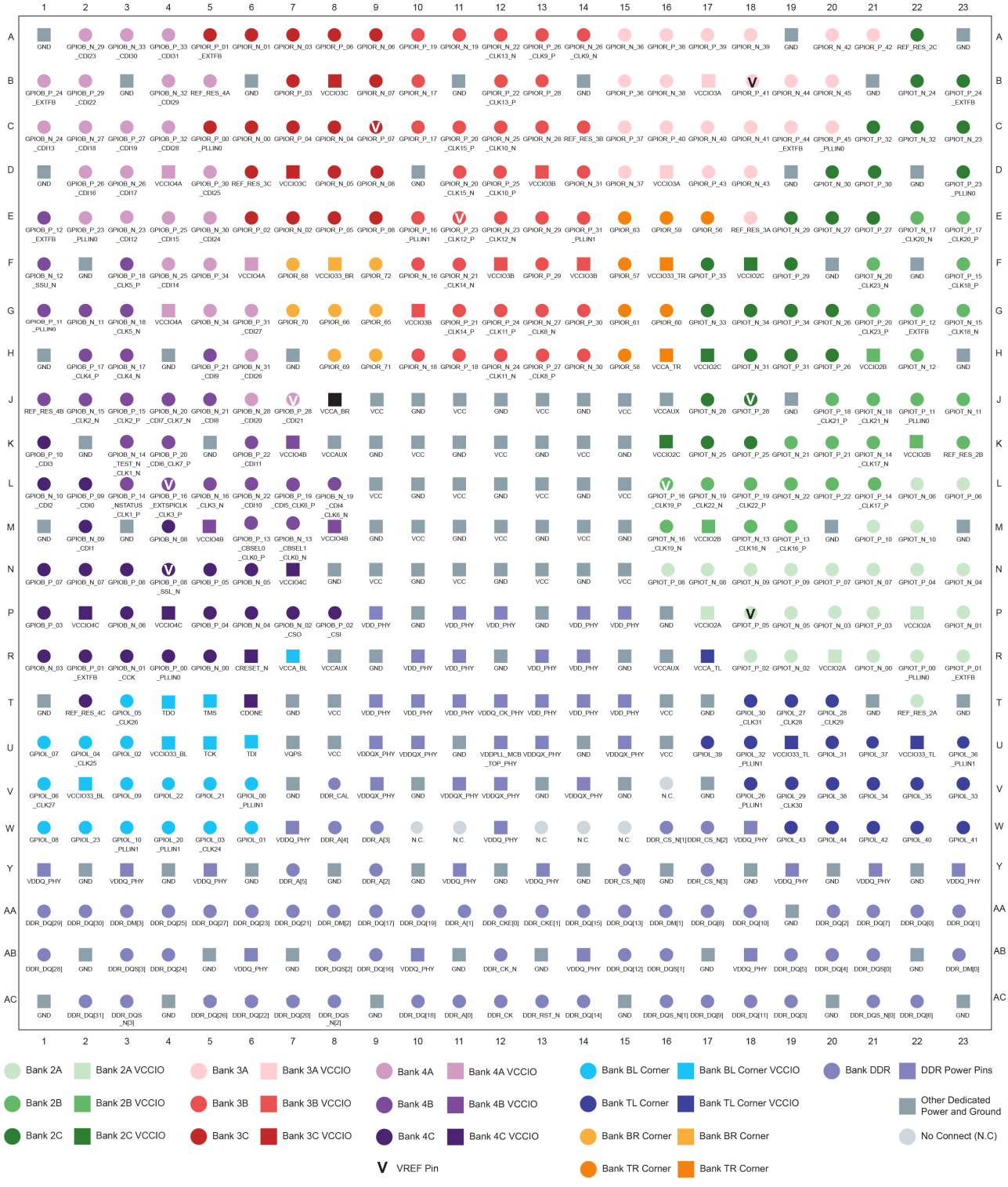


Figure 43: 529-Ball (G) FBGA Emulated MIPI RX Groups

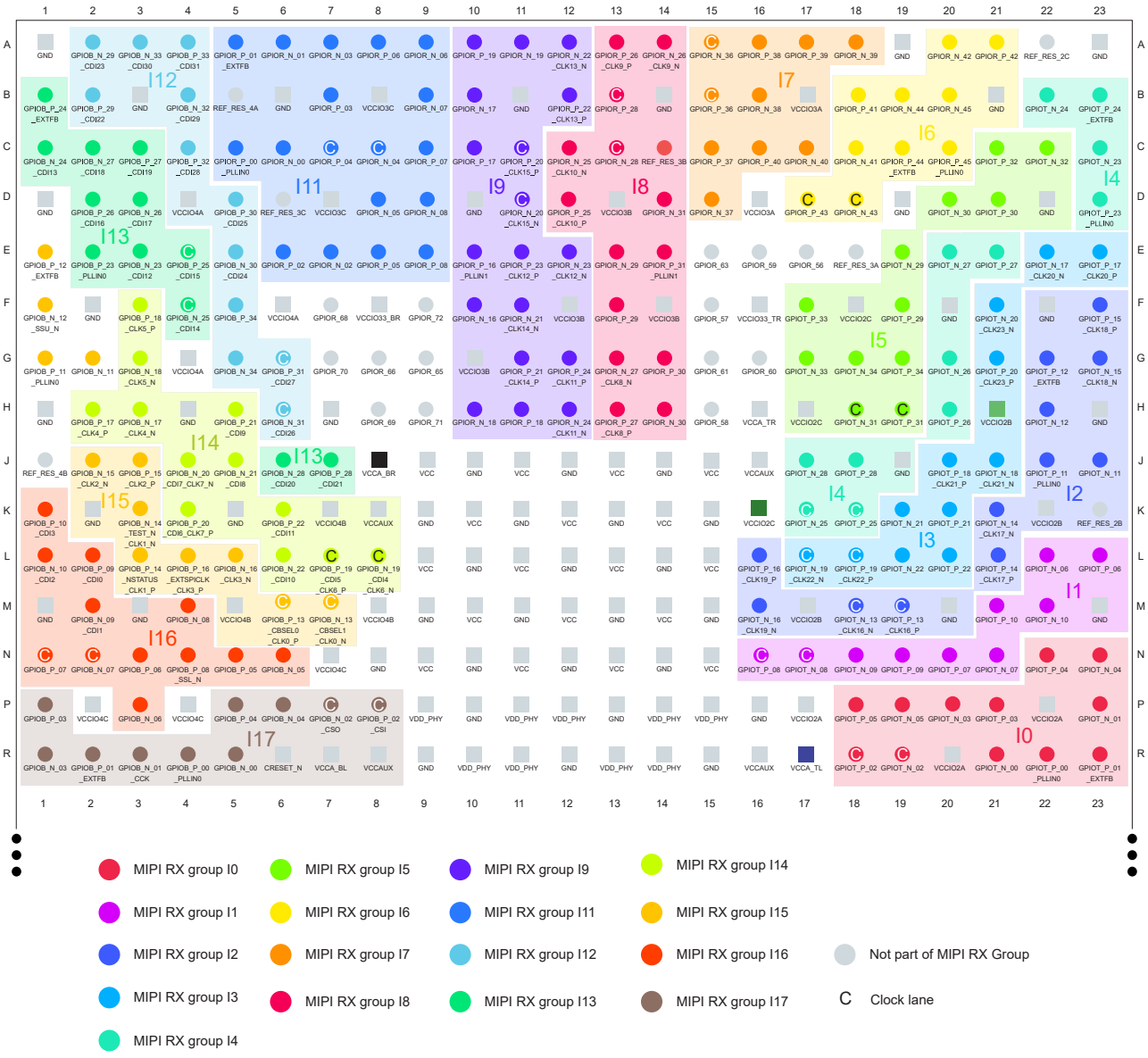


Figure 44: 529-Ball (G) FBGA Package Marking

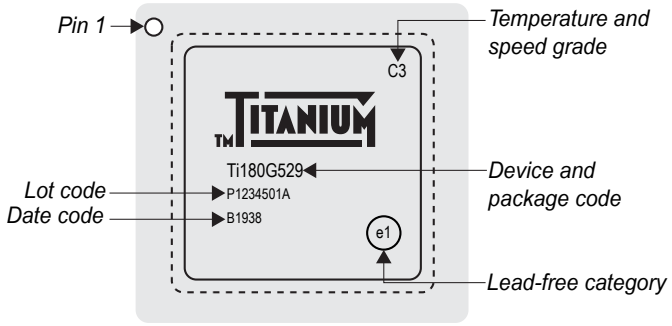
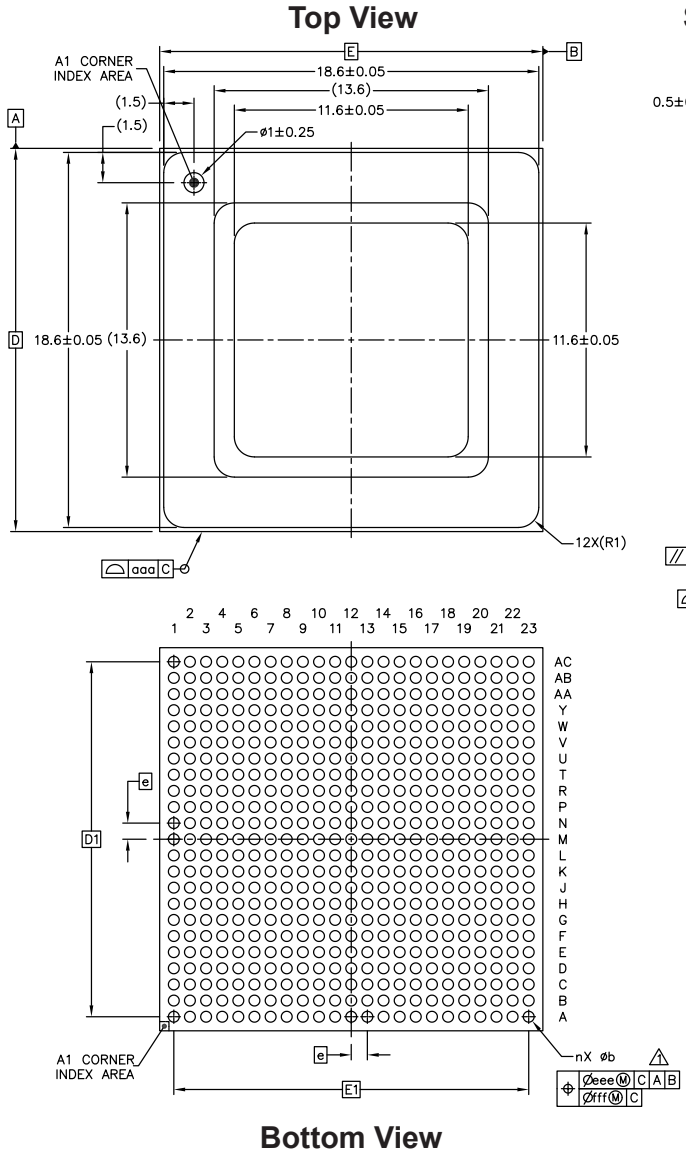


Figure 45: 529-Ball (G) FBGA Package Outline



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	2.72
STAND OFF	A1	0.36	---	0.46
SUBSTRATE THICKNESS	A2		0.765	REF
HEAT SLUG THICKNESS	A3		1.35	REF
BODY SIZE	D		19	BSC
	E		19	BSC
BALL DIAMETER			0.5	
BALL OPENING			0.4	
BALL WIDTH	b	0.44	---	0.64
BALL PITCH	e		0.8	BSC
BALL COUNT	n		529	
EDGE BALL CENTER TO CENTER	D1		17.6	BSC
	E1		17.6	BSC
BODY CENTER TO CONTACT BALL	SD		---	BSC
	SE		---	BSC
PACKAGE EDGE TOLERANCE	aaa		0.15	
SUBSTRATE FLATNESS	bbb		0.25	
COPLANARITY	ddd		0.2	
BALL OFFSET (PACKAGE)	eee		0.25	
BALL OFFSET (BALL)	fff		0.1	

NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

529-Ball (C) FBGA Package Specifications

Figure 46: 529-Ball (C) FBGA Pinout Diagram

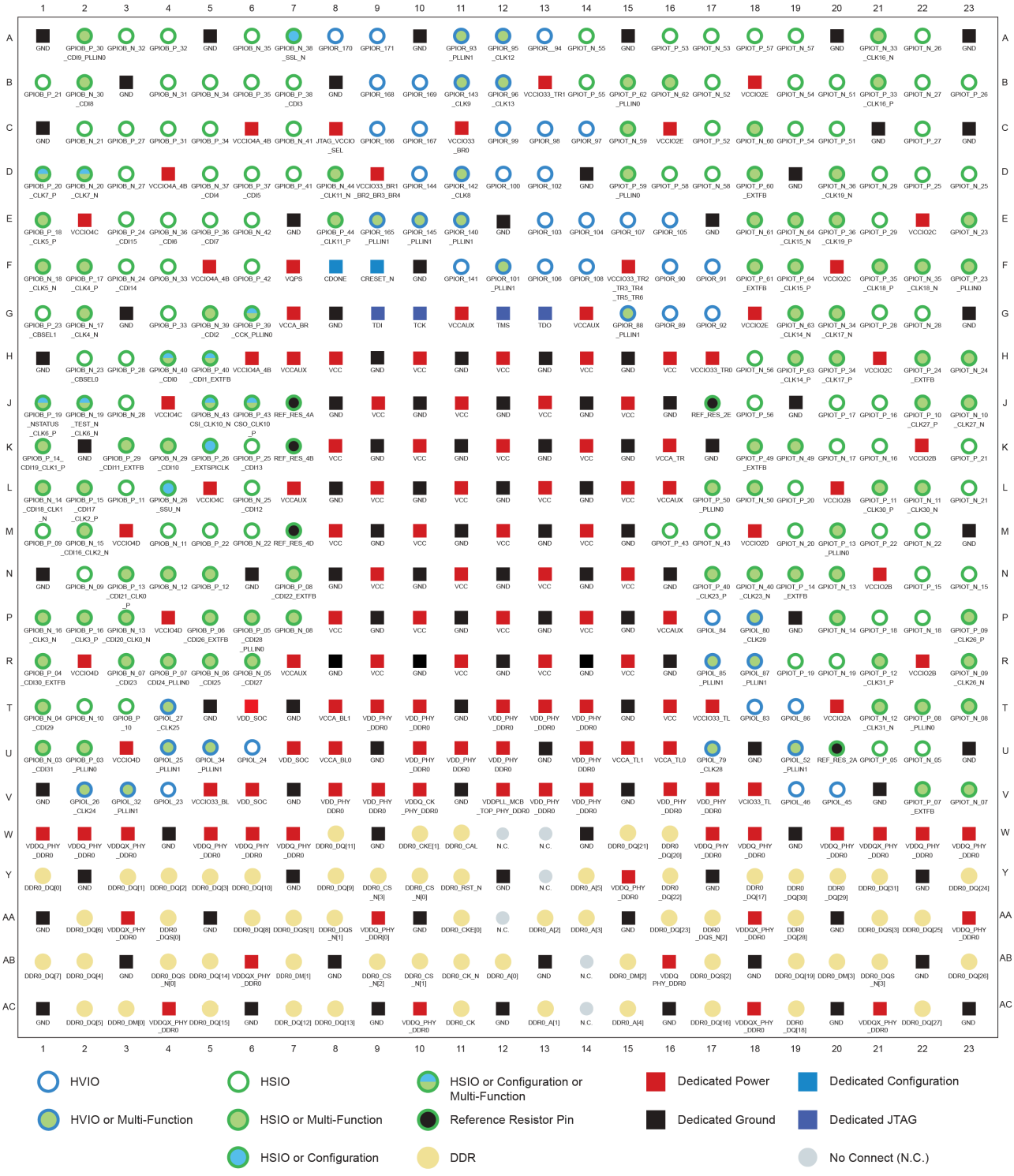


Figure 47: 529-Ball (C) FBGA I/O Bank Diagram

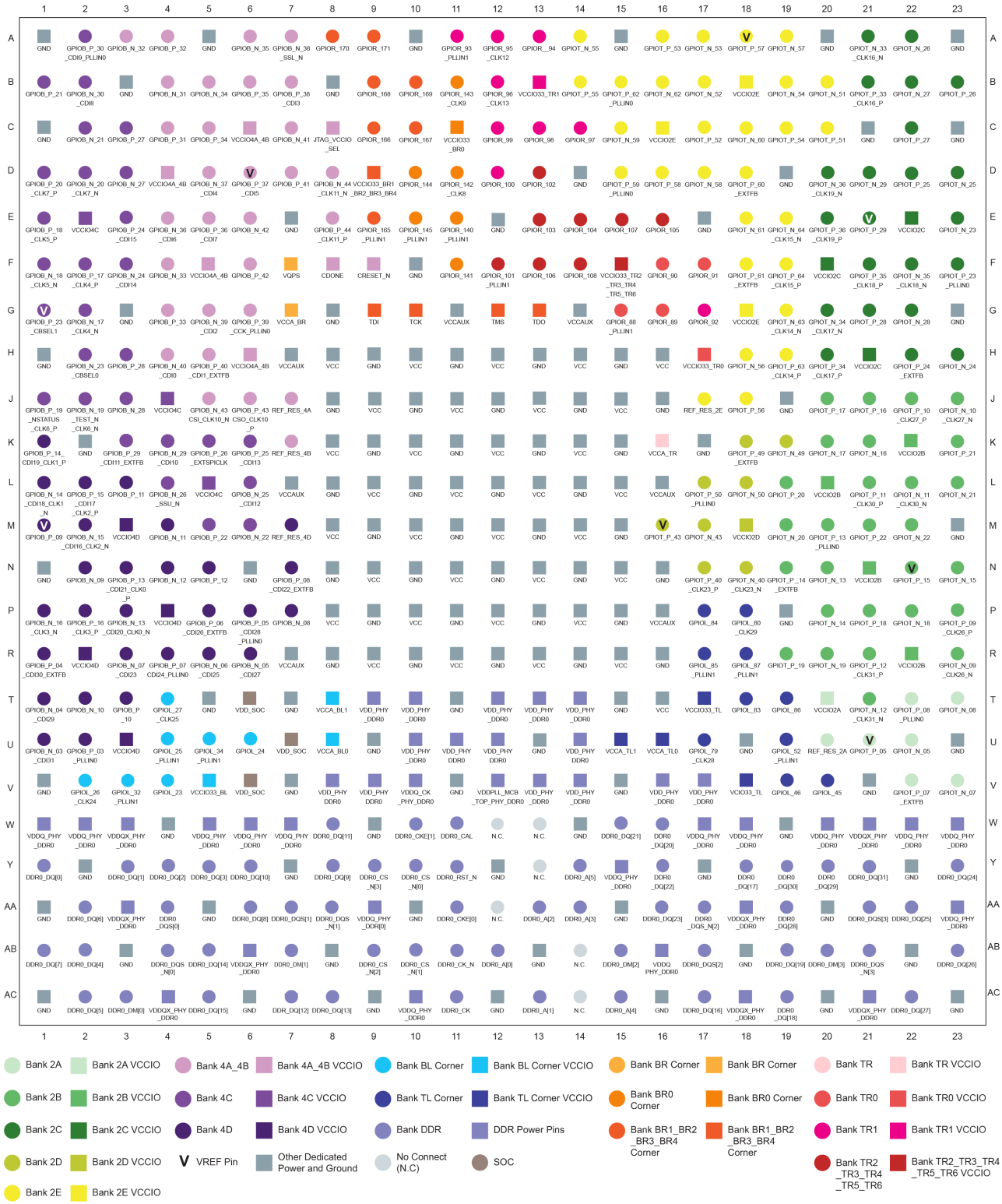


Figure 48: 529-Ball (C) FBGA Emulated MIPI RX Groups

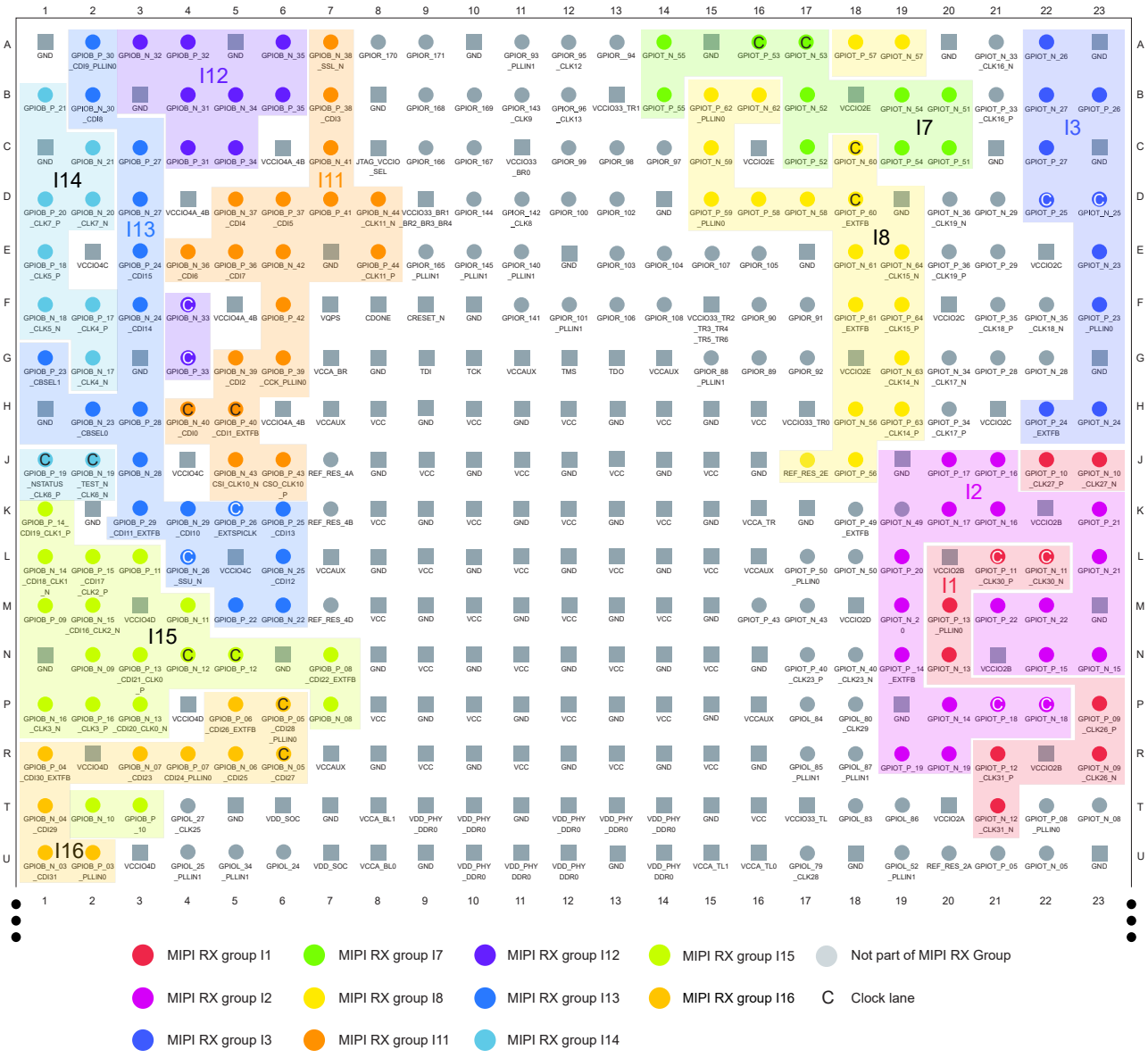


Figure 49: 529-Ball (C) FBGA Package Marking

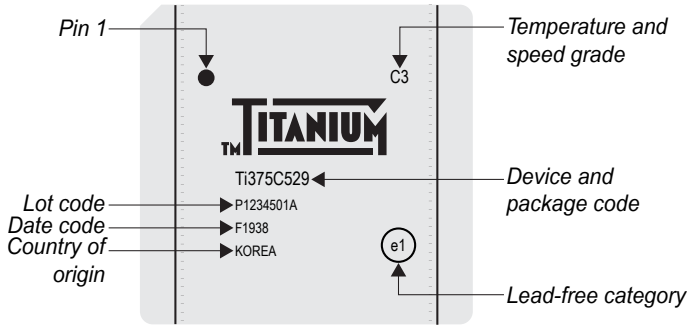
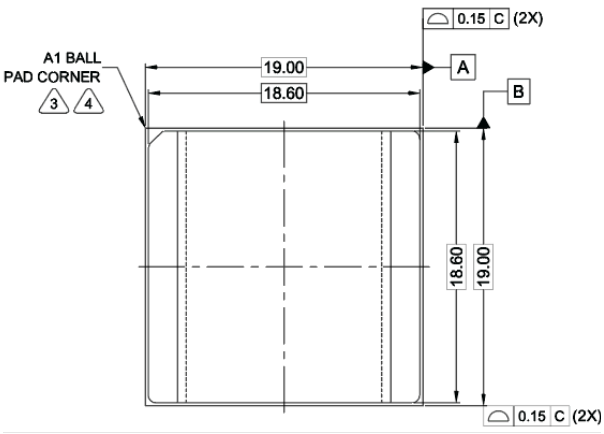
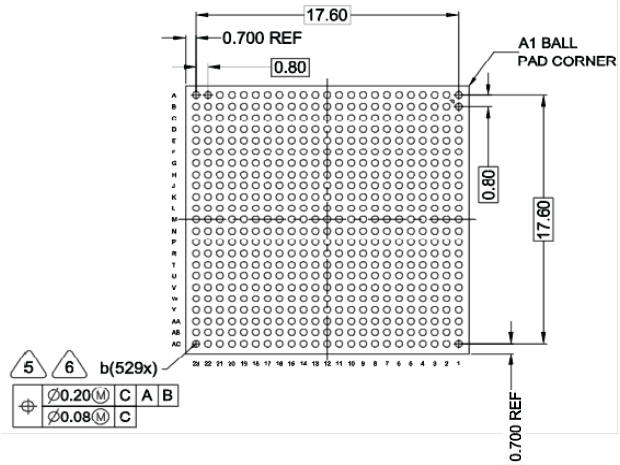


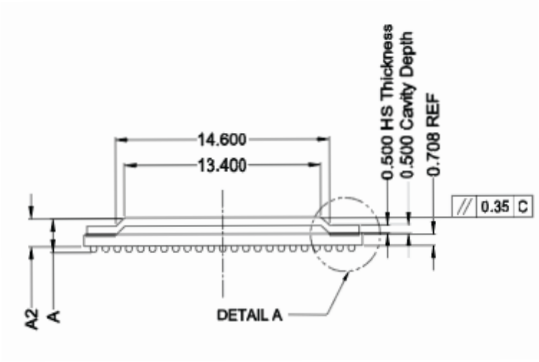
Figure 50: 529-Ball (C) FBGA Package Outline

Top View



Bottom View





Side View

DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A	2.015	2.168	2.321
A1	0.280	0.380	0.480
A2	1.672	1.788	1.904
b	0.400	0.500	0.600
NUMBER OF BALL 529			

NOTES:

1. All DIMENSIONS AND TOLERANCE CONFORM TO ASME Y14.5M-2018.
2. TERMINAL POSITIONS DESIGNATION PER JESD 95.
3. CORNER DETAILS PER JCET OPTION.
4. PIN 1 IDENTIFIER CAN BE CHAMFER, INK MARK, LASERED MARK, METALLIZED MARK.
5. BALL DIAMETER AFTER REFLOW.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM C.
7. USING ϕ0.500MM RAW SOLDER BALL SIZE DURING ASSEMBLY.

Solder Reflow Guidelines for Surface-Mount Devices

This section provides general guidelines for solder reflow process for Efinix® surface-mount FPGAs. The data used in this document is based on IPC/JEDEC (Association Connecting Electronics Industries/JEDEC Solid State Technology Association) standards. Each printed circuit board (PCB) has its profile, which depends upon the board design and the reflow equipment used. You must characterize each PCB to find a reliable profile.

Reflow

During solder reflow, follow these guidelines:

- Use caution when profiling to ensure that the maximum temperature difference between components is less than 10 °C.
- For best results, perform forced convection reflow with nitrogen.

Inspection

Follow these inspection guidelines:

- **Pre-reflow**—Use visual inspection to verify solder paste dispense location and quantity.
- **Pick and place**—Use machine vision as necessary to ensure proper component placement.
- **Post reflow**—Use electrical testing to verify solder joint formation.

BGA Reballing

Efinix does not recommend BGA reballing. Reballed BGA packages void the original Efinix® specifications.

Peak Reflow Temperatures

Table 12: Peak Reflow Temperature (T_p) by Package

Package	Moisture Sensitivity Level	Peak Reflow Temperature (+0/-5 °C)
WLCSP	1	260
FBGA	3	260

Note: These packages are "green" and RoHS compliant.

Reflow Profile for SMT Packages

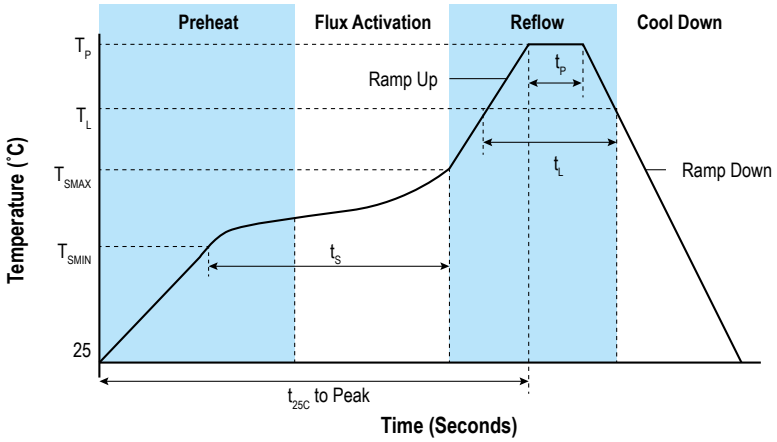
The reflow process usually includes four phases:

1. **Preheat Phase—**The preheat phase brings the assembly from 25 °C to T_S. During this phase, the solvent evaporates from the solder paste. The preheat temperature ramp rate should be less than 2 °C/second to avoid solder balling defects such as solder ball spattering and bridging.
   - **Solder Ball Spattering—**Spattering, the most common solder balling defect, is caused by solvents evaporating explosively. To eliminate spattering, use a slower temperature rise in the preheat phase.
   - **Bridging—**Bridging is usually caused by inaccurate or splashy screen printing, and can often occur with fine pitch components. It can also be caused by solder paste slumping during a rapid temperature rise in the preheat phase.
2. **Flux Activation Phase—**As the temperature rises slowly, it reaches a point at which the flux completely wets the surfaces to be soldered.
3. **Reflow Phase—**The temperature rises to a level sufficient to reflow the solder. The flux wicks surface oxides and contaminants away from the melted solder, resulting in a clean solder joint.
4. **Cool Down Phase—**Ramp down the temperature as fast as possible to control grain size; however, do not exceed 6 °C/second.

Table 13: Peak Reflow Temperature (T_P) Parameters

Parameter	Description	Specification (Lead and Halogen Free Packages)
Ramp up	Average ramp-up rate (T_{SMAX} to T_P)	3 °C/second maximum
T_{SMIN}	Preheat peak minimum temperature	150 °C
T_{SMAX}	Preheat peak maximum temperature	200 °C
t_s	Time between T_{SMIN} and T_{SMAX}	60 - 120 seconds
T_L	Solder melting point	217 °C
t_L	Time maintained above T_L	60 - 150 seconds
t_P	Time within 5 °C of peak temperature	30 seconds
Ramp down	Ramp-down rate	6 °C/second maximum
t_{25C} to T_p	Time from 25 °C to peak temperature	8 minutes maximum

Figure 51: Thermal Reflow Profile



Thermal Resistance

Thermal management is an important consideration when designing your system. Efinix® device data sheets describe the maximum allowable junction temperature so you can assess your system's thermal characteristics. To ensure that the device and package do not exceed the junction temperature requirements, you should always complete a thermal analysis of your specific design.

The data shown in this section is relative and actual values depend on a variety of factors such as die size, paddle size, airflow, power applied, printed circuit board design, the proximity of other devices, and user applications. Because of this, Efinix FPGAs do not come with preset thermal solutions.

Table 14: Device/Package Thermal Resistance

Measurements taken at 25 °C ambient temperature.

Package	Pitch	Dimensions (mm)	Θ_{JA} (°C/W) Still Air	Θ_{JA} (°C/W) 1 m/s	Θ_{JA} (°C/W) 2 m/s	Θ_{JB} (°C/W)	Θ_{JC} (°C/W)
WLCSP64	0.4	3.5 x 3.4	37.24	33.56	32.42	11.95	0.14
F100	0.5	5.5 x 5.5	45.62	41.53	40.14	26.13	20.35
F225	0.65	10 x 10	36.89	33.15	32.03	22.32	11.03
J361	0.65	13 x 13	17.50	14.76	13.85	6.07	2.04
G400	0.8	16 x 16	15.42	13.06	12.16	5.34	1.53
J484, L484, M484	0.8	18 x 18	16.25	13.56	12.70	6.53	3.89
G529	0.8	19 x 19	12.58	10.14	9.20	3.31	1.12
C529	0.8	19 x 19	(3)	(3)	(3)	(3)	(3)

Where:

- Θ_{JA} is the junction-to-ambient thermal resistance
- Θ_{JB} is the junction-to-board thermal resistance
- Θ_{JC} is the junction-to-case thermal resistance

(3) Pending characterization.

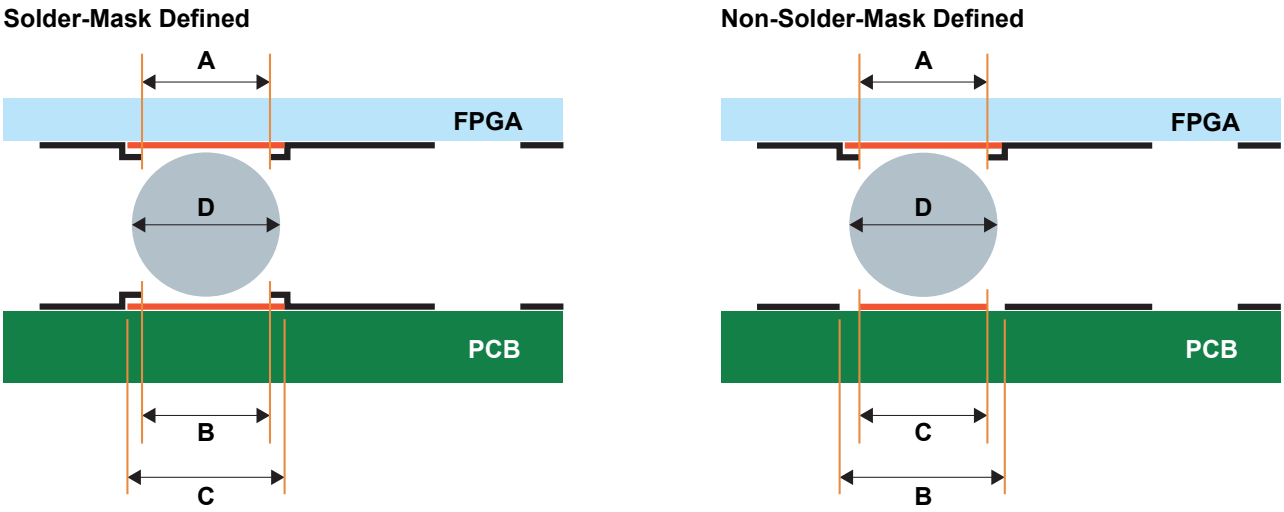
PCB Guidelines for BGA Packages

PCB Solder Pad Guidelines

Efinix provides solder mask defined (SMD) and non-solder mask defined (NSMD) diameter information. Use this data when creating your board landing pads.

Non-solder-mask defined (NSMD) pad designs perform better than solder mask defined pads due to lower stresses in the solder near the top of pad. Additionally, they provide a better "grip" area around the pad edge. For best reliability, the Generic Requirements for Surface Mount Design and Land Pattern Standard (IPC-7351A) recommends a NSMD pad with a diameter that is slightly smaller than the solder ball.

Figure 52: SMD and Non-SMD Pad Specification



Legend:

A: BGA package solder mask opening
B: Optimum PCB solder mask opening
C: Optimum PCB pad size
D: Solder ball diameter

Table 15: PCB Solder Pad Recommendations

Package	Pitch (mm)	A	SMD		Non-SMD		D
		BGA Package Solder Mask Opening (mm)	B Optimum PCB Solder Mask Opening (mm)	C Optimum PCB Pad Size (mm)	B Optimum PCB Solder Mask Opening (mm)	C Optimum PCB Pad Size (mm)	Solder Ball Diameter (mm)
W64	0.4	N/A	0.2	0.25	0.3	0.2	0.2
F100	0.5	0.25	0.25	0.3	0.35	0.2	0.25
F225	0.65	0.3	0.3	0.35	0.45	0.3	0.35
J361	0.65	0.3	0.3	0.35	0.45	0.3	0.35
G400	0.8	0.35	0.35	0.4	0.5	0.35	0.4
J484, L484, M484	0.8	0.35	035	0.4	0.5	0.35	0.4
G529	0.8	0.4	0.4	0.5	0.6	0.4	0.5
C529	0.8	0.45	0.45	0.55	0.6	0.4	0.5

Routing between Pads on the Top Layer

You can route signal trace between solder pads on the top layer of the PCB while meeting the clearance requirement.

Figure 53: Routing Traces between Pads on the Top Layer

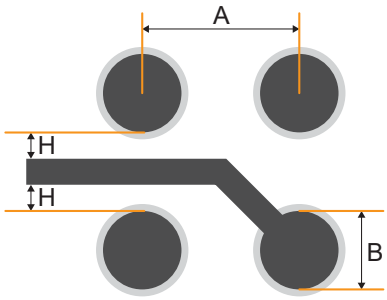


Table 16: Routing Measurements

Measurement	Description	Package								Unit
		W64	F100	F225	J361	G400	J484, L484, M484	G529	C529	
A	Ball pitch.	0.4	0.5	0.65	0.65	0.8	0.8	0.8	0.8	mm
	Ball ϕ.	0.2	0.25	0.35	0.35	0.4	0.4	0.5	0.5	mm
B	Width of the solder landing pad ϕ. (SMD)	0.25	0.3	0.35	0.35	0.4	0.4	0.5	0.55	mm
	Width of the solder landing pad ϕ. (NSMD)	0.2	0.2	0.3	0.3	0.35	0.35	0.4	0.4	mm
H (min.)	Minimum space between the trace and the landing pad. (SMD)	(4)	0.06	0.08	0.08	0.1	0.1	0.08	0.08	mm
	Minimum space between the trace and the landing pad. (NSMD)	(4)	0.08	0.08	0.08	0.1	0.1	0.08	0.08	mm

(4) The via is under the pad, no traces between landing pads.

Guidelines for Vias

You use vias to drop routing down to lower layers. This type of via, called an "offset via," is very robust. The solder mask completely covers the via, which prevents short circuits during paste application, allows for paste overprinting, and prevents etch entrapment.

PCB fabricators use a laser drill for these size vias. Confirm that your fabricator can maintain the tight tolerances required to ensure adequate clearances between vias and pads.

Figure 54: Via Dimensions

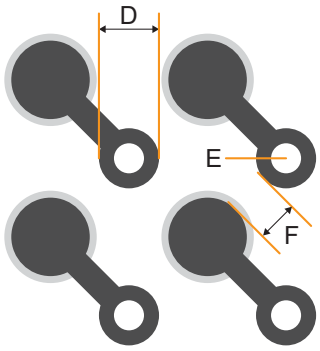


Table 17: Via Measurements

Measurement	Description	Package							Unit
		W64	F100	F225	J361	G400	J484, L484, M484	C529, G529	
D	Via capture pad width.	0.25	0.25	0.3	0.3	0.45	0.45	0.45	mm
E	Finished via ϕ.	0.127	0.127[5]	0.15	0.15	0.225	0.225	0.225	mm
F (min.)	Space between the landing pad and via.	[6]	0.072	0.1	0.1	0.1	0.1	0.08	mm

[5] This is a laser via.
[6] The via is under the pad, no traces between landing pads.

Routing through Different PCB Layers

You can route a trace between two solder pads, at the outer two rows of solder pads on the top layer. If you use all of the top-layer routing tracks to route the first and second rows, the inner rows of solder pads must connect to another routing layer with vias for routing outside of the BGA area.

You can use this method to route all of the inner solder pads. Because there is only enough space to route one trace between vias, you need an additional routing layer for every inner row of solder pads after the fourth row.

Figure 55: BGA Trace Routing for Top and Second Layers

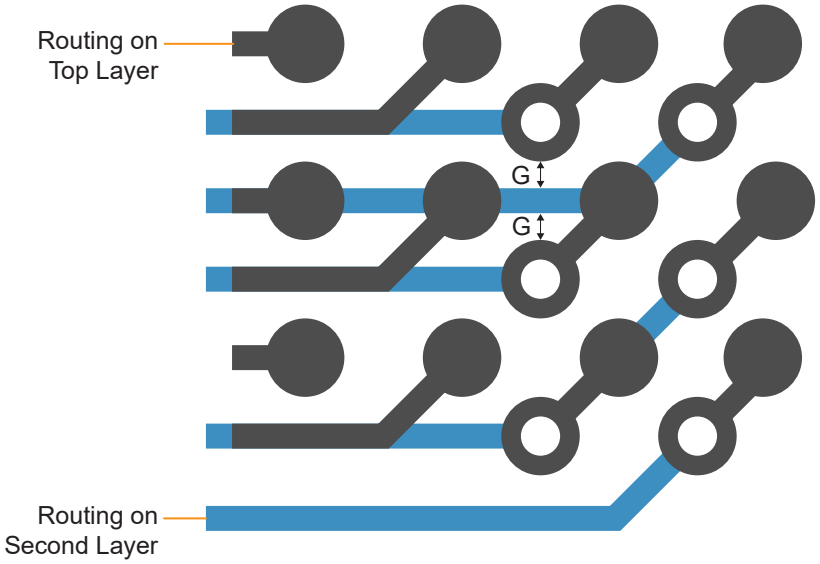


Table 18: Routing Measurements

Measurement	Description	Package							Unit
		W64	F100	F225	J361	G400	J484, L484, M484	C529, G529	
G (min.)	Minimum space required between via and trace.	0.08	0.08	0.08	0.08	0.08	0.08	0.08	mm

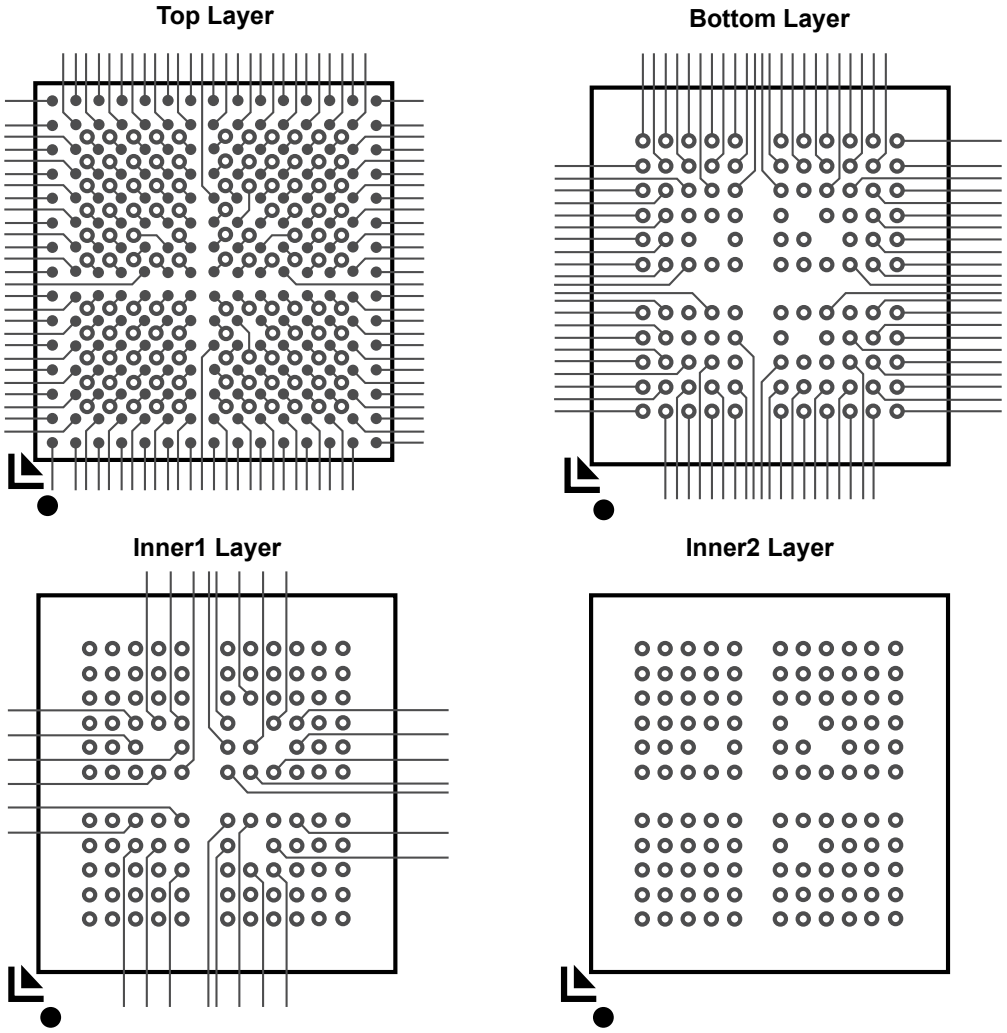
F225 Escape Routing

The following table and figure show how to perform escape routing for the F225 package. These guidelines are one example of acceptable routing using three PCB layers. You can do a different escape routing scheme with a different number of layers. The minimum number of PCB layers is four.

Table 19: Titanium F225 PCB Escape Routing Parameter

Parameter	Specification	Unit
Width of the solder landing pad ϕ	0.35	mm
Width of the solder mask opening ϕ	0.45	mm
Trace width	0.08	mm
Clearance	0.08	mm
Via capture pad width	0.4	mm
Via drill diameter	0.2	mm

Figure 56: 4-Layer Titanium F225 PCB Escape Routing Diagram



Titanium FPGAs Solder Ball

Refer to the table for the recommended type of solder ball used for Titanium FPGAs:

Table 20: Titanium FPGAs Solder Ball

Device	Solder Ball Type
Ti35/Ti60F100S3F2	SAC305
Ti35/Ti60F225	SAC305
Ti60WLCSP64	SAC405
Ti90/Ti120/Ti180J361	LF35
Ti90/Ti120/Ti180G400	LF35
Ti90/Ti120/Ti180J484	LF35
Ti90/Ti120/Ti180G529	SAC305
Ti135/Ti200/Ti375C529	SAC305

Green Packaging

Efinix FPGAs use packaging solutions that are safer for the environment. These packages are lead (Pb) free and are RoHS compliant. Efinix refers to these products as "green" packaging.

Tape and Reel Packaging

Efinix offers WLCSP devices in tape and reel packaging.

Table 21: Tape and Reel Packaging

Package	Carrier Width (mm)	Cover Width (mm)	Pitch (mm)	Reel Size (in)	Maximum Quantity per Reel
WLCSP64	12	9.5	8	13	2,500

Figure 57: Pin 1 Location (WLCSP64 Packages)

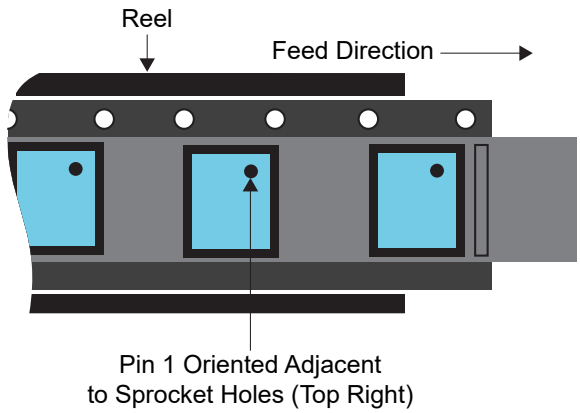
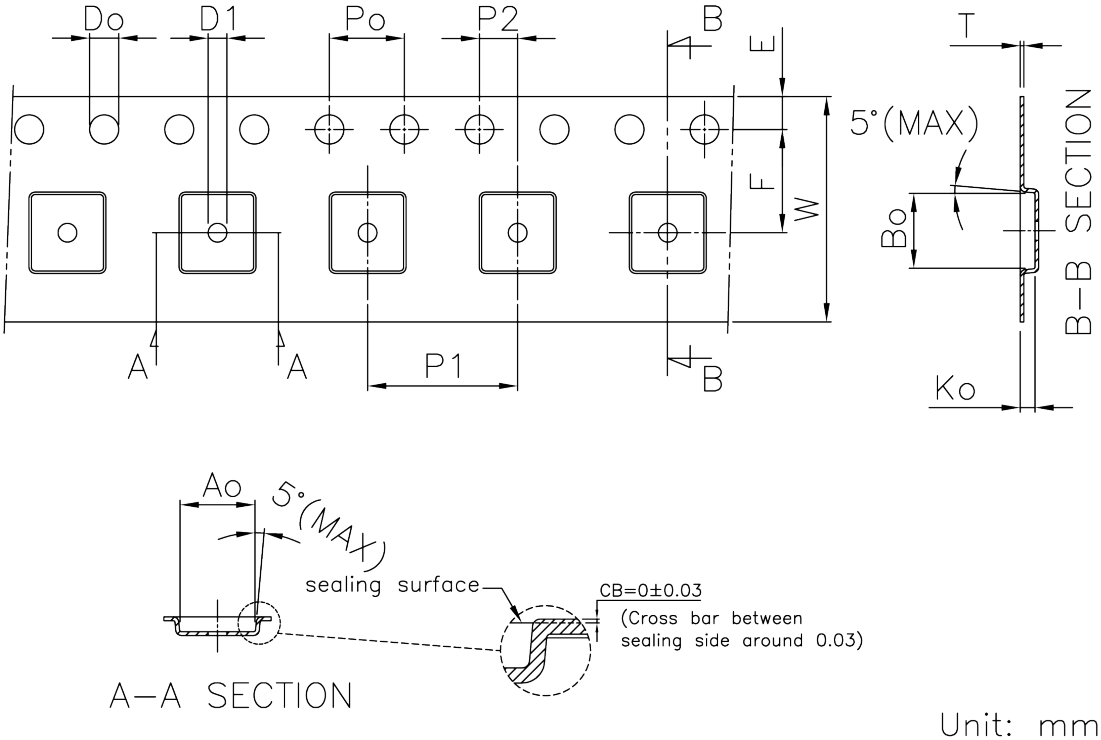


Figure 58: Tape Outline (WLCSP64 Packages)



Unit: mm

Symbol	Ao	Bo	Ko	Po	P1	P2	T
Spec	3.59±0.05	3.75±0.05	0.67±0.05	4.00±0.10	8.00±0.10	2.00±0.05	0.25±0.03
Symbol	E	F	Do	D1	W	10Po	
Spec	1.75±0.10	5.50±0.05	$1.50^{+0.10}_{-0}$	1.00±0.05	12.0±0.30	40.0±0.20	

Notice:

1. 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.
2. Carrier camber shall be not more than 1mm per 250mm.
3. Ao & Bo measured on a place in the middle of corner radii.
4. Ko measured from a place on the inside bottom of the pocket to top surface of carrier.
5. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
6. Surface resistivity $\geq 1.0*10^{5}$ & $\leq 1.0*10^{8}$ ohm/sq.
7. Tooling type : Male tooling.

Tray Packaging

Efinix offers BGA devices in tray packaging.

Table 22: Tray Packaging

Package	Quantity per Tray	Tray Matrix	Tray Stack	Quantity per Stack
F100	490	14 x 35	10 + 1	4,900
F225	168	8 x 21	10 + 1	1,680
J361	119	7 x 17	10 + 1	1,190
G400	84	6 x 14	10 + 1	840
J484, L484, M484	84	6 x 14	10 + 1	840
G529	60	5 x 12	5 + 1	300
C529	84	6 x 14	10 + 1	840

Revision History

Table 23: Revision History

Date	Version	Description
March 2024	5.4	Removed M361 and F529 packages. (DOC-1769)
February 2024	5.3	Added in new section Titanium FPGAs Solder Ball. (DOC-1709) Added C529 Package. (DOC-1582) Updated pinout descriptions. Updated Titanium Package Options table in Available Package Options section. Updated package marking and outline for F225 and updated package marking for M361, G400, J484, L484, M484, F529, G529, and C529. Updated Tray Packaging for C529 package.
September 2023	5.2	Added package specifications for Ti90, Ti120, and Ti180 G400 package. (DOC-1392) Corrected bank for TDO signal in I/O bank figures for J484, L484, and M484 packages. (DOC-1416) Added in thermal resistance information for G529 and J529 packages. (DOC-1426) Updated the lead-free category for 100-ball and 225-ball FPGA Package Marking. Updated table Peak Reflow Temperature (T_p) by Package.
April 2023	5.1	Update the package specification for Ti60 F225 package due to change of thickness. (DOC-1211)
February 2023	5.0	Added J361, J484 and G529 packages. (DOC-1137) Updated REF_RES_3A pin connection requirement in the Pinout Description topic.

Date	Version	Description
December 2022	4.1	Updated pinout and I/O bank figures for M484 and F529 packages. (DOC-1045) Updated configuration pins external weak pull-up requirements. (DOC-1035)
September 2022	4.0	Added F529 package. Updated PCB guidelines. Updated tray packaging.
July 2022	3.0	Added M361 package. Added L484 package. F484 package renamed as M484.
February 2022	2.0	Added F484 package. Updated available package options table.
December 2021	1.2	Updated PCB Solder Pad Recommendations, Routing Measurements, and added PCB Routing Example. (DOC-649) Updated A7 pin name in 64-Ball WLCSP diagrams.
September 2021	1.1	Updated PCB guidelines. (DOC-504) Updated W64 package outline. (DOC-504) Updated available package options.
June 2021	1.0	Initial release.