Efinity® Programmer User Guide

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Introduction

Efinix provides a standalone Windows Programmer for use on lab machines or in a manufacturing environment. This tool has the same features as the Programmer provided with the Efinity® software, and works on 32- and 64-bit Windows operating systems.

The standalone Programmer uses a bitstream file (**.hex** for SPI programming or **.bit** for JTAG programming) that you generate with the Efinity® software to program Trion® FPGAs.

Learn more: For information on generating a bitstream file or on using the Efinity® software, refer to the Efinity Software User Guide.

Software Requirements

- Windows 8.1 or later, 32 or 64 bit
- Zadig software to install USB drivers
  zadig.akeo.ie

Configuration Modes

Trion® FPGAs have dedicated configuration pins. You select the configuration mode by setting the appropriate condition on the input configuration pins. Trion® FPGAs support the following configuration modes.

Table 1: Configuration Modes

Mode	Description
SPI Active (serial/parallel)	The Trion® FPGA load the bitstream itself from non-volatile SPI flash memory.
SPI Passive (serial/parallel)	An external microprocessor or microcontroller sends the bitstream to the Trion® FPGA using the SPI interface.
JTAG	A host computer send instructions through a download cable to the Trion® FPGA's JTAG interface using JTAG instructions.
SPI Active using JTAG Bridge	The Efinity® software includes the Flash Controller Utility that gives you full control over a SPI flash device and lets you perform actions comparable to an FTDI flash controller chip. The **SPI Active using JTAG Bridge** programing mode lets you write a new user image to flash. See the Flash Controller Utility User Guide and flash controller example design in the Support Center for more information.

About USB Drivers

To program Trion® FPGAs using the Efinity® software and programming cables, you need to install drivers.

Efinix development boards have an FTDI FTDI2232 chip that facilitates communication through the USB connector. You need to install a driver for each board that you want to program.

For your own development board, Efinix suggests using the FTDI Chip FT2232H Mini Module for JTAG programming Trion® FPGAs. (You can use any JTAG cable for JTAG functions other than programming.)

You can also use the FTDI Chip C232HMDDHSL-0 programming cable, however, the FT2232H Mini Module has a better power and ground plane design, which reduces noise and makes it a more robust solution compared to the cable.

Note: Refer to the FTDI Chip web site for more information about the module or cable.

Install the USB Driver (Windows)

The following instructions explain how to install a USB driver for Windows.

1. Download the Zadig software from zadig.akeo.ie. (You do not need to install it; simply run the downloaded executable.)
2. Run the Zadig software.

   Note: To ensure that the USB driver is persistent across user sessions, run the Zadig software as administrator.

3. Choose **Options > List All Devices**.
4. Turn off **Options > Ignore Hubs or Composite Parents**.
5. Select the board, cable or module to target:
   - Select the Efinix development board; if there is more than one, choose the one shown as a composite.
   - If you are using the FTDI Chip C232HM-DDHSL-0 programming cable or FT2232H Mini Module, select **FTDIBUS (<*version*>)** and USB ID **0403 6014**.
6. Select one of the following options in the **Driver** drop-down list. (Do **not** choose WinUSB.)

Option	Description
libusb-win32 (*version*)	This driver is more stable for unplug/plug events. This driver does not work when debugging with OpenOCD.
libusbK (*version*)	Use this driver if you plan to use OpenOCD to debug any Efinix RISC-V SoC.

7. Click **Replace Driver**.
8. Repeat step 2 for each unique JTAG device you want to target. For example, if you want to use both the T8 and T20 development boards, you must install 2 USB drivers, one for each board.
9. Close the Zadig software.

When you open the Device Manager in the Windows Control Panel, it displays the new USB device driver.

Note: The FTDI (FT2232) chips on Efinix development boards communicate with the USB port. These chips have separate channels for SPI and JTAG. Therefore, you **must** install the driver for the composite parent, **not** for the individual SPI and JTAG interfaces. If you install the driver for each interface, each interface appears as a unique FTDI device, which will make it hard to select the correct port during programming. Hint: the interface names end with *(Interface N)*, where *N* is the channel number; do not choose these.

Using the GUI Programmer

The graphical user interface makes it easy to select images and program FPGAs. To use the Programmer:

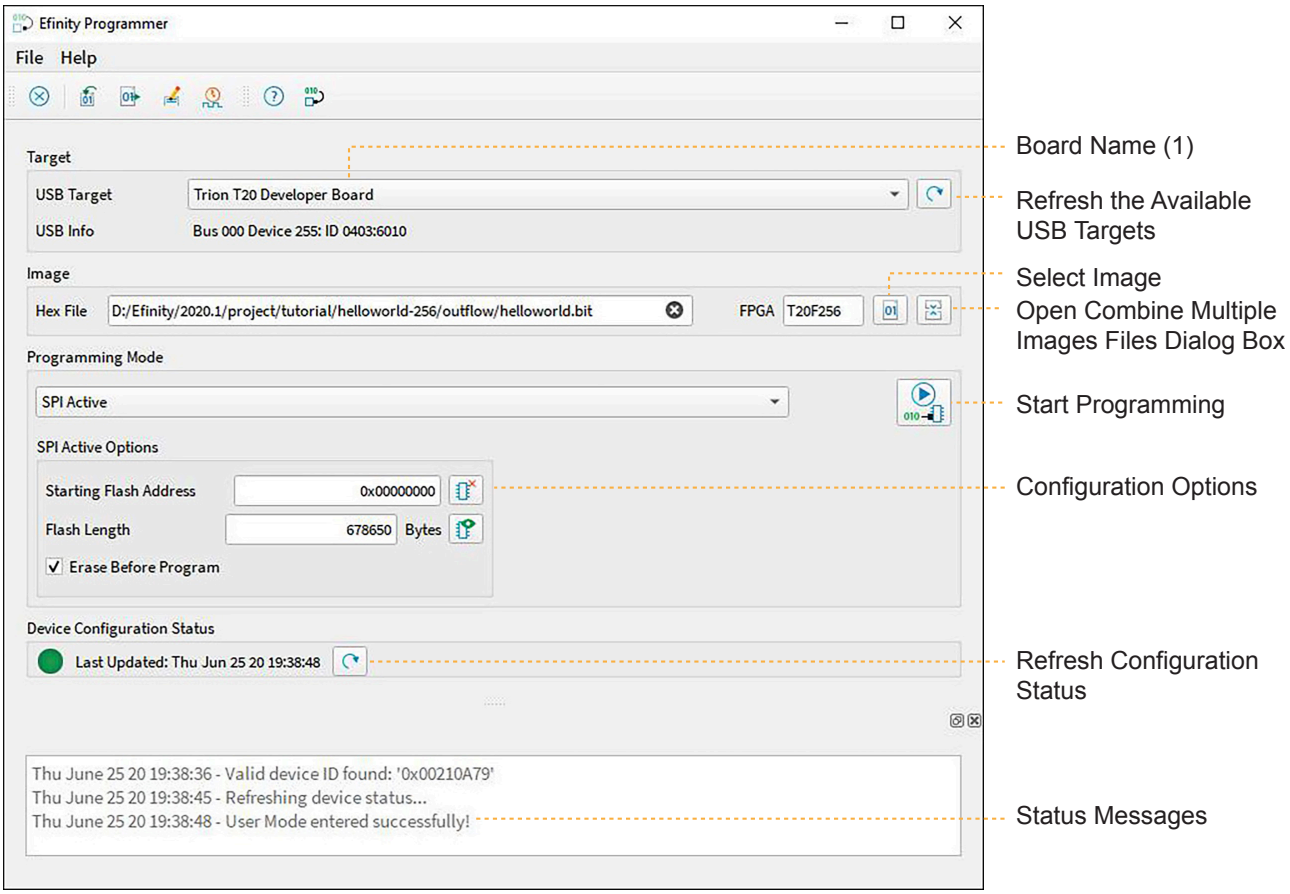
1. Choose a target.
2. Choose a bitstream file. Use a **.hex** file for SPI modes or a **.bit** file for JTAG mode.
3. Choose the programming mode and then select options.

Mode	Options
SPI Active	Starting Flash Address Flash Length Erase Before Program
SPI Passive	Clock Speed
JTAG	Device Select JTAG Clock Speed
SPI Active using JTAG Bridge	Starting Flash Address Flash Length Erase Before Program Device Select JTAG Clock Speed

4. Click the Program FPGA or Program Flash button.

The FPGA or flash device's configuration status displays in the Device Configuration Status area. Click the Refresh button to refresh the status.

Figure 1: Programmer



Note:
1. The T8 development board name displays as AVR USB HID Demo

Note: For detailed information on how to use configuration modes and set up your circuit board for configuration, refer to AN 006: Configuring Trion FPGAs.

SPI Programming

You can program Trion FPGAs using the SPI interface and a **.hex** file.

Program a Single Image

In single image programming mode, you configure one Trion® FPGA with one image.

1. Click the **Select Image File** button.
2. Browse to the **outflow** directory and choose <*project name*>**.hex**.
3. Choose **SPI Active** or **SPI Passive** configuration mode.
4. Click **Start Program**. The console displays programming messages.

Program Multiple Images

In this programming mode, you specify up to four images that can configure one FPGA. You then use the FPGA's CBSEL pins or the FPGA's internal reconfiguration interface to select which image to use. You can only configure in active mode.

1. Click the **Combine Multiple Images** button.
2. Choose **Selectable Flash Image** as the **Mode**.
3. Enter the output file name.
4. Choose the output file location. The default is the project's **outflow** directory.
5. Choose **External Flash Image** or **Internal Flash Image**

The external option uses the CBSEL pins to select the image. The internal option uses the internal reconfiguration interface to select the image.

6. Click in the table row corresponding to the position for which you want to add an image.
7. Click **Add Image**.
8. Select the image file to place in that location.
9. Click **OK**.
10. Repeat steps 6 through 9 as needed. You can add up to four images.
11. Click **Apply** to generate the combined image file.
12. Click **Close** to return to the Programmer, which displays the combined image file as the image to use for programming.
13. Click **Start Program**.

Note: For more information on programming multiple images, refer to **Example Design: Configuring a Trion Development Board with Multiple Images** on the Downloads page in the Support center.

Program a Daisy Chain

In this programming mode, you specify any number of images to configure a daisy chain of FPGAs. You can choose active or passive configuration for first FPGA; the rest are in passive mode.

1. Click the **Combine Multiple Images** button.
2. Select **Daisy Chain** as the **Mode**.
3. Enter the output file name.
4. Choose the output file location. The default is the project's **outflow** directory.
5. Click **Add Image** to add a file to the daisy chain.
6. Repeat step 5 to add as many files as you want to the chain. Use the up/down arrows to re-order the images if needed.
7. Click **Apply** to generate the combined image file.
8. Click **Close** to return to the Programmer, which displays the combined image file as the image to use for programming.
9. Click **Start Program**.

JTAG Programming

You can program Trion FPGAs using the JTAG interface and a **.bit** file.

JTAG Device IDs

Table 2: JTAG Device IDs

FPGA	Package	JTAG Device ID
T4, T8	BGA49, BGA81	0x0
T8	QFP144	0x00210A79
T13	All	0x00210A79
T20	BGA169, BGA256	0x00210A79
T20	BGA324	0x00240A79
T35	All	0x00240A79
T55, T85, T120	All	0x00220A79

Program a Single Image

In single image programming mode, you configure one Trion® FPGA with one image.

1. Click the **Select Image File** button.
2. Browse to the **outflow** directory and choose <*project name*>**.hex**.
3. Choose the **JTAG** configuration mode.
4. Click **Start Program**. The console displays programming messages.

Program Using a JTAG Chain

You can program an FPGA that is part of a JTAG chain. The chain can include Trion® FPGAs as well as other devices. You define your JTAG chain using a JTAG Chain File (**.jcf**). You import the JTAG Chain File into the Programmer to perform programming. The JTAG Chain File is an XML file that includes all of the device in the chain. For example:

```
<?xml version="1.0">

<chain>
   <device chip_num="1" id_code="0x00210a79" ir_width="4" istr_code="1100" />
   <device chip_num="2" id_code="0x00210a79" ir_width="4" istr_code="1100" />
   <device chip_num="3" id_code="0x00210a79" ir_width="4" istr_code="1100" />
</chain>
```

where:

- `chip_num` is the device order starting from position 1.
- `id_code` is the hexadecimal JEDEC device ID (all lowercase letters)
- `ir_width` is the width of the instruction register in bits
- `istr_code` is the binary IDCODE instruction

Note: For Trion® FPGAs, use 1100 as the `istr_code`.

To program using a JTAG chain:

1. Create a JTAG Chain File using a text editor.
2. Open the Programmer.

3. Choose your **USB Target** and **Image**.
4. Select **JTAG** as the **Programming Mode**.
5. Click the Import JCF toolbar button.
6. Browse to your JTAG Chain File and click **Open**.
7. Select which device you want to program in the drop-down list next to the **JTAG Programming Mode** option.
8. Click **Start Program**.

JTAG Programming with FTDI Chip Hardware

These instructions describe how to program Trion® FPGAs using the FTDI Chip FT2232H Mini Module and C232HMDDHSL-0 programming cable.

Efinix® has tested the hardware for use with Trion® FPGAs. The FT2232 Mini Module has better VCC/GND plane design which is more robust against noise compared to the C232HMDDHSL-0 programming cable. Therefore, Efinix® recommends that you use the FT2232 Mini Module to avoid JTAG programming issues.

1. Open the Efinity® software.
2. Open the Efinity® Programmer.
3. Click the Select Bitstream Image button.
4. Browse to your image and click **OK**.
5. Choose one of the following in the **USB Target** drop-down list:
   - **C232HM-DDHSL-0** for FTDI cable
   - **Dual RS232 HS** for FT2232 Mini Module
6. Choose **JTAG** from the **Programming Mode** drop-down list.
7. Click **Start Program**.

Connecting a JTAG Mini Module

The following figures show the connection diagram for the mini module and your board.

Figure 2: T4, T8, T13, T20BGA256, and T20BGA169 Connections

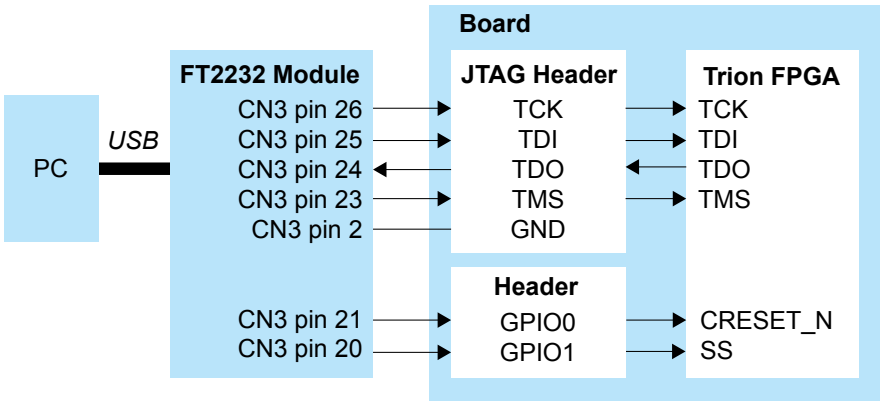
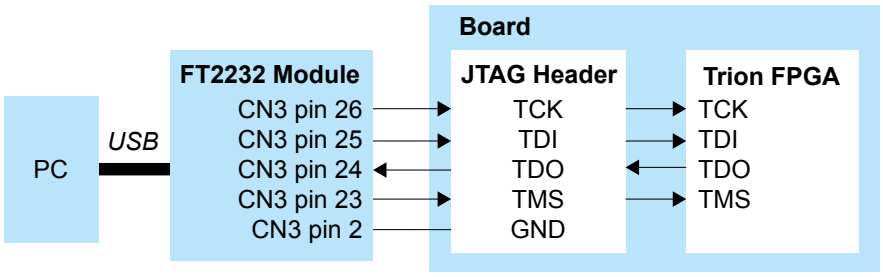


Figure 3: T20BGA324, T35, T55, T85, and T120 Connections



Connecting a JTAG Cable

The following figures show the connection diagram for the cable and your board. The colors correspond to the wire colors on the FTDI cable.

Note: For T4, T8, T13, and T20 (BGA256 and BGA169) FPGAs, this programming method uses the `CRESET_N` and `SS` pins in addition to the standard JTAG pins. However, the `CRESET_N` and `SS` pins and FTDI cable or module are only needed for JTAG programming. You can use the standard 4 JTAG pins and any cable for other JTAG functions.

Figure 4: T4, T8, T13, T20BGA256, and T20BGA169 Connections

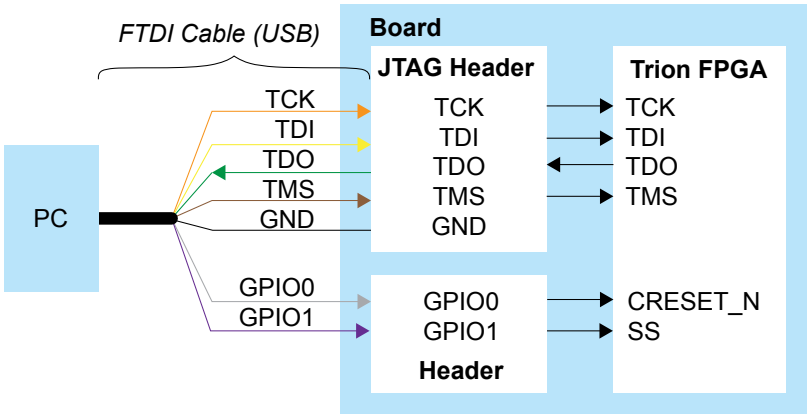
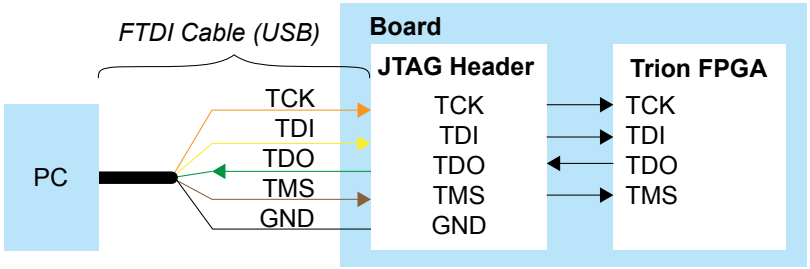


Figure 5: T20BGA324, T35, T55, T85, and T120 Connections



Where to Learn More

The Efinity® software includes documentation as PDF user guides and on-line HTML help. This documentation is provided with the software. You can also access the latest versions of PDF documentation in the Support Center:

- **Efinity Software User Guide**
- **Efinity Synthesis User Guide**
- **Efinity Timing Closure User Guide**
- **Efinity Software Installation User Guide**
- **Efinity Trion Tutorial**
- **Trion Interfaces User Guide**
- **Efinity Interface Designer Python API**
- **Efinity Software Quantum Primitives User Guide**

In addition to documentation, Efinix field application engineers have created a series of videos to help you learn about aspects of the software. You can view these videos in the Support Center.

Revision History

Table 3: Revision History

Date	Version	Description
June 2020	1.0	Initial release.