



Efinix® Trion™ FPGA Overview

The Efinix® Trion™ programmable platform, built on Efinix Quantum™ technology, delivers substantial Power-Performance-Area advantages over traditional FPGA products. Trion FPGAs feature programmable logic and a routing fabric built using Quantum technology. The fabric is wrapped with an I/O interface in a small footprint package that is required by many high-volume applications such as mobile and IoT. In addition to logic and routing, the fabric includes embedded memory blocks and multiplier blocks (or DSP blocks).

Figure 1 Trion FPGA Block Diagram

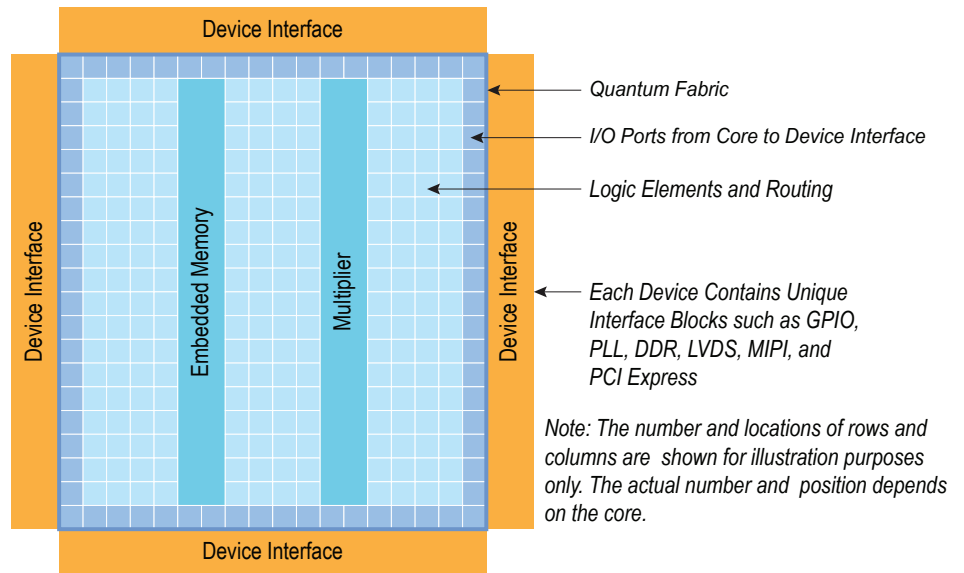


Table 1 Trion Resources and Interfaces

| Feature | T4 | T8 | T13 | T20 | T35 | T55 | T85 | T120 | T165 | T200 |
|---|--------|--------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Logic Elements (LEs) | 3,888 | 7,384 | 12,828 | 19,728 | 31,680 | 54,195 | 84,096 | 112,128 | 168,000 | 192,000 |
| Mask Programmable Memory | √ | √ | √ | √ | — | — | — | — | — | — |
| Embedded RAM bits (kb) | 77 | 123 | 727 | 1,044 | 1,475 | 2,765 | 4,055 | 5,407 | 12,364 | 14,131 |
| 18x18 Multipliers | 4 | 8 | 24 | 36 | 120 | 150 | 240 | 320 | 1,450 | 1,760 |
| PLLs | 1 | 1 | 5 | 5 | 6 | 8 | 8 | 8 | 10 | 10 |
| Maximum GPIO (1) | 59 | 59 | 213 | 213 | 200 | 388 | 388 | 388 | 415 | 415 |
| LVDS (RX + TX) | — | — | 13 | 13 | 20 | 56 | 56 | 56 | 50 | 50 |
| DDR3/LPDDR3 (800 Mbps) | — | — | — | x16 | x16 | x32 | x32 | x32 | x64 | x64 |
| MIPI 4-lane DPHY with built-in CSI-2 controller | — | — | 2 RX 2 TX | 2 RX 2 TX | 2 RX 2 TX | 3 RX 3 TX | 3 RX 3 TX | 3 RX 3 TX | 3 RX 3 TX | 3 RX 3 TX |
| PCI Express Gen 1/2 | — | — | — | — | — | — | — | — | x4 | x4 |
| Typical Standby I _{cc} (Ultra-Low Power[ULP] option) | 150 μA | 150 μA | | | | | | | | |

(1) The LVDS and DDR interface have dedicated I/O; therefore, the maximum GPIO does not include the I/O count for those interfaces. Additionally, if your design does not use LVDS, you can use its dedicated I/O as GPIO instead.

The initial phase of the Trion platform is built on SMIC's 40LL process, with a logic density range from 4K to 200K logic elements (LEs) and standard interfaces such as GPIO, PLLs, oscillators, MIPI, DDR, LVDS, PCI Express, etc. Trion FPGAs target general-purpose custom logic markets (mobile, IoT, general consumer, industrial, and medical) as well as fast-growing markets such as compute acceleration and deep learning in edge devices.

Standard I/O Interfaces

The initial rollout of Trion FPGAs supports the following interfaces:

- **MIPI**—4-lane MIPI D-PHY with a built-in (hardened) CSI-2 controller and up to 6 Gbps per PHY. Achieves low power and low cost, and provides a royalty-free, easy implementation for MIPI CSI-2.
- **LVDS**—Up to 800 Mbps LVDS data rate with up to 44.8 Gbps aggregate bandwidth.
- **DDR**—Provides DDR3/LPDDR3 support. Up to 800 Mbps DDR line rates with up to 51.2 Gbps peak bandwidth. DDR Interface includes hardened PHY and memory controller, providing low power, low cost, and easy to integrate memory interface.
- **PCI Express**—Supports Gen1/Gen2, x1, x2, x4 lanes with root complex and end point support.

Mask Programmable Memory (MPM)

T4, T8, T13, and T20 FPGAs are equipped with optional MPM. With this feature, you use on-chip MPM instead of

an external serial flash device to configure the FPGA. This option is for systems that require an ultra-small form factor and the lowest cost structure such that an external serial flash device is undesirable and/or not required at volume production. MPM is a one-time factory programmable option that requires a Non-Recurring Engineering (NRE) payment. To enable MPM, you submit your design to our factory; our Applications Engineers (AEs) convert your design into a single configuration mask to be specially fabricated.

Efinity Software Support

The Efinity® software provides a complete tool flow from RTL design to bitstream generation, including synthesis, place-and-route, and timing analysis. The software has a graphical user interface (GUI) that provides a visual way to set up projects, run the tool flow, and view results. The software also has a command-line flow and Tcl command console. The software-generated bitstream file configures Trion devices. The software supports the Verilog HDL and VHDL languages.

In Production Now

T4 and T8 FPGAs are in production now. Our Trion T8 BGA81 Development Kit, as well as T4/T8 sample boxes, are available for purchase in our online store. The Trion T20 BGA256 Development Kit is available for pre-ordering. Visit us online at www.efinixinc.com/shop to register for store access.

Table 2 Package Options

| Feature | T4 | T8 | T13 | T20 | T35 | T55 | T85 | T120 | T165 | T200 |
|-----------------------------------|----|----|-----|-----|-----|-----|-----|------|------|------|
| 49-ball FBGA (0.4 mm, 3x3 mm) | √ | √ | | | | | | | | |
| 81-ball FBGA (0.5 mm, 5x5 mm) | √ | √ | | | | | | | | |
| 144-ball FBGA (0.65 mm, 8x8 mm) | | | √ | √ | | | | | | |
| 256-ball FBGA (0.8 mm, 13x13 mm) | | | √ | √ | | | | | | |
| 324-ball FBGA (0.65 mm, 12x12 mm) | | | | √ | √ | √ | √ | | | |
| 576-ball FBGA (0.65 mm, 16x16 mm) | | | | | | √ | √ | √ | | |
| 676-ball FBGA (0.8 mm, 21x21 mm) | | | | | | √ | √ | √ | √ | √ |
| 784-ball FBGA (0.8 mm, 23x23 mm) | | | | | | | | | √ | √ |