AN 054: Performing Simulation with IBIS Models

AN054-v1.1
May 2023
www.efinixinc.com

Contents

Introduction

Designing high-speed systems have become increasingly important. Systems like high-definition vision, high-performance computing, high-bandwidth accelerator cards, and high-speed network applications require faster and more efficient data transmissions. However, signal integrity issues are becoming more significant on high-speed systems. Minimizing signal distortion in your design reduces the need for redesigning and rework, resulting in a shorter time-to-market product, thus creating a cost-efficient project. Hence, performing signal integrity simulation before beginning any board development work is important.

Efinix provides I/O Buffer Information Specification (IBIS) models for signal integrity simulation at the system board level. IBIS models are behavioral and describe the characteristics of the digital input/output (I/O) buffers. IBIS models are formatted in ASCII format that contain V-I (voltage versus current) and V-T (voltage versus time) tables to describe the buffer's behavior. With the IBIS models, the designer can detect any signal integrity issues such as reflection, crosstalk, ground and power bounce, and ringing. Using the IBIS models for signal integrity simulation is relatively simple as the designer has a variety of EDA tools at his disposal.

Note: Efinix® provides FREE licences for the Efinity® software. Alternatively, when you buy a development kit, you also get a software license and one year of upgrades. After the first year, you can request a free maintenance renewal. The Efinity software is available for download from the **Support Center**. To get your free license, create an account, login, and then go to the Efinity page to request your license.

Comparing IBIS to SPICE Models

IBIS models have several advantages compared to SPICE models. The following table compares the two models.

Table 1: SPICE and IBIS Model Comparison

Item	SPICE Models	IBIS Models
Circuit Information	Contains confidential information that is proprietary on internal circuits and processes (e.g. transistor models, etc.).	Contains behavioral information regarding buffers only. Does not disclose design information.
Complexity	High	Medium
Accuracy	High	Medium
Simulation Period	Long	Short

File Structure of IBIS Models

The file have 3 sections:

1. File header and file end information
2. Component description
3. Buffer modeling

A single file can contain more than one component to describe the buffer behavior. Thus, sections 2 and 3 can be repeated in one file.

Table 2: Keywords for File Header and File End Information

Keyword	Description
[IBIS ver]	Show the version number of **.ibs** file. It is the first keyword in the first line of any **.ibs** file.
[Comment Char]	State a new comment to replace the default character ("|") if needed for all types of file. The new comment character to be expressed must be followed by an underscore character and the letters **char** (**|_char**). Example: **[Comment Char] |_char**.
[File name]	File names shall have a stem of no more than (<) sixty (60) characters and no less than one character followed by a period ("."), followed by a **.ibs** file name extension. The file name shall be the actual name of the file.
[File Rev]	Tracks the file revision.
[Date]	The date of the file creation. Limited to a maximum of 40 characters. Example: February 28, 2023.
[Source]	The source from which the information originates.
[Notes]	Additonal information related to the file.
[Disclaimer]	A statement notice from the manufacturer repudiating a claim.
[Copyright]	A statement notice of exclusive and assignable legal right to the manufacturer.
[End]	Marks the end of the file.

Table 3: Keywords for Component Description

Keyword	Description
[Component]	Marks the beginning of the IBIS description of the integrated circuit named after the keyword. If the **.ibs** file contains data for more than one component, each section must begin with a new [Component] keyword. The length of the component must not exceed 40 characters. Blank characters (spaces) are allowed but are not recommended.
[Manufacturer]	Shows the name of the component manufacturer. The length of the manufacturer's name must not exceed 40 characters and blank characters (spaces) are allowed (e.g., Efinix Inc.). The manufacturer's name must be consistent in all **.ibs** files.
[Package]	Simple RLC model to represent the parasitic element in the package. The values are provided in minimum, typical, and maximum.
[Pin]	The [Model]s and [Model Selector]s are associated with the package pin names, signal names, and RLC values. The RLC values are specific for each pin and the values overwrite the default RLC values defined in [Package].
[Diff Pin]	Specify the differential pins with the differential receiver threshold and output delays. The values for output delays are provided in minimum, typical, and maximum.
[Series Pin Mapping]	Associate two pins with a model in series. Efinix uses this keyword to specify the internal termination model between the two LVDS pins.
[Model Selector]	Option to select the list of [Model]s for the programmable I/O buffer.

Table 4: Keywords for Buffer Modeling

Keyword	Description
[Model]	The name of the modeled buffer and marks the start of the description of the buffer's behavior. Also, this keyword has these few sub-parameters: Model_type: The type of buffer (e.g. Input, Output, I/O). Polarity: Polarity of buffer's output from input (e.g., Non-Inverting, Inverting). Enable: Polarity of buffer's output enables (e.g., Active-High, Active-Low). V_{inl}, V_{inh}: Input voltage threshold low and high. C-comp: Die capacitance without including the parasitic capacitance on the package. C_comp_pullup, C_comp_pulldown, C_comp_power_clamp and C_comp_gnd_clamp are the die capacitance between the I/O pad and the corresponding supply references. V_{meas}: Reference voltage level that the manufacturer uses for the model. C_{ref}, R_{ref}, V_{ref}: Load test that the manufacturer uses when specifying the propagation delay and/or output switching time of the model.
[Model Spec]	Provides the minimum, typical, and maximum values for V_{inl}, V_{inh}, C_{ref}, R_{ref}, V_{ref}, and V_{meas} sub-parameters.
[Add Submodel]	Specify the electrical characteristic of the [Submodel] to be added to a model. Non-Driving mode is to add characteristics when the model is receiving or in high impedance.
[Temperature Range]	Specify the temperature for the corresponding I-V tables and ramp rates.
[Voltage Range]	Specify the power supply voltage (VCC) for the model.
[Pullup Reference]	Specify alternate voltage rail for the [Pullup] I-V tables.
[Pulldown Reference]	Specify alternate voltage rail for the [Pulldown] I-V tables.
[POWER Clamp Reference]	Specify alternate voltage rail for the [POWER Clamp] I-V tables.
[GND Clamp Reference]	Specify alternate voltage rail for the [GND Clamp] I-V tables.

Keyword	Description
[Pulldown]	I-V tables to describe the behavior of the low-driven output. The tables are a reference to the GND (or [Pulldown Reference]).
[Pullup]	I-V tables to describe the behavior of the high-driven output. The tables are a reference to the VCC (or [Pullup Reference]).
[GND Clamp]	I-V tables to describe the behavior of the high-impedance input or output. The tables are a reference to the GND (or [Pulldown Clamp Reference]).
[POWER Clamp]	I-V tables to describe the behavior of the high-impedance input or output. The tables are a reference to the VCC (or [Pullup Clamp Reference]).
[ISSO PU](1)	I-V tables to describe the effective current for the pull-up structure, with respect to the voltage variation of the VCC (or [Pullup Reference]).
[ISSO PD](1)	I-V tables to describe the effective current for the pull-down structure, with respect to the voltage variation of the GND (or [Pulldown Reference]).
[Ramp]	Define the ramp rate with the effects of the C_comp or C_comp_* parameters. dV/dt_r is for the rising edges while dV/dt_f is for the falling edges.
[Rising Waveform]	V-T tables to describe the shape of an output waveform for the transition from low to high.
[Falling Waveform]	V-T tables to describe the shape of an output waveform for the transition from high to low.
[Composite Current](1)	V-T tables to describe the current for the identical time points in [Rising Waveform] and [Falling Waveform].
[Submodel]	Enable the extra buffer behaviors under certain conditions. Dynamic_clamp type activates the additional clamps when the buffer is in receive mode.

Learn more: For more information regarding the structure of IBIS models, refer to https://ibis.org/

(1) Only available for models with IBIS version 5.1 and later. The models that do not have this keyword comply with versions lower than 5.1.

I/O Features to Improve Signal Integrity

Efinix FPGAs provide several I/O features to improve signal integrity on the system board level design. Efinix highly recommends running an IBIS simulation to determine the optimum setting for the following I/O features.

These I/O features can be set and controlled using the Efinity's Interface Designer. To learn more on the Interface Designer, you may refer to **Trion Interfaces User Guide** or **Titanium Interfaces User Guide**.

Variable Drive Strength

Simulation using an IBIS model is important to find a suitable drive strength for a project. As the drive strength increases, the rise time and fall time also increase. This variable drive strength is used to drive the signals of many components or high-load capacitance components. Furthermore, it can overcome degrading signals caused by a higher trace resistance and capacitance.

Important: The highest drive strength is not necessarily the best solution because increasing the current introduces excessive overshoot and undershoot. Additionally, higher variable drive strength translates to higher power consumption.

Trion Drive Strength

All Trion® FPGA single-ended drivers support variable drive strength. The following tables show the drive strength settings available for GPIO and LVDS configured as GPIO.

Table 5: Trion GPIO Drive Strength Support

I/O Standard	Drive Strength
3.3 V LVCMOS	1, 2, 3, 4
2.5 V LVCMOS	1, 2, 3, 4
1.8 V LVCMOS	1, 2, 3, 4
3.3 V LVTTL	1, 2, 3, 4

Table 6: Trion LVDS Configured as GPIO Drive Strength Support

Not available for Trion T4, T8, T13, and T20 (WLCSP80, QFP144, BGA169, and BGA256)

I/O Standard	Drive Strength
3.3 V LVCMOS	1, 2, 3, 4
2.5 V LVCMOS	1, 2, 3, 4
1.8 V LVCMOS	1, 2, 3, 4
3.3 V LVTTL	1, 2, 3, 4

Titanium Drive Strength

All Titanium FPGA single-ended drivers support variable drive strength. The following tables show the drive strength settings available for HVIO and HSIO configured as GPIO.

Table 7: Titanium HVIO Drive Strength Support

I/O Standard	Drive Strength (mA)
3.3 V LVCMOS	2, 4, 6, 8
3.0 V LVCMOS	2, 4, 6, 8
2.5 V LVCMOS	4, 8, 12, 16
1.8 V LVCMOS	4, 8, 12, 16
3.3 V LVTTL	4, 8, 12, 16
3.0 V LVTTL	4, 8, 12, 16

Table 8: Titanium HSIO Configured as GPIO Drive Strength Support

I/O Standard	Drive Strength (mA)
1.8 V LVCMOS	4, 8, 12, 16
1.5 V LVCMOS	4, 8, 12, 16
1.2 V LVCMOS	2, 4, 8, 12
1.8 V SSTL	4, 8, 10, 12
1.5 V SSTL	4, 8, 10, 12
1.2 V SSTL	4, 8, 10, 12
1.8 V HSTL	4, 8, 10, 12
1.5 V HSTL	4, 8, 10, 12
1.2 V HSTL	4, 8, 10, 12

Slew Rate Control

The slew rate control feature can also help to reduce signal integrity issues at the system board level. The slow slew rate signal can reduce undershoot, overshoot, and ringing. It limits the output voltage change rate, effectively filtering out fast-changing transients. Hence, the IBIS simulation allows you to identify the pin that can be set to slow slew rate control (slew rate control disabled) to improve the board's overall performance.

Important: Because a slow slew rate reduces the rise time and fall time, it is not suitable for high-speed system requirements. It is more suitable for applications that require slow I/O clocks such as UART and I^2C.

Trion Slew Rate Control

The following tables show the supported slew rate control for Trion FPGAs.

Table 9: Trion Slew Rate Control Support

I/O	Slew Rate Control
GPIO	✓
LVDS configured as GPIO	✓ (2)

Titanium Slew Rate Control

The following tables show the supported slew rate control for Titanium FPGAs.

Table 10: Titanium Slew Rate Control Support

I/O	Slew Rate Control
HVIO	–
HSIO configured as GPIO	✓

(2) Only T20 (BGA324 and BGA400), T35, T55, T85, and T120 FPGAs support slew rate control on LVDS configured as GPIO.

Programmable Pre-emphasis

On Titanium FPGAs, the HSIO pins that are configured as a true differential driver have a feature to set the pre-emphasis. Pre-emphasis improves signal quality by counteracting the effects of channel loss. It does so by momentarily increasing the strength of high-frequency signals. Hence, you can use IBIS simulation to find the optimal amount of pre-emphasis needed for each true differential driver.

Important: Overuse of pre-emphasis can lead to over-modulation and degradation of the signal quality, while a lower level of pre-emphasis does not provide enough enhancement to overcome the effects of channel loss.

Titanium's HSIO pins only support programmable pre-emphasis for true differential drivers such as LVDS, Sub-LVDS, Bus-LVDS, RSDS, Mini LVDS, and SLVS. The following table shows the programmable pre-emphasis available for HSIO.

Table 11: Supported Pre-emphasis for HSIO Configured as True Differential I/O

I/O Standard	Programmable Pre-emphasis
LVDS	Low, Medium Low, Medium High, and High
Sub-LVDS	Low, Medium Low, Medium High, and High
Bus-LVDS	Low, Medium Low, Medium High, and High
RSDS	Low, Medium Low, Medium High, and High
Mini LVDS	Low, Medium Low, Medium High, and High
SLVS	Low, Medium Low, Medium High, and High

Note: Trion does not support programmable pre-emphasis.

DDR Controller Settings

Trion DDR Controller

On Trion FPGAs, the dedicated output DDR pins have both programmable input and output terminations. The programmable output termination controls the drive strength of a signal. To achieve a high-speed data rate, a higher drive strength is required to obtain a low rising and falling time. Also, similar drive strength is required to overcome the effect of degrading signals caused by a higher trace resistance and capacitance on the board. Relatively, the programmable input termination is used to reduce the effect of the signal reflection. With the IBIS simulation, you can identify the most suitable values for the input and output terminations.

Important:

- Excessive use of drive strength increases power consumption and crosstalk interference.
- Excessive use of on-die termination will cause the signal to become over-damped, thus increasing the rise time and fall time which affects the quality of the signal. Therefore, due to this reason, it is important to run the IBIS simulation for the proper DDR controller setting.

The Trion DDR controller supports programmable input and output termination. The following table show the input and output termination available in the DDR controller.

Table 12: Trion DDR Controller Supported Termination

DDR DRAM Interface	Programmable Termination (Ω)	
	Input Termination	Output Termination
DDR3	20, 30, 40, 60, 120	34.3, 40
LPDDR2	120, OFF	34.3, 40, 48, 60, 80, 120
LPDDR3	120, 240, OFF	34.3, 40, 48, 60, 80

Titanium DDR Controller

On Titanium FPGAs, the dedicated DDR pins have a variable pull-up/pull-down drive strength and a pull-up/pull-down on-die termination. The function of a pull-up/pull-down drive strength is to improve the signal quality of a high-speed signal. On the system board level, a high drive strength is required to overcome the effect of signal loss caused by a higher trace resistance and capacitance. Another advantage is that the pull-up/pull-down on-die termination can help reduce signal reflection.

Titanium DDR controller supports variable pull-up/pull-down drive strength and pull-up/pull-down on-die termination. The following table shows the pull-up/pull-down drive strength and pull-up/pull-down on-die termination available in the DDR controller.

Important:

- Excessive use of drive strength increases power consumption and crosstalk interference.
- Excessive use of on-die termination will cause the signal to become over-damped, thus increasing the rise time and fall time which affects the quality of the signal. Therefore, due to this reason, it is important to run the IBIS simulation for the proper DDR controller setting.

Table 13: Titanium DDR Controller Supported Termination

DDR DRAM Interface	Programmable Termination (Ω)			
	DQ Pull-down Drive Strength	DQ Pull-down ODT	DQ Pull-up Drive Strength	DQ Pull-up ODT
LPDDR4	34.3, 40, 48, 60, 80, 120, 240	34.3, 40, 48, 60, 80, 120, 240, Hi-Z	34.3, 40, 48, 60, 80, 120, 240	34.3, 40, 48, 60, 80, 120, 240, Hi-Z
LPDDR4x	34.3, 40, 48, 60, 80, 120, 240	34.3, 40, 48, 60, 80, 120, 240, Hi-Z	34.3, 40, 48, 60, 80, 120, 240	34.3, 40, 48, 60, 80, 120, 240, Hi-Z

Revision History

Table 14: Revision History

Date	Version	Description
May 2023	1.1	Update note in Introduction.
March 2023	1.0	Initial release.