Trion® T120 BGA576 Development Kit User Guide

T120F576-DK-UG-v2.3
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Contents

Introduction

Thank you for choosing the Trion® T120 BGA576 Development Kit (part number: T120F576C-DK), which allows you to explore the features of the T120 FPGA with a MIPI CSI-2 interface and DDR controller. The kit includes 3 daughter cards that let you connect MIPI cameras, a Raspberry Pi V2 camera module, and extend the GPIO, plus a Raspberry Pi camera module and accessories.

Warning: The board can be damaged without proper anti-static handling.

What's in the Box?

The Trion® T120 BGA576 Development Kit includes:

- Trion® T120 BGA576 Development Board preloaded with a demonstration design
- MIPI and LVDS Expansion Daughter Card
- 2 Raspberry Pi Camera Connector Daughter Cards
- Raspberry Pi V2 camera module with 15-pin FFC/FPC cable
- 10 standoffs, 10 screws, and 6 nuts for development board and daughter cards
- 3 foot USB cable (type A to micro type B)
- Universal AC to DC power adapter

Important: This kit includes a power cable with a type A plug (U.S. style). You need an adapter to use this cable with other socket types.

Register Your Kit

When you purchase an Efinix development kit, you also receive a license for the Efinity® software plus one year of software upgrades and patches. After the first year you can request a free maintenance renewal. The Efinity® software is available for download from the Support Center.

To download the software, first register at our Support Center (https://www.efinixinc.com/register) and then register your development kit.

Download the Efinity® Software

To develop your own designs for the T120 device on the board, you must install the Efinity® software. You can obtain the software from the Support Center.

The Efinity® software includes tools to program the device on the board. Refer to the Efinity® Software User Guide for information about how to program the device.

Learn more: Efinity® documentation is installed with the software (see **Help** > **Documentation**) and is also available in the Support Center under Documentation.

Installing the Linux USB Driver

The following instructions explain how to install a USB driver for Linux operating systems.

1. Disconnect your board from your computer.
2. In a terminal, use these commands:

```
> sudo <installation directory>/bin/install_usb_driver.sh
> sudo udevadm control --reload-rules
```

Note: If your board was connected to your computer before you executed these commands, you need to disconnect and re-connect it.

Installing the Windows USB Drivers

Note: If you have another Efinix board and are using the Trion® T120 BGA576 Development Board, you must manage drivers accordingly. Refer to **AN 050: Managing Windows Drivers** for more information.

On Windows, you use software from Zadig to install drivers. Download the Zadig software (version 2.7 or later) from zadig.akeo.ie. (You do not need to install it; simply run the downloaded executable.)

To install the driver:

1. Connect the board to your computer with the appropriate cable and power it up.
2. Run the Zadig software.

   Note: To ensure that the USB driver is persistent across user sessions, run the Zadig software as administrator.

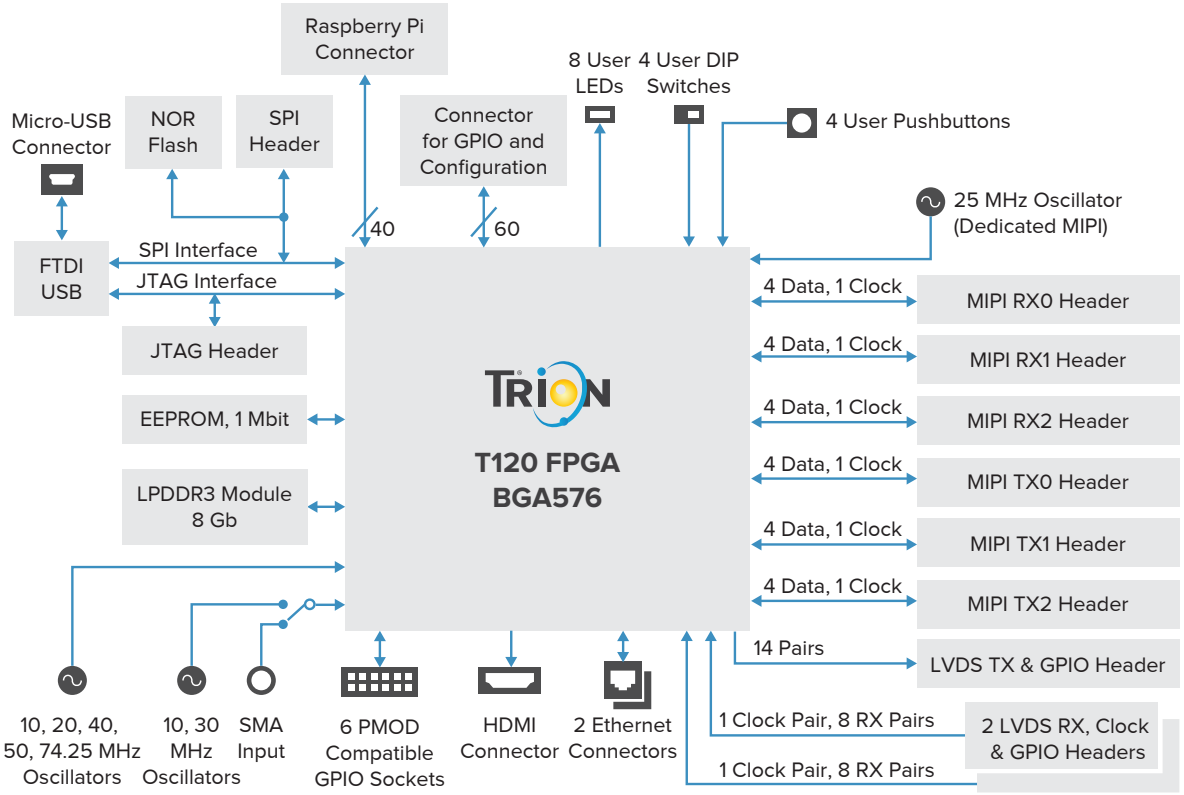
3. Choose **Options > List All Devices**.
4. Repeat the following steps for each interface. The interface names end with *(Interface N)*, where *N* is the channel number.
   - Select **libusb-win32** in the **Driver** drop-down list.
   - Click **Replace Driver**.
5. Close the Zadig software.

Note: This section describes how to install the libusb-win32 driver for each interface separately. If you have previously installed a composite driver or installed using libusbK drivers, you do not need to update or reinstall the driver. They should continue to work correctly.

Board Functional Description

The Trion® T120 BGA576 Development Board contains a variety of components to help you build designs for the Trion® T120 device.

Figure 1: Trion® T120 BGA576 Development Board Block Diagram



Features

- Efinix® T120F576I4 device in an 576-ball FineLine BGA package with MIPI CSI-2 interface and DDR DRAM controller
- LPDDR3 256 Mbits x 32 bits memory supporting up to 8 Gb
- HDMI 1080p transmitter for video output
- Triple-speed Ethernet PHY
- 1 Mbit EEPROM
- 128 Mbit SPI NOR flash memory
- FTDI FT2232H dual-channel chipset with USB controller
- Micro-USB type B receptacle
- Designed to accommodate multiple daughter cards:
  - Six MIPI high-speed connectors to attach Efinix camera connector daughter cards
  - Three LVDS high-speed headers to attach the Efinix GPIO daughter card
- 60-pin high-speed connector for user I/O
- 40-pin socket compatible with Raspberry Pi computer
- Six 12-pin PMOD-compatible GPIO sockets
- User LEDs and switches:
  - 8 LEDs on T120F576I4 bank 4C
  - 4 pushbutton switches (connected to bank 4C I/O pins)
  - 4 DIP switches (connected to bank 4C I/O pins)
- 10, 20, 25, 30, 40, 50, and 74.25 MHz oscillators for T120F576I4 PLL input
- Optional 3.3 V external clock source available through SMA input to drive the T120F576I4 PLL input or clock input pin
- Power:
  - Power source: 12 V, 5 A power supply
  - On-board regulator sources: 1.2 V (5 A), 1.25 V (0.5 A), 3.3 V (5 A), 5 V (0.5 A), 1.8 (2 A), 2.5V (2 A), and 2.8 V (0.5 A)
  - On-board regulator for LPDDR3 memory
  - Fixed 3.3 V VCCIO for T120F576I4 I/O banks 1A, 1B, 1C, 1D, 1E, 1F, 1G, 2A, 2B, 2C, 2D, 2E, 3D, 4B, 4C, 4D, 4E, and 4F
  - User selectable voltages from 1.8 V, 2.5 V, and 3.3 V for bank 2F and 4A
  - Optional header for camera power supply with power on sequence
  - Optional header for daughter card power supply
- Power good and T120F576I4 configuration done LEDs

Overview

The board features the Efinix® T120 programmable device in a 576-ball FBGA package, which is fabricated using Efinix® Quantum® technology. The Quantum®-accelerated programmable logic and routing fabric is wrapped with an I/O interface in a small footprint package. T120 devices also include embedded memory blocks and multiplier blocks (or DSP blocks). You create designs for the T120 device in the Efinity® software, and then download the resulting configuration bitstream to the board using the USB connection.

Learn more: For more information on T120 FPGAs, refer to the T120 Data Sheet.

Figure 2: Trion® T120 BGA576 Development Board Components (Top)

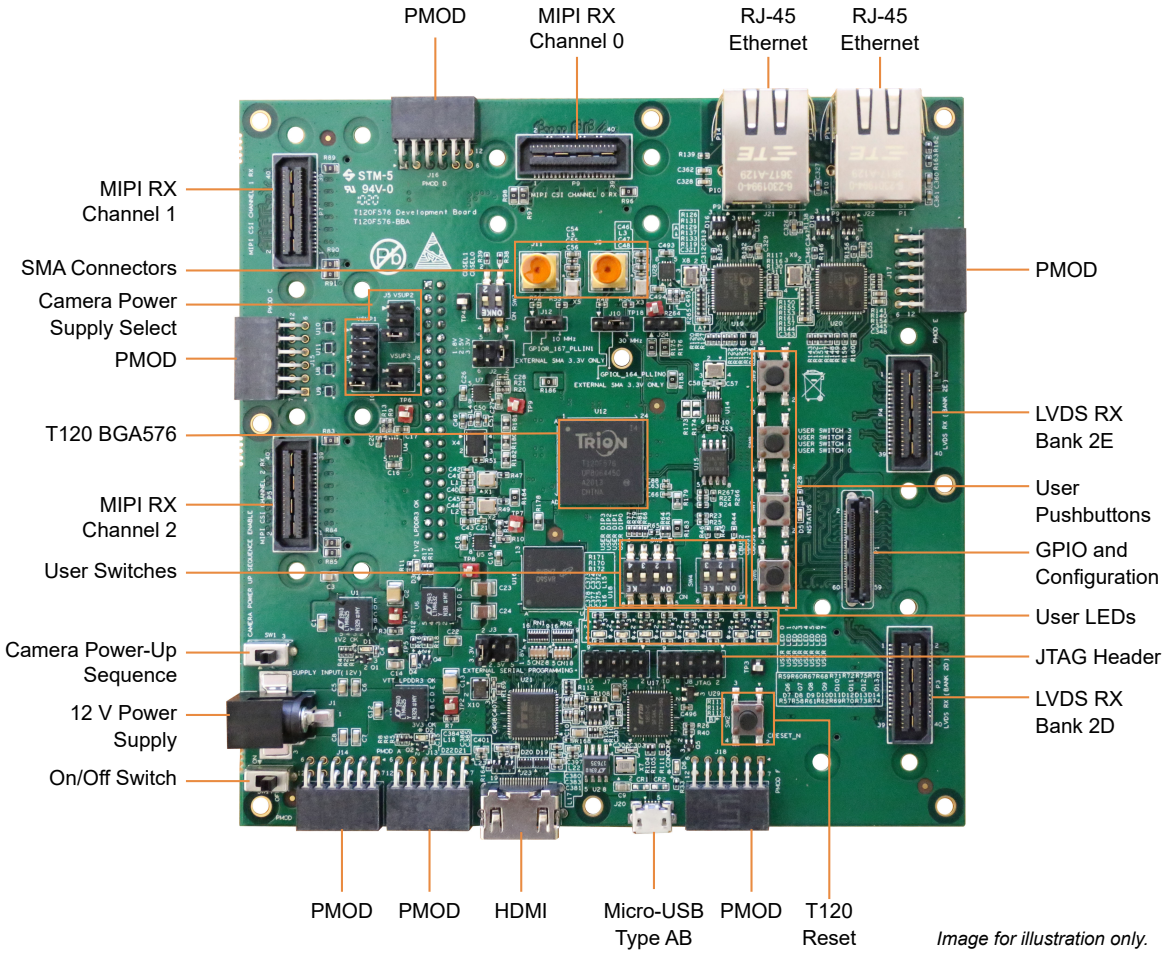
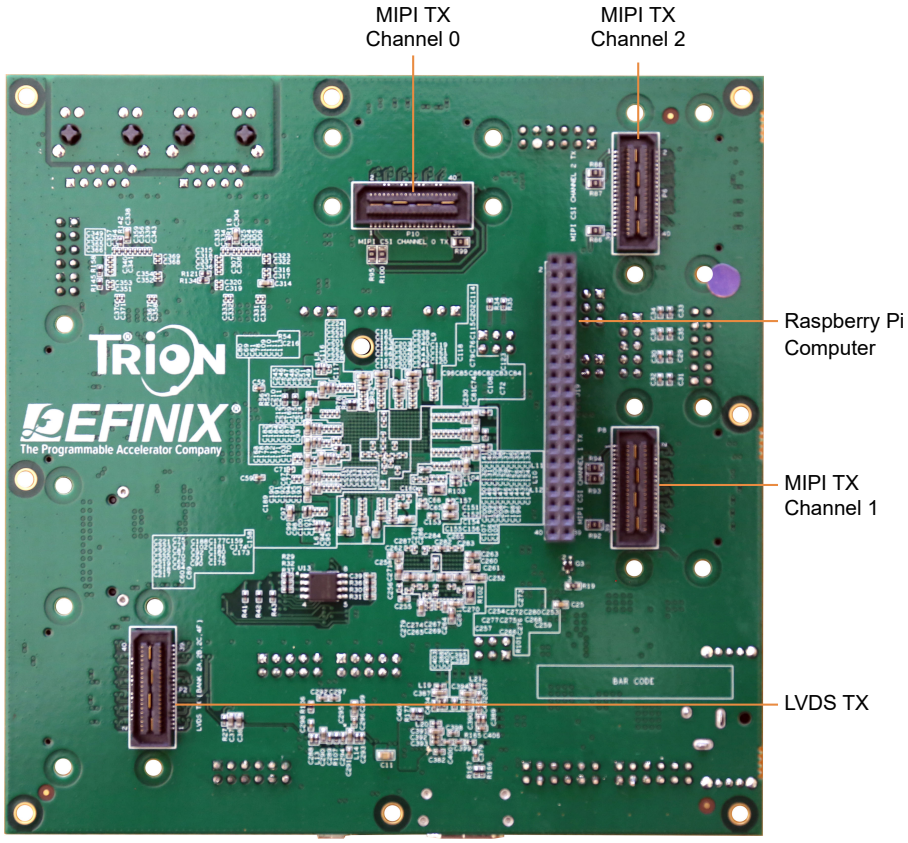


Figure 3: Trion® T120 BGA576 Development Board Components (Bottom)



The Trion® T120 BGA576 Development Board provides six 0.8 mm high-speed ground plane sockets for the MIPI CSI-2 interface and three 0.8 mm high-speed ground plane sockets for the LVDS transmitters and receivers. It has six sockets to connect PMOD-compatible peripherals. Additionally, it has a 0.5 mm high-speed connector for additional I/O pins and one 40-pin header for connecting to a Raspberry Pi computer.

The FTDI FT2232H module has two channels to support SPI (FTDI interface 0) and JTAG (FTDI interface 1) configuration. It receives the T120 configuration bitstream from a USB host and writes to the on-board SPI NOR flash memory. After a reset in SPI passive mode, the FTDI controller can also write the configuration bitstream directly to the FPGA. Additionally, it supports direct JTAG programming mode in which it writes the configuration bitstream directly to the FPGA through the JTAG interface.

Learn more: Refer to **AN 006 Configuring Trion FPGAs** for more information.

The SPI NOR flash memory stores the configuration bitstream it receives from the FTDI FT2232H module. The T120 device accesses this configuration bitstream when it is in active configuration mode (default).

The board's main power supply is the 12 V DC input. Use the included power supply to provide the board with power through the 12 V input jack. The recommended power input is a 12 V (5 A minimum) DC power source.

Note: Although the Trion® T120 BGA576 Development Board has a different power-up sequence, you should follow the power-up sequence in the **T120 Data Sheet** when designing your own board. For improved reliability, Efinix® recommends that you use supervisor IC at `CRESET_N` explained in **AN 006 Configuring Trion FPGAs**.

The board regulates down the 12 V DC input using on-board switching regulators to provide the necessary voltages for the T120 device, LPDDR3, Ethernet PHY, HDMI transmitter, PMOD module, SPI flash memory, SDRAM and on-board oscillator.

Learn more: Refer to the Trion T120 BGA576 Development Board Schematics and BOM for more information about the components used in the Trion® T120 BGA576 Development Board.

Power On

To turn on the development board, turn on switch SW17. Upon power-up, the 12 V DC power is input to the on-board regulators through 12 V input jack (CON1) to generate the required 3.3 V, 2.8 V, 2.5 V, 1.8 V, 1.25 V, and 1.2 V for components on the board. When these voltages are up and stable, on-board LEDs (D1, D2, D3, and D4) illuminate, giving you a visual confirmation that the power supplies on the board are up and stable.

Note: The micro-USB cable cannot power the board. You must use the provided 12 V DC power adapter cable.

Reset

The T120F576I4 device is typically brought out of reset with the CRESET signal. Upon power up, the T120F576I4 device is held in reset until CRESET toggles high-low-high.

Note: You can manually assert the high-low-high transition with pushbutton switch SW2.

CRESET has a pull-up resistor. When you press SW2, the board drives CRESET low; when you release SW2, the board drives CRESET high. Thus, a single press of SW2 provides the required high-low-high transition.

After toggling CRESET, the T120F576I4 device goes into configuration mode and reads the device configuration bitstream from the flash memory. When configuration completes successfully, the device drives the CDONE signal high. CDONE is connected to a green LED (D6), which turns on when the T120F576I4 device enters user mode.

Clock Sources

Seven on-board oscillators (10, 20, 25, 30, 40, 50, and 74.25 MHz), are available to drive the T120F576I4 PLL input pin and clock input. The T120F576I4provides two additional external clock input through the SMA inputs (J9 and J11). Set the jumper J10 and J12 shown in Header J10 and J12 (Clock and PLL Input Select) on page 21 to select the SMA inputs.

Table 1: Oscillator and Clock Generator Sources

Clock Source	PLL Input Pin	PLL
10 MHz oscillator or 3.3 V SMA input	GPIOR_167_PLLIN1	PLL_TR1
10 MHz oscillator	GPIOL_15_PLLIN0	PLL_BL0
20 MHz oscillator	GPIOR_187_PLLIN1	PLL_BR1
25 MHz oscillator	GPIOR_169_MREFCLK	Dedicated MIPI clock source
30 MHz oscillator or 3.3 V SMA input	GPIOL_164_PLLIN0	PLL_TL0
40 MHz oscillator	GPIOL_19_PLLIN1	PLL_BL0
50 MHz oscillator	GPIOR_186_PLLIN0	PLL_BR0
74.25 MHz oscillator	GPIOR_166_PLLIN0	PLL_TR0

Configuration

The Trion® T120 BGA576 Development Board has two DIP switches to set the configuration mode for the T120 FPGA.

Learn more: For more details on configuration, refer to AN 006 Configuring Trion FPGAs.

Table 2: Configuration Pins

Reference	Configuration Pin	Notes
SW3	CBSEL	Choose which image to load from the SPI flash device.
SW4	CBUS	Select configuration bus width for SPI active or passive configuration.

EEPROM

The Trion® T120 BGA576 Development Board has a 1 Mbit (131,072 x 8) EEPROM to store user data (part number AT24CM01-SHD-T). You can program the EEPROM through the I^2C bus at the preset address 0x50.

Table 3: EEPROM Pins

Signal Name	FPGA Pin
EEPROM_SCL	GPIOL_04
EEPROM_SDA	GPIOL_05

Camera Power-Up Circuit

The Trion® T120 BGA576 Development Board includes a basic power up sequence circuit for MIPI CSI-2 cameras. You control the circuit using SW1. When SW1 is on, the power up goes from VSUP1 to VSUP2 to VSUP3 in sequence.

Note: To apply power in sequence, set the jumpers for J4, J5 and J6 as described in Header J4, J5, and J6 (Power Select).

Headers

The board contains a variety of headers to provide power, inputs, and outputs, and to communicate with external devices or boards.

Table 4: Trion® T120 BGA576 Development Board Headers

Reference Designator	Description
P1	60-pin high-speed connector for GPIO and configuration
P2	40-pin high-speed connector for LVDS receiver (TX) and GPIO
P3	40-pin high-speed connector for LVDS transmitter (RX) and GPIO
P4	40-pin high-speed connector for LVDS transmitter (RX) and GPIO
P5	40-pin connector for MIPI CSI-2 channel 2 receiver, 1.8, 2.5, 3.3 V GPIO, and power supply
P6	40-pin connector for MIPI CSI-2 channel 2 transmitter, 1.8, 2.5, 3.3 V GPIO, and power supply
P7	40-pin connector for MIPI CSI-2 channel 1 receiver, 1.8, 2.5, 3.3 V GPIO, and power supply
P8	40-pin connector for MIPI CSI-2 channel 1 transmitter, 1.8, 2.5, 3.3 V GPIO, and power supply
P9	40-pin connector for MIPI CSI-2 channel 0 receiver, 1.8, 2.5, 3.3 V GPIO, and power supply
P10	40-pin connector for MIPI CSI-2 channel 0 transmitter, 1.8, 2.5, 3.3 V GPIO, and power supply
J1	12 V DC power supply input jack
J2	User selectable VCCIO for bank 2F
J3	User selectable VCCIO for bank 4A
J4	User selectable supply with or without power up sequence for MIPI CSI-2 camera (5.0, 3.3, and 2.8 V)
J5	User selectable supply with or without power up sequence for MIPI CSI-2 camera (3.3 and 1.8 V)
J6	User selectable supply with or without power up sequence for MIPI CSI-2 camera (1.2 V)
J7	External SPI NOR flash programming header
J8	JTAG header
J9	SMA connector for external 3.3 V clock source input
J10	3-pin header to select whether to use the on-board 30 MHz oscillator or SMA input from external clock source
J11	SMA connector for external 3.3 V clock source input
J12	3-pin header to select whether to use the on-board 10 MHz oscillator or SMA input from external clock source
J13 - J18	12-pin PMOD socket
J19	40-pin connector compatible with Raspberry Pi computer
J20	Micro-USB Type-AB receptacle
J21, J22	RJ-45 triple-speed Ethernet connector
J23	HDMI output connector
J24	I2C header to access configurable cloak generator(1)

(1) Only applicable to Rev. BBA board.

Header P1 (GPIO and Configuration)

P1 is a high-speed connector (part number is LSHM-130-02.5-L-DV-A-S-TR) that you can connect to an external board. Through it, the external board can configure the T120 FPGA and control the GPIO. P1 connects to GPIO pins in banks 1A, 1B, 1C, 1G, 2C, 3D, 4A and TR_CORNER. These pins are fixed to 3.3 V. P1 also provides 12 V DC power directly from the DC adapter. To connect to P1, use part number: LSHM-130-02.5-L-DV-A-S-TR.

Table 5: P1 Pin Assignments

Pin Number	Pin Name	Pin Number	Pin Name
1	12V	2	12V
3	GPIOL_01_CCK	4	GPIOL_11_CBUS0
5	GPIOL_00_SS_N	6	GPIOL_12_CBUS1
7	GPIOL_08_CDI0	8	GPIOL_13_CBUS2
9	GPIOL_09_CDI1	10	CDONE
11	GPIOL_14_CDI2	12	GPIOL_150_NSTATUS
13	GPIOL_16_CDI3	14	CRESET_N
15	GPIOL_18_CDI4	16	GPIOR_172_CTRL13
17	GPIOL_20_CDI5	18	GPIOR_173_CTRL12
19	GPIOL_22_CDI6	20	GPIOR_174_CLK15
21	GPIOL_24_CDI7	22	GPIOR_175_CLK14
23	GND	24	GPIOR_188_PLLIN2
25	GPIOL_66_CLK0	26	GND
27	GPIOL_67_CLK1	28	GPIOT_TXP21
29	GPIOL_65_CTRL3	30	GPIOT_TXN21
31	GPIOL_64_CTRL2	32	GPIOT_TXP22
33	GPIOL_63_CTRL1	34	GPIOT_TXN22
35	GPIOL_62_CTRL0	36	GPIOT_TXP23
37	GPIOL_159	38	GPIOT_TXN23
39	GPIOL_160_PLLIN1	40	GPIOT_TXP24
41	GPIOL_162_EXTFB	42	GPIOT_TXN24
43	GND	44	GND
45	GPIOR_168_PLLIN2	46	GPIOT_TXP25
47	GPIOL_56	48	GPIOT_TXN25
49	GPIOL_53	50	GPIOT_TXP26
51	GPIOL_49	52	GPIOT_TXN26
53	GPIOL_36	54	GPIOT_TXP27
55	GPIOL_17_EXTFB0	56	GPIOT_TXN27
57	GPIOB_RXP29_CLKP2	58	GPIOT_TXP28
59	GPIOB_RXN29_CLKN2	60	GPIOT_TXN28
61	GND	62	GND

Headers P2, P3, and P4 (LVDS)

P2, P3, and P4 contain the LVDS signals. P2 header has 14 dedicated LVDS channels. P3 and P4 headers has 9 dedicated LVDS channels each. You can also use LVDS pins as GPIO.

Learn more: Refer to the Trion Interfaces User Guide for instructions on using the LVDS pins as GPIO.

Table 6: P2 Pin Assignments

Pin Number	Signal Name	Description	Pin Number	Signal Name	Description
1	GPIOB_TXP00	Dedicated LVDS TX Channel 00	2	GPIOB_TXP07	Dedicated LVDS TX Channel 07 (bottom)
3	GPIOB_TXN00		4	GPIOB_TXN07	
5	GND	Ground	6	GND	Ground
7	GPIOB_TXP01	Dedicated LVDS TX Channel 01	8	GPIOB_TXP08	Dedicated LVDS TX Channel 08
9	GPIOB_TXN01		10	GPIOB_TXN08	
11	GND	Ground	12	GND	Ground
13	GPIOB_TXP02	Dedicated LVDS TX Channel 02	14	GPIOB_TXP09	Dedicated LVDS TX Channel 09
15	GPIOB_TXN02		16	GPIOB_TXN09	
17	GND	Ground	18	GND	Ground
19	GPIOB_TXP03	Dedicated LVDS TX Channel 03	20	GPIOT_TXP07	Dedicated LVDS TX Channel 07 (top)
21	GPIOB_TXN03		22	GPIOT_TXN07	
23	GND	Ground	24	GND	Ground
25	GPIOB_TXP04	Dedicated LVDS TX Channel 04	26	GPIOT_TXP17	Dedicated LVDS TX Channel 17
27	GPIOB_TXN04		28	GPIOT_TXN17	
29	GND	Ground	30	GND	Ground
31	GPIOB_TXP05	Dedicated LVDS TX Channel 05	32	GPIOT_TXP18	Dedicated LVDS TX Channel 18
33	GPIOB_TXN05		34	GPIOT_TXN18	
35	GND	Ground	36	GND	Ground
37	GPIOB_TXP06	Dedicated LVDS TX Channel 06	38	GPIOT_TXP20	Dedicated LVDS TX Channel 20
39	GPIOB_TXN06		40	GPIOT_TXN20	

Table 7: P3 Pin Assignments

Pin Number	Signal Name	Description	Pin Number	Signal Name	Description
1	GPIOT_RXP09_CLKP0	Dedicated LVDS RX clock	2	GPIOT_RXP07	Dedicated LVDS RX Channel 07
3	GPIOT_RXN09_CLKN0		4	GPIOT_RXN07	
5	GND	Ground	6	GND	Ground
7	GPIOT_RXP01	Dedicated LVDS RX Channel 01	8	GPIOT_RXP08	Dedicated LVDS RX Channel 08
9	GPIOT_RXN01		10	GPIOT_RXN08	
11	GND	Ground	12	GND	Ground
13	GPIOT_RXP02	Dedicated LVDS RX Channel 02	14	NC	No Connect
15	GPIOT_RXN02		16	NC	
17	GND	Ground	18	GND	Ground
19	GPIOT_RXP03	Dedicated LVDS RX Channel 03	20	NC	No Connect
21	GPIOT_RXN03		22	NC	
23	GND	Ground	24	GND	Ground
25	GPIOT_RXP04	Dedicated LVDS RX Channel 04	26	NC	No Connect
27	GPIOT_RXN04		28	NC	
29	GND	Ground	30	GND	Ground
31	GPIOT_RXP05	Dedicated LVDS RX Channel 05	32	NC	No Connect
33	GPIOT_RXN05		34	NC	
35	GND	Ground	36	GND	Ground
37	GPIOT_RXP06	Dedicated LVDS RX Channel 06	38	NC	No Connect
39	GPIOT_RXN06		40	NC	

Table 8: P4 Pin Assignments

Pin Number	Signal Name	Description	Pin Number	Signal Name	Description
1	GPIOT_RXP19_CLKP1	Dedicated LVDS RX clock	2	GPIOT_RXP17	Dedicated LVDS RX Channel 17
3	GPIOT_RXN19_CLKN1		4	GPIOT_RXN17	
5	GND	Ground	6	GND	Ground
7	GPIOT_RXP11	Dedicated LVDS RX Channel 11	8	GPIOT_RXP18	Dedicated LVDS RX Channel 18
9	GPIOT_RXN11		10	GPIOT_RXN18	
11	GND	Ground	12	GND	Ground
13	GPIOT_RXP12	Dedicated LVDS RX Channel 12	14	NC	No Connect
15	GPIOT_RXN12		16	NC	
17	GND	Ground	18	GND	Ground
19	GPIOT_RXP13	Dedicated LVDS RX Channel 13	20	NC	No Connect
21	GPIOT_RXN13		22	NC	
23	GND	Ground	24	GND	Ground
25	GPIOT_RXP14	Dedicated LVDS RX Channel 14	26	NC	No Connect
27	GPIOT_RXN14		28	NC	
29	GND	Ground	30	GND	Ground
31	GPIOT_RXP15	Dedicated LVDS RX Channel 15	32	NC	No Connect
33	GPIOT_RXN15		34	NC	
35	GND	Ground	36	GND	Ground
37	GPIOT_RXP16	Dedicated LVDS RX Channel 16	38	NC	No Connect
39	GPIOT_RXN16		40	NC	

Headers P5, P7 and P9 (MIPI Receiver)

P5, P7 and P9 are dedicated MIPI CSI-2 receiver high-speed interface connectors that support 1 clock lane and 4 data lanes. These headers also include optional supply pins VSUP1, VSUP2, VSUP3, as well as five 1.8 V or 3.3 V GPIO pins (user selectable). You can use these connectors to attach a camera connector daughter card.

Table 9: MIPI Receiver Channel 0 (P9), Channel 1 (P7), and Channel 2 (P5)

where x is 2, 1 or 0

Pin Number	Signal Name	Description	Pin Number	Signal Name	Description
1	VSUP1	Voltage supply 1	2	MIPI*x*_RXD_P0	Differential MIPI Receiver Channel Lane 0
3	VSUP2	Voltage supply 2	4	MIPI*x*_RXD_N0	
5	GND	Ground	6	GND	Ground
7	NC	No Connect	8	MIPI*x*_RXD_P1	Differential MIPI Receiver Channel Lane 1
9	NC		10	MIPI*x*_RXD_N1	
11	GND	Ground	12	GND	Ground
13	NC	No Connect	14	MIPI*x*_RXD_P2	Differential MIPI Receiver Channel Lane 2
15	NC		16	MIPI*x*_RXD_N2	
17	GND	Ground	18	GND	Ground
19	NC	No Connect	20	MIPI*x*_RXD_P3	Differential MIPI Receiver Channel Lane 3
21	NC		22	MIPI*x*_RXD_N3	
23	GND	Ground	24	GND	Ground
25	NC	No Connect	26	MIPI*x*_RXD_P4	Differential MIPI Receiver Channel 0 Lane 4
27	NC		28	MIPI*x*_RXD_N4	
29	GND	Ground	30	GND	Ground
31	NC	No Connect	32	PMOD_A_IO0 (P9) PMOD_B_IO0 (P7) PMOD_C_IO0 (P5)	1.8 or 3.3 V GPIO
33	NC		34	PMOD_A_IO1(P9) PMOD_B_IO1 (P7) PMOD_C_IO1 (P5)	1.8 or 3.3 V GPIO
35	GND	Ground	36	GND	Ground
37	VSUP3	Voltage supply 3	38	PMOD_A_IO2 (P9) PMOD_B_IO2 (P7) PMOD_C_IO2 (P5)	1.8 or 3.3 V GPIO
39	PMOD_D_IO4 (P5) PMOD_D_IO2 (P7) PMOD_D_IO0 (P9)	1.8 or 3.3 V GPIO	40	PMOD_A_IO3 (P9) PMOD_B_IO3 (P7) PMOD_C_IO3 (P5)	1.8 or 3.3 V GPIO

Headers P6, P8, and P10 (MIPI Transmitters)

P6, P8, and P10 are dedicated MIPI CSI-2 transmitter high-speed interface connectors that support 1 clock lane and 4 data lanes. These headers also include optional supply pins VSUP1, VSUP2, VSUP3, as well as five 1.8 V or 3.3 V GPIO pin (user selectable). You can use these connectors to attach a camera connector daughter card.

Note: P6, P8, and P10 are located on the bottom of the board.

Table 10: MIPI Transmitter Channel 0 (P10), Channel 1(P8) and Channel 2 (P6)

where x is 2, 1 or 0

Pin Number	Signal Name	Description	Pin Number	Signal Name	Description
1	VSUP1	Voltage supply 1	2	MIPI*x*_TXD_P0	Differential MIPI Transmitter Channel Lane 0
3	VSUP2	Voltage supply 2	4	MIPI*x*_TXD_N0	
5	GND	Ground	6	GND	Ground
7	NC	No Connect	8	MIPI*x*_TXD_P1	Differential MIPI Transmitter Channel Lane 1
9	NC		10	MIPI*x*_TXD_N1	
11	GND	Ground	12	GND	Ground
13	NC	No Connect	14	MIPI*x*_TXD_P2	Differential MIPI Transmitter Channel Lane 2
15	NC		16	MIPI*x*_TXD_N2	
17	GND	Ground	18	GND	Ground
19	NC	No Connect	20	MIPI*x*_TXD_P3	Differential MIPI Transmitter Channel Lane 3
21	NC		22	MIPI*x*_TXD_N3	
23	GND	Ground	24	GND	Ground
25	NC	No Connect	26	MIPI*x*_TXD_P4	Differential MIPI Transmitter Channel Lane 4
27	NC		28	MIPI*x*_TXD_N4	
29	GND	Ground	30	GND	Ground
31	NC	No Connect	32	PMOD_A_IO4 (P10) PMOD_B_IO4 (P8) PMOD_C_IO4 (P6)	1.8 or 3.3 V GPIO
33	NC		34	PMOD_A_IO5 (P10) PMOD_B_IO5 (P8) PMOD_C_IO5 (P6)	1.8 or 3.3 V GPIO
35	GND	Ground	36	GND	Ground
37	VSUP3	Voltage supply 3	38	PMOD_A_IO6 (P10) PMOD_B_IO6 (P8) PMOD_C_IO6 (P6)	1.8 or 3.3 V GPIO
39	PMOD_D_IO5 (P6) PMOD_D_IO3 (P8) PMOD_D_IO1 (P10)	1.8 or 3.3 V GPIO	40	PMOD_A_IO7 (P10) PMOD_B_IO7 (P8) PMOD_C_IO7 (P6)	1.8 or 3.3 V GPIO

Header J1 (12 V Power)

J1 is a 12 V DC power supply input jack. J1 supplies power to regulators on the board that power the T120F576I4 FPGA. The maximum current supply to this input jack is 10 A.

Header J2 and J3

J2 and J3 are a 6-pin headers used to select the voltage supply for banks 2F (J2) and bank 4A (J3). By default, the jumpers connect pin 1 and 2, which is 3.3 V. Connect the jumpers as shown in the following table to change the voltages..

Jumper	VCCIO2F (J2)	VCCIO4A (J3)
Connect pins 1 and 2	3.3 V (default)	3.3 V (default)
Connect pins 3 and 4	2.5 V	2.5 V
Connect pins 5 and 6	1.8 V	1.8 V

Warning: For J2 and J3, only select one voltage at a time; otherwise you may damage the board.

Header J4, J5, and J6 (Power Select)

J4, J5, and J6 are headers you use to select the voltage and/or power up sequence option. Use a jumper across 2 pins to make your selection.

- J4 controls the voltage (5.0, 3.3, and 2.8) for the 4 MIPI headers and 2 LVDS headers
- J5 controls the voltage (3.3 and 1.8) for the 4 MIPI headers and 2 LVDS headers
- J6 controls the voltage (1.2) for the four MIPI headers

Table 11: Voltage Selection for J4, J5, and J6

Jumper	VSUP1 (J4)	VSUP2 (J5)	VSUP3 (J6)
Connect pins 1 and 2	5.0 V	3.3 V	1.2 V
Connect pins 3 and 4	3.3 V	1.8 V	1.2 V with power up sequence (default)
Connect pins 5 and 6	3.3 V with power up sequence	1.8 V with power up sequence (default)	-
Connect pins 7 and 8	2.8 V	-	-
Connect pins 9 and 10	2.8 V with power up sequence (default)	-	-

Warning: For each header, only select one voltage at a time; otherwise you may damage the board.

Header J7 (SPI)

J7 is a SPI interface that you can use to configure the on-board NOR flash or T120F576I4 FPGA.

Table 12: J7 Pin Assignments

Pin Number	Signal Name	Description	T120F576I4 Pin Name
1	CCK	SPI configuration clock	GPIOL_01_CCK
2	CRESET_N	Configuration reset pin (active low)	CRESET_N
3	CDI0	SPI serial data output	GPIOL_08_CDI0
4	CONDONE	Configuration done status pin	CDONE
5	CDI1	SPI serial data input	GPIOL_09_CDI1
6	HOLD	SPI hold pin (active low)	-
7	SS	SPI slave select pin (active low)	GPIOL_00_SS
8	3V3	3.3 V power supply	-
9	FTDI_RST	Reset pin for on board FTDI FT2232 chipset (active low)	-
10	GND	Ground	-

Header J8 (JTAG)

Headers J8 is the JTAG interfaces for configuration or boundary scan testing.

Table 13: J8 Pin Assignments

Pin Number	Signal Name	Description
1	TDO	JTAG data output signal
2	3.3V	3.3 V power supply
3	TCK	JTAG data clock
4	TDI	JTAG data input
5	TMS	JTAG TMS mode select
6	FTDI_RST	Reset pin for on-board FTDI FT2232 module (active low)
7	SS	Slave select signal
8	CRESET_N	Configuration reset pin (active low)
9	GND	Ground
10	GND	Ground

Header J10 and J12 (Clock and PLL Input Select)

J10 and J12 are a 3-pin header used to select the source for the T120F576I4 clock input and PLL input. Drive a 3.3 V clock source input into the SMA connector, J9 or J11, if you are using the external clock source option.

Table 14: J10 Clock Selection Pin Assignments

Pin Number	Signal	Notes
1	External clock source from SMA input J9	Connect pins 2 and 3 to select the SMA input
2	GPIOL_164_PLLIN0	
3 (default)	30 MHz on-board oscillator	Connect pins 1 and 2 to select the oscillator

Table 15: J12 Clock Selection Pin Assignments

Pin Number	Signal	Notes
1	External clock source from SMA input J9	Connect pins 2 and 3 to select the SMA input
2	GPIOR_167_PLLIN1	
3 (default)	10 MHz on-board oscillator	Connect pins 1 and 2 to select the oscillator

Headers J13, J14, J15, J16, J17, and J18 (PMOD)

J13, J14, J15, J16, J17, and J18 are 12-pin sockets for connecting to peripheral modules (PMODs) such as ADC, DAC, audio, WiFi, Bluetooth, etc. These interfaces support PMOD type 1, 2, 2A, 3, 4, 4A, 5 and 6. You can choose between 1.8 V, 2.5 V, and 3.3 V for these sockets.

Table 16: J13 Pin Assignments

Pin Number	Signal Name	T120F576I4 Pin Name	Pin Number	Signal Name	T120F576I4 Pin Name
1	PMOD_A_IO0	GPIOB_RXN24	7	PMOD_A_IO1	GPIOB_RXP24
2	PMOD_A_IO2	GPIOB_RXP23	8	PMOD_A_IO3	GPIOB_RXN23
3	PMOD_A_IO4	GPIOB_RXN21	9	PMOD_A_IO5	GPIOB_RXP21
4	PMOD_A_IO6	GPIOB_RXN22	10	PMOD_A_IO7	GPIOB_RXP22
5	GND	-	11	GND	-
6	3.3 V	-	12	3.3 V	-

Table 17: J14 Pin Assignments

Pin Number	Signal Name	T120F576I4 Pin Name	Pin Number	Signal Name	T120F576I4 Pin Name
1	PMOD_B_IO0	GPIOB_RXN26	7	PMOD_B_IO1	GPIOB_RXN25
2	PMOD_B_IO2	GPIOB_RXP27	8	PMOD_B_IO3	GPIOB_RXP26
3	PMOD_B_IO4	GPIOB_RXN27	9	PMOD_B_IO5	GPIOB_RXP25
4	PMOD_B_IO6	GPIOB_RXP28	10	PMOD_B_IO7	GPIOB_RXN28
5	GND	-	11	GND	-
6	3.3 V	-	12	3.3 V	-

Table 18: J15 Pin Assignments

Pin Number	Signal Name	T120F576I4 Pin Name	Pin Number	Signal Name	T120F576I4 Pin Name
1	PMOD_C_IO0	GPIOT_RXP20	7	PMOD_C_IO1	GPIOT_RXN20
2	PMOD_C_IO2	GPIOT_RXP21	8	PMOD_C_IO3	GPIOT_RXN21
3	PMOD_C_IO4	GPIOT_RXP22	9	PMOD_C_IO5	GPIOT_RXN22
4	PMOD_C_IO6	GPIOT_RXP23	10	PMOD_C_IO7	GPIOT_RXN23
5	GND	-	11	GND	-
6	3.3 V	-	12	3.3 V	-

Table 19: J16 Pin Assignments

Pin Number	Signal Name	T120F576I4 Pin Name	Pin Number	Signal Name	T120F576I4 Pin Name
1	PMOD_D_IO0	GPIOT_RXP24	7	PMOD_D_IO1	GPIOT_RXN24
2	PMOD_D_IO2	GPIOT_RXP27	8	PMOD_D_IO3	GPIOT_RXN27
3	PMOD_D_IO4	GPIOT_RXP28	9	PMOD_D_IO5	GPIOT_RXN28
4	PMOD_D_IO6	GPIOT_RXP29	10	PMOD_D_IO7	GPIOT_RXN29
5	GND	-	11	GND	-
6	3.3 V	-	12	3.3 V	-

Table 20: J17 Pin Assignments

Pin Number	Signal Name	T120F576I4 Pin Name	Pin Number	Signal Name	T120F576I4 Pin Name
1	PMOD_E_IO0	GPIOT_TXP13	7	PMOD_E_IO1	GPIOT_TXN13
2	PMOD_E_IO2	GPIOT_TXP14	8	PMOD_E_IO3	GPIOT_TXN14
3	PMOD_E_IO4	GPIOT_TXP15	9	PMOD_E_IO5	GPIOT_TXN15
4	PMOD_E_IO6	GPIOT_TXP16	10	PMOD_E_IO7	GPIOT_TXN16
5	GND	-	11	GND	-
6	3.3 V	-	12	3.3 V	-

Table 21: J18 Pin Assignments

Pin Number	Signal Name	T120F576I4 Pin Name	Pin Number	Signal Name	T120F576I4 Pin Name
1	PMOD_F_IO0	GPIOB_TXP16	7	PMOD_F_IO1	GPIOB_TXN16
2	PMOD_F_IO2	GPIOB_TXP17	8	PMOD_F_IO3	GPIOB_TXN17
3	PMOD_F_IO4	GPIOB_TXP18	9	PMOD_F_IO5	GPIOB_TXN18
4	PMOD_F_IO6	GPIOB_TXP19	10	PMOD_F_IO7	GPIOB_TXN19
5	GND	-	11	GND	-
6	3.3 V	-	12	3.3 V	-

Header J19 (Raspberry Pi)

J19 is a 40-pin connector that is compatible with Raspberry Pi computers. It connects to GPIO pins in banks 2A and 4B.

Note: J19 is located on the bottom of the board.

Table 22: J19 Pin Assignments

Pin Number	Signal Name	T120F576I4 Pin Name	Pin Number	Signal Name	T120F576I4 Pin Name
1	3.3 V	-	2	5.0 V	-
3	RASPI_GPIO2	GPIOT_TXP05	4	5.0 V	-
5	RASPI_GPIO3	GPIOT_TXN05	6	GND	-
7	RASPI_GPIO4	GPIOT_TXN06	8	RASPI_GPIO14	GPIOT_TXP06
9	GND	-	10	RASPI_GPIO15	GPIOT_TXP03
11	RASPI_GPIO17	GPIOT_TXN03	12	RASPI_GPIO18	GPIOT_TXP04
13	RASPI_GPIO27	GPIOT_TXN04	14	GND	-
15	RASPI_GPIO22	GPIOB_RXN14	16	RASPI_GPIO23	GPIOB_RXP14
17	3.3 V	-	18	RASPI_GPIO24	GPIOB_RXP11
19	RASPI_GPIO10	GPIOB_RXN11	20	GND	-
21	RASPI_GPIO9	GPIOB_RXP12	22	RASPI_GPIO25	GPIOB_RXN12
23	RASPI_GPIO11	GPIOB_RXP15	24	RASPI_GPIO8	GPIOB_RXN15
25	GND	-	26	RASPI_GPIO7	GPIOB_RXN13
27	NC	-	28	NC	-
29	RASPI_GPIO5	GPIOB_RXP13	30	GND	-
31	RASPI_GPIO6	GPIOB_RXP17	32	RASPI_GPIO12	GPIOB_RXN17
33	RASPI_GPIO13	GPIOB_RXN18	34	GND	-
35	RASPI_GPIO19	GPIOB_RXN16	36	RASPI_GPIO16	GPIOB_RXP18
37	RASPI_GPIO26	GPIOB_RXN19	38	RASPI_GPIO20	GPIOB_RXP16
39	GND	-	40	RASPI_GPIO21	GPIOB_RXP19

Header J20 (USB Connector)

J20, a micro-USB type B socket, is the interface between the board and your computer for communication. Connect the micro-USB cable for configuring T120F576I4 FPGA and NOR flash. The board supports three different configuration modes: SPI passive mode, SPI active mode, and JTAG mode.

Note: The USB cable cannot power the board.

Header J21 and J22 (RJ-45 Ethernet)

The board has two Gigabit Ethernet transceivers from Davicom (part number: DM9119INP, which is compliant with IEEE Std. 802.33 MAC and IEEE STD. 802.3I 1000BASE-TX/100BASE-TX/10BASE-T. The chip supports:

- Reduced Gigabit Media Independent Interface (RGMII) to the MAC controller
- Standard unshielded twisted pair (UTP) CAT6, CAT5e, CAT5, CAT3 cable (10 Mbps only)
- Auto-negotiation with auto MDI/MDI crossover correction, auto polarity correction, and power down mode
- Advanced DSP for baseline wander correction, equalization, echo, and crosstalk cancellation

The Ethernet transceivers are set to the following address:

- *U19*—0x03H
- *U20*—0x07H

Table 23: J21 (Ethernet) Pin Assignments

Signal Name	U19 Pin Name	T120F576I4 Pin Name	Description
ETH1_GTXCLK	GTXCLK	GPIOL_68	GMII transmit clock
ETH1_TXEN	TXEN	GPIOT_TXP02	GMII/MII transmit enable
ETH1_TXD3	TXD[3]	GPIOL_85	GMII and MII transmit data
ETH1_TXD2	TXD[2]	GPIOL_77	GMII and MII transmit data
ETH1_TXD1	TXD[1]	GPIOL_76	GMII and MII transmit data
ETH1_TXD0	TXD[0]	GPIOL_75	GMII and MII transmit data
ETH1_RXC	RXC	GPIOL_70	GMII and MII receive clock
ETH1_RXDV	RXDV/AD[2]	GPIOT_TXN02	GMII and MII receive data valid
ETH1_RXD3	RXD[3]/AN[1]	GPIOL_91	GMII and MII receive data
ETH1_RXD2	RXD[2]/AN[0]	GPIOL_89	GMII and MII receive data
ETH1_RXD1	RXD[1]/TXDLY	GPIOL_88	GMII and MII receive data
ETH1_RXD0	RXD[0]/AD[3]	GPIOL_87	GMII and MII receive data
ETH1_RSTN	RSTN	GPIOT_TXP01	Global reset input; active-low to reset the entire chip
ETH1_MDC	MDC	GPIOT_TXN01	Serial clock line
ETH1_MDIO	MDIO	GPIOT_TXN00	Serial data line
ETH1_IRQ	IRQ	GPIOT_TXP00	Interrupt to MAC

Table 24: J22 (Ethernet) Pin Assignments

Signal Name	U19 Pin Name	T120F576I4 Pin Name	Description
ETH2_GTXCLK	GTXCLK	GPIOL_69	GMII transmit clock
ETH2_TXEN	TXEN	GPIOT_TXN10	GMII/MII transmit enable
ETH2_TXD3	TXD[3]	GPIOR_184	GMII and MII transmit data
ETH2_TXD2	TXD[2]	GPIOR_179	GMII and MII transmit data
ETH2_TXD1	TXD[1]	GPIOR_178	GMII and MII transmit data
ETH2_TXD0	TXD[0]	GPIOR_185	GMII and MII transmit data
ETH2_RXC	RXC	GPIOL_71	GMII and MII receive clock
ETH2_RXDV	RXDV/AD[2]	GPIOT_TXP12	GMII and MII receive data valid
ETH2_RXD3	RXD[3]/AN[1]	GPIOR_181	GMII and MII receive data
ETH2_RXD2	RXD[2]/AN[0]	GPIOR_183	GMII and MII receive data
ETH2_RXD1	RXD[1]/TXDLY	GPIOR_182	GMII and MII receive data
ETH2_RXD0	RXD[0]/AD[3]	GPIOR_176	GMII and MII receive data
ETH2_RSTN	RSTN	GPIOT_TXN12	Global reset input; active-low to reset the entire chip
ETH2_MDC	MDC	GPIOT_TXP11	Serial clock line
ETH2_MDIO	MDIO	GPIOT_TXP10	Serial data line
ETH2_IRQ	IRQ	GPIOT_TXN11	Interrupt to MAC

Header J23 (HDMI)

J23 is an HDMI connector that outputs video through the on-board LVDS HDMI transmitter from ITE Tech. Inc. (part number: IT6263N). The IT6263 (U21) is a high-performance, single-chip De-SSC LVDS to HDMI converter. It supports HDMI v1.4a standard with resolutions up to 1080p with UXGA and 10-bit deep colors. The HDMI transmitter I/O pins are connected to banks 1D, 4D and 4E. The HDMI device is set to address 0x98, and you can access it through the I^2C interface.

Table 25: J23 HDMI Pin Assignments

Signal Name	U21 Pin Name	T120F576I4 Pin Name	Description
HDMI_RESET	SYSRSTN	GPIOL_74	Hardware reset pin. Active Low
HDMI_RXPCLK	RXPCLK	GPIOB_TXP26	LVDS positive clock input
HDMI_RXNCLK	RXNCLK	GPIOB_TXN26	LVDS negative clock input
HDMI_RXPA1	RXPA1	GPIOB_TXP13	LVDS first link positive input
HDMI_RXNA1	RXNA1	GPIOB_TXN13	LVDS first link negative input
HDMI_RXPB1	RXPB1	GPIOB_TXP24	LVDS first link positive input
HDMI_RXNB1	RXNB1	GPIOB_TXN24	LVDS first link negative input
HDMI_RXPC1	RXPC1	GPIOB_TXP25	LVDS first link positive input
HDMI_RXNC1	RXNC1	GPIOB_TXN25	LVDS first link negative input
HDMI_RXPD1	RXPD1	GPIOB_TXP23	LVDS first link positive input
HDMI_RXND1	RXND1	GPIOB_TXN23	LVDS first link negative input
HDMI_RXPE1	RXPE1	GPIOB_TXP22	LVDS first link positive input
HDMI_RXNE1	RXNE1	GPIOB_TXN22	LVDS first link negative input
HDMI_RXPA2	RXPA2	GPIOB_TXP10	LVDS second link positive input
HDMI_RXNA2	RXNA2	GPIOB_TXN10	LVDS second link negative input
HDMI_RXPB2	RXPB2	GPIOB_TXP12	LVDS second link positive input
HDMI_RXNB2	RXNB2	GPIOB_TXN12	LVDS second link negative input
HDMI_RXPC2	RXPC2	GPIOB_TXP11	LVDS second link positive input
HDMI_RXNC2	RXNC2	GPIOB_TXN11	LVDS second link negative input
HDMI_RXPD2	RXPD2	GPIOB_TXP14	LVDS second link positive input
HDMI_RXND2	RXND2	GPIOB_TXN14	LVDS second link negative input
HDMI_RXPE2	RXPE2	GPIOB_TXP21	LVDS second link positive input
HDMI_RXNE2	RXNE2	GPIOB_TXN21	LVDS second link negative input
HDMI_PCSCL	PCSCL	GPIOT_TXP15	Serial programming clock for chip programming
HDMI_PCSDA	PCSDA	GPIOT_TXN15	Serial programming data for chip programming

Header J24 (Configurable Clock Generator)

J24 is an I2C bus header that connects to the on-board I2C configurable clock generator, Si5351A-B11429-GT (U14)[2]. You can change the clock output frequency of the clock generator through J24 header. Refer to part manufacturer for the correct procedure in configuring Si3531A clock generator.

Table 26: J24 (Configurable Clock Generator) Pin Assignments

Pin Number	Signal Name	T120F576I4 Pin Name	Description
1	SCL_SILAB	GPIOL_72	Serial clock input for clock generator.
2	SDA_SILAB	GPIOL_73	Serial data line for clock generator.
3	GND	-	Ground

User Outputs

The board has 8 green user LEDs that are connected to I/O pins in T120F576I4 banks 2F. By default, the T120F576I4 I/O connected to these LEDs are set as active high. To turn a given LED on, pull the corresponding I/O signal high.

Note: When adding these GPIO in the Efinity® Interface Designer, configure them as output pins.

Table 27: User Outputs

Reference Designator	Schematic Name	T120F576I4 Pin Name	Active
D7	USER_LED0	GPIOB_RXP04	High
D8	USER_LED1	GPIOB_RXN04	High
D9	USER_LED2	GPIOB_RXP05	High
D10	USER_LED3	GPIOB_RXN05	High
D11	USER_LED4	GPIOB_RXP06	High
D12	USER_LED5	GPIOB_RXN06	High
D13	USER_LED6	GPIOB_RXP07	High
D14	USER_LED7	GPIOB_RXN07	High

[2] Only applicable to Rev.BBA board.

User Inputs

The board has 4 pushbutton switches and 4 DIP switches that you can use as inputs to the T120F576I4 device. The T120F576I4 bank 2F I/O signals connect to T120F576I4 pins to control the functionality. When building designs using this switches, turn on an internal pull up for these pins in the Interface Designer.

When you press the pushbutton switches the signal drives low, indicating user input. Turning the DIP switch to the on position drives the signal low.

Table 28: User Pushbuttons

Reference Designator	Schematic Name	T120F576I4 Pin Name	Active
SW6	USER_SWITCH0	GPIOB_RXP08	Low
SW7	USER_SWITCH1	GPIOB_RXN08	Low
SW8	USER_SWITCH3	GPIOB_RXP09	Low
SW9	USER_SWITCH4	GPIOB_RXN09	Low

Table 29: User DIP Switches

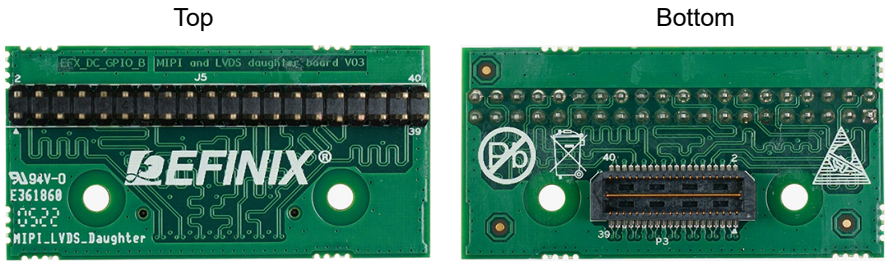
Reference Designator	Schematic Name	T120F576I4 Pin Name	Active
SW5.1	USER_DIP0	GPIOB_RXP02	Low
SW5.2	USER_DIP1	GPIOB_RXN02	Low
SW5.3	USER_DIP2	GPIOB_RXP03	Low
SW5.4	USER_DIP3	GPIOB_RXN03	Low

MIPI and LVDS Expansion Daughter Card

The MIPI and LVDS Expansion Daughter Card (part number: EFX_DC_GPIO_B) converts the signals from the development board's QSE connector.

Learn more: Refer to the **MIPI and LVDS Expansion Daughter Card Schematics and BOM** for the part details and schematics.

Figure 4: MIPI and LVDS Expansion Daughter Card



Warning: The board can be damaged without proper anti-static handling.

Features

- Bridges 40-pin QSE connector on the development board to a 40-pin header
- Power supplied from the development board; no external power required
  - Each pin supports up to 3 A

Headers

Table 30: MIPI and LVDS Expansion Daughter Card Headers

Reference Designator	Description
P3	40-pin QTE connector bringing MIPI or LVDS signals, power, and 1.8 V GPIO pins from the development board.
J5	40-pin header.

Headers P3 (QTE Connector) and J5 (40-Pin Header)

P3 is a 40-pin QTE connector to connect the daughter card to the QSE connector on the development board. J5 is a 40-pin header.

Table 31: P3 and J5 Pin Assignments

Pin Number	Pin Name	Description	Pin Number	Pin Name	Description
1	GPIO_H01	User I/O	2	GPIO_H02	User I/O
3	GPIO_H03	User I/O	4	GPIO_H04	User I/O
5	GND	Ground	6	GND	Ground
7	GPIO_H07	User I/O	8	GPIO_H08	User I/O
9	GPIO_H09	User I/O	10	GPIO_H10	User I/O
11	GND	Ground	12	GND	Ground
13	GPIO_H13	User I/O	14	GPIO_H14	User I/O
15	GPIO_H15	User I/O	16	GPIO_H16	User I/O
17	GND	Ground	18	GND	Ground
19	GPIO_H19	User I/O	20	GPIO_H20	User I/O
21	GPIO_H21	User I/O	22	GPIO_H22	User I/O
23	GND	Ground	24	GND	Ground
25	GPIO_H25	User I/O	26	GPIO_H26	User I/O
27	GPIO_H27	User I/O	28	GPIO_H28	User I/O
29	GND	Ground	30	GND	Ground
31	GPIO_H31	User I/O	32	GPIO_H32	User I/O
33	GPIO_H33	User I/O	34	GPIO_H34	User I/O
35	GND	Ground	36	GND	Ground
37	GPIO_H37	User I/O	38	GPIO_H38	User I/O
39	GPIO_H39	User I/O	40	GPIO_H40	User I/O

Signal Mapping

MIPI Signal Mapping

This table shows the pin mapping from the MIPI headers (P5, P6, P7, P8, P9, and P10) to the daughter card headers.

Table 32: MIPI Signal Mapping

Where x is 0 or 1 and y is TXD or RXD

Pin Number	Daughter Card Pin	MIPI Pin	Pin Number	Daughter Card Pin	MIPI Pin
1	GPIO_H01	VSUP1	2	GPIO_H02	MIPI*x_y*_P0
3	GPIO_H03	VSUP2	4	GPIO_H04	MIPI*x_y*_N0
5	GND	GND	6	GND	GND
7	NC	No Connect	8	GPIO_H08	MIPI*x_y*_P1
9	NC		10	GPIO_H10	MIPI*x_y*_N1
11	GND	GND	12	GND	GND
13	NC	No Connect	14	GPIO_H14	MIPI*x_y*_P2
15	NC		16	GPIO_H16	MIPI*x_y*_N2
17	GND	GND	18	GND	GND
19	NC	No Connect	20	GPIO_H20	MIPI*x_y*_P3
21	NC		22	GPIO_H22	MIPI*x_y*_N3
23	GND	GND	24	GND	GND
25	NC	No Connect	26	GPIO_H26	MIPI*x_y*_P4
27	NC		28	GPIO_H28	MIPI*x_y*_N4
29	GND	GND	30	GND	GND
31	NC	No Connect	32	GPIO_H32	PMOD_C_IO0 (P5) PMOD_C_IO4 (P6) PMOD_B_IO0 (P7) PMOD_B_IO4 (P8) PMOD_A_IO0 (P9) PMOD_A_IO4 (P10)
33	NC		34	GPIO_H34	PMOD_C_IO1 (P5) PMOD_C_IO5 (P6) PMOD_B_IO1 (P7) PMOD_B_IO5 (P8) PMOD_A_IO1(P9) PMOD_A_IO5 (P10)
35	GND	GND	36	GND	GND

Pin Number	Daughter Card Pin	MIPI Pin	Pin Number	Daughter Card Pin	MIPI Pin
37	GPIO_H37	VSUP3	38	GPIO_H38	PMOD_C_IO2 (P5) PMOD_C_IO6 (P6) PMOD_B_IO2 (P7) PMOD_B_IO6 (P8) PMOD_A_IO2 (P9) PMOD_A_IO6 (P10)
39	GPIO_H39	PMOD_D_IO4 (P5) PMOD_D_IO5 (P6) PMOD_D_IO2 (P7) PMOD_D_IO3 (P8) PMOD_D_IO0 (P9) PMOD_D_IO1 (P10)	40	GPIO_H40	PMOD_C_IO3 (P5) PMOD_C_IO7 (P6) PMOD_B_IO3 (P7) PMOD_B_IO7 (P8) PMOD_A_IO3 (P9) PMOD_A_IO7 (P10)

LVDS Signal Mapping

This table shows the pin mapping from the LVDS headers (P2, P3, and P4) to the daughter card headers.

Table 33: LVDS Signal Mapping

Pin Number	Daughter Card Pin	Signal Name	Signal Name	Signal Name
1	GPIO_H01	GPIOB_TXP00	GPIOT_RXP09_CLKP0	GPIOT_RXP19_CLKP1
2	GPIO_H02	GPIOB_TXP07	GPIOT_RXP07	GPIOT_RXP17
3	GPIO_H03	GPIOB_TXN00	GPIOT_RXN09_CLKN0	GPIOT_RXN19_CLKN1
4	GPIO_H04	GPIOB_TXN07	GPIOT_RXN07	GPIOT_RXN17
5	GND	GND	GND	GND
6	GND	GND	GND	GND
7	GPIO_H07	GPIOB_TXP01	GPIOT_RXP01	GPIOT_RXP11
8	GPIO_H08	GPIOB_TXP08	GPIOT_RXP08	GPIOT_RXP18
9	GPIO_H09	GPIOB_TXN01	GPIOT_RXN01	GPIOT_RXN11
10	GPIO_H10	GPIOB_TXN08	GPIOT_RXN08	GPIOT_RXN18
11	GND	GND	GND	GND
12	GND	GND	GND	GND
13	GPIO_H13	GPIOB_TXP02	GPIOT_RXP02	GPIOT_RXP12
14	GPIO_H14	GPIOB_TXP09	NC	NC
15	GPIO_H15	GPIOB_TXN02	GPIOT_RXN02	GPIOT_RXN12
16	GPIO_H16	GPIOB_TXN09	NC	NC
17	GND	GND	GND	GND
18	GND	GND	GND	GND
19	GPIO_H19	GPIOB_TXP03	GPIOT_RXP03	GPIOT_RXP13
20	GPIO_H20	GPIOT_TXP07	NC	NC
21	GPIO_H21	GPIOB_TXN03	GPIOT_RXN03	GPIOT_RXN13

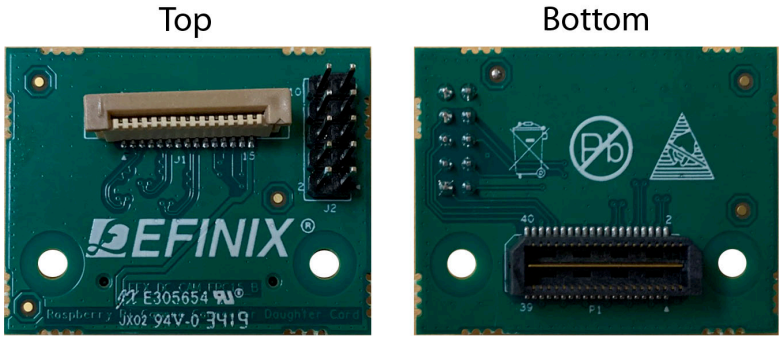
Pin Number	Daughter Card Pin	Signal Name	Signal Name	Signal Name
22	GPIO_H22	GPIOT_TXN07	NC	NC
23	GND	GND	GND	GND
24	GND	GND	GND	GND
25	GPIO_H25	GPIOB_TXP04	GPIOT_RXP04	GPIOT_RXP14
26	GPIO_H26	GPIOT_TXP17	NC	NC
27	GPIO_H27	GPIOB_TXN04	GPIOT_RXN04	GPIOT_RXN14
28	GPIO_H28	GPIOT_TXN17	NC	NC
29	GND	GND	GND	GND
30	GND	GND	GND	GND
31	GPIO_H31	GPIOB_TXP05	GPIOT_RXP05	GPIOT_RXP15
32	GPIO_H32	GPIOT_TXP18	NC	NC
33	GPIO_H33	GPIOB_TXN05	GPIOT_RXN05	GPIOT_RXN15
34	GPIO_H34	GPIOT_TXN18	NC	NC
35	GND	GND	GND	GND
36	GND	GND	GND	GND
37	GPIO_H37	GPIOB_TXP06	GPIOT_RXP06	GPIOT_RXP16
38	GPIO_H38	GPIOT_TXP20	NC	NC
39	GPIO_H39	GPIOB_TXN06	GPIOT_RXN06	GPIOT_RXN16
40	GPIO_H40	GPIOT_TXN20	NC	NC

Raspberry Pi Camera Connector Daughter Card

The Raspberry Pi Camera Connector Daughter Card (part number: EFX_DC_CAM_FPC15_B) bridges between the development board and a Raspberry Pi camera module. The daughter card connects to a Raspberry Pi computer or any Raspberry Pi camera using a 15 pin flat cable. Additionally, the board has a 10 pin header for optional camera control pins.

Learn more: Refer to the Raspberry Pi Camera Connector Daughter Card Schematics and BOM for the part details and schematics.

Figure 5: Raspberry Pi Camera Connector Daughter Card



Warning: The board can be damaged without proper anti-static handling.

Features

- Bridges 40-pin MIPI CSI-2 interface on a Trion® T120 BGA576 Development Board to a 15-pin interface
- Pin to pin compatible with Raspberry Pi cameras
- Supports up to 1.5 Gbps on MIPI interface
- User selectable pins for optional camera functions
- Power supplied from the Trion® T120 BGA576 Development Board; no external power required; each pin supports up to 3 A

Note: For technical support using Raspberry Pi cameras, please refer to their web site at www.raspberrypi.org.

Headers

Table 34: Raspberry Pi Camera Connector Daughter Card Headers

Reference Designator	Description
P1	40-pin QTE header bringing MIPI signals, power, and 1.8 V GPIO pins from the Trion® T120 BGA576 Development Board.
J1	15-pin flexible printed cable (FPC) connector for Raspberry Pi MIPI camera modules.
J2	10-pin header for optional Raspberry Pi MIPI camera module signals.

Header P1 (Development Board Connector)

P1 is a 40-pin QTE header to connect the daughter card to the development board. The header provides MIPI signals and power to the camera module.

- *Raspberry Pi computer*—When using this daughter card with a Raspberry Pi computer, connect header P1 to a MIPI TX socket on the development board.
- *Raspberry Pi camera*—When using this daughter card with a Raspberry Pi camera, connect header P1 to a MIPI RX socket on the development board.

Table 35: Development Board Connector (P1)

where *n* is RXD or TXD, depending on whether you are connecting to a camera or Raspberry Pi computer.

Pin Number	Pin Name	Description	Pin Number	Pin Name	Description
1	3V3_15FPC	3.3V Supply	2	MIPI_P0_15FPC	Differential MIPI lane 0
3	NC	No connect	4	MIPI_N0_15FPC	
5	GND	Ground	6	GND	Ground
7	NC	No connect	8	MIPI_P1_15FPC	Differential MIPI lane 1
9	NC		10	MIPI_N1_15FPC	
11	GND	Ground	12	GND	Ground
13	NC	No connect	14	MIPI_P2_15FPC	Differential MIPI lane 2
15	NC		16	MIPI_N2_15FPC	
17	GND	Ground	18	GND	Ground
19	NC	No connect	20	NC	No connect
21	NC		22	NC	
23	GND	Ground	24	GND	Ground
25	NC	No connect	26	NC	No connect
27	NC		28	NC	
29	GND	Ground	30	GND	Ground
31	NC	No connect	32	GPIO0	1.8 V GPIO
33	NC		34	GPIO1	1.8 V GPIO
35	GND	Ground	36	GND	Ground
37	NC	No connect	38	GPIO2	1.8 V GPIO
39	NC		40	GPIO3	1.8 V GPIO

Header J1 (Raspberry Pi FPC15 Connector)

J1 is a 15-pin flexible flat cable header for connecting to a Raspberry Pi MIPI camera module.

- *Raspberry Pi computer*—When using this daughter card with a Raspberry Pi computer, these pins are TX.
- *Raspberry Pi camera*—When using this daughter card with a Raspberry Pi camera, these pins are RX.

Table 36: Raspberry Pi FPC15 Connector (J1)

where *n* is RXD or TXD, depending on whether you are connecting to a camera or Raspberry Pi computer.

Pin Number	Pin Name	Description
1	GND	Ground
2	MIPI_N0_15FPC	Differential MIPI lane 0
3	MIPI_P0_15FPC	
4	GND	Ground
5	MIPI_N1_15FPC	Differential MIPI lane 1
6	MIPI_P1_15FPC	
7	GND	Ground
8	MIPI_N2_15FPC	Differential MIPI lane 2
9	MIPI_P2_15FPC	
10	GND	Ground
11	GPIO2_15FPC	GPIO for Raspberry Pi MIPI camera module
12	GPIO3_15FPC	
13	GPIO0_15FPC	Serial clock for Raspberry Pi MIPI camera module
14	GPIO1_15FPC	Serial data for Raspberry Pi MIPI camera module
15	3V3_15FPC	3.3 V power supply

Header J2 (Optional Camera Signals)

The J2 header has optional pins (SCL and SDA) that are used for MIPI Camera Command Set (CSS) transactions. These signals are routed to the Trion® FPGA on the board. You can control these pins with an external device by removing the jumpers and connecting wires from the header to an external device.

Note: If you connect jumpers to any pins in J2, do not use the corresponding GPIO in your design. For example, if you use jumpers on pins 1-2 and 3-4, do not use `GPIO_69` or `GPIO_70`.

Table 37: Optional Camera Signals (J2)

Pin Number	Pin Name	Description	Pin Number	Pin Name	Description
1	GPIO0	1.8 V I/O from development board	2	GPIO0_15FPC	I^2C bus SCL signal
3	GPIO1		4	GPIO1_15FPC	I^2C bus SDA signal
5	GPIO2		6	GPIO2_15FPC	Camera GPIO
7	GPIO3		8	GPIO3_15FPC	Camera clock
9	GND	Ground	10	GND	Ground

Setting up the Board

Installing Standoffs

Before using the board, attach the standoffs with the screws provided in the kit.

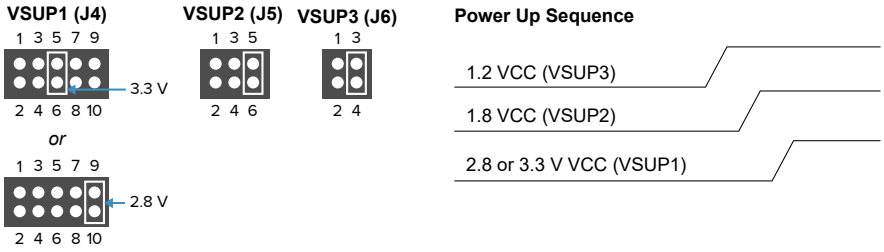
Warning: You can damage the board if you over tighten the screws. Tighten all screws to a torque between 4 ± 0.5 kgf/cm and 5 ± 0.5 kgf/cm.

Setting the Power-Up Sequence for MIPI Cameras

Trion® T120 BGA576 Development Board has a built-in power-up sequence circuit for the MIPI transmitter and receiver interfaces (P5, P6, P7, P8, P9, and P10) that is compatible with MIPI camera sensor power requirements. To enable the power-up sequence, you slide SW1 to position 3 and connect jumpers on the power supply headers J4, J5, and J6 for the voltages you want.

1. Remove power from the board.
2. Choose your camera voltage for VSUP1 (J4) by connecting pins 5 and 6 for 3.3 V or pins 9 and 10 for 2.8 V.
3. Connect pins 5 and 6 for VSUP2 (J5).
4. Connect pins 3 and 4 for VSUP3 (J6).
5. Slide SW1 to position 3.
6. Attach the camera connector daughter card for the camera you want to use to the board.
7. Attach the camera to the daughter card.
8. Turn on power to the board.

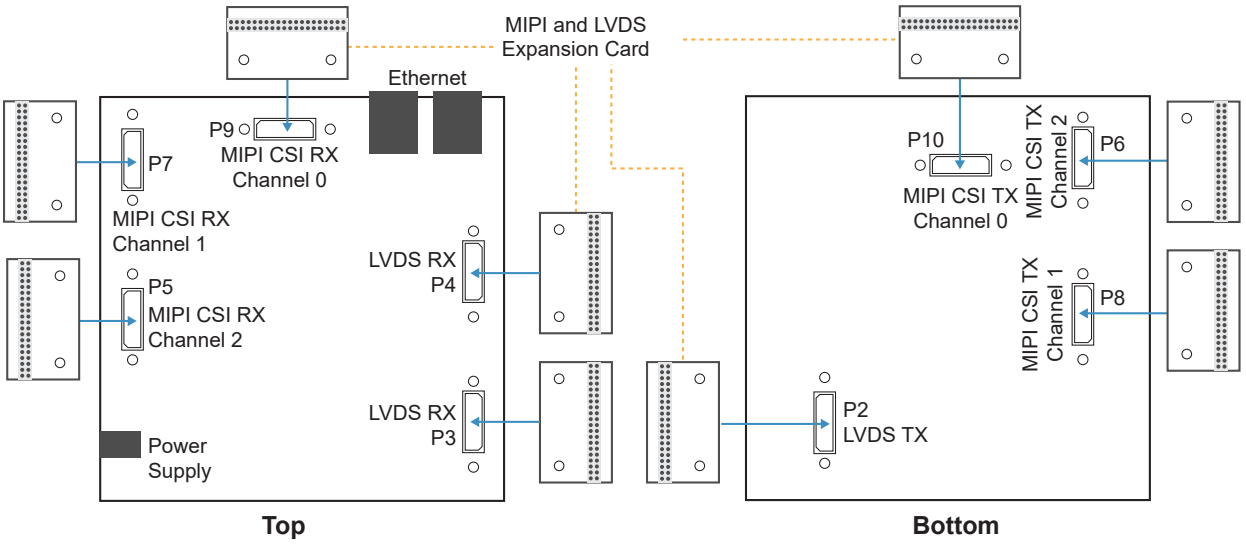
Figure 6: Setting the Power Sequence Jumpers



Attaching the MIPI and LVDS Expansion Daughter Card

The Trion® T120 BGA576 Development Board supports an expansion daughter card that fans out the GPIO.

Figure 7: Attaching MIPI and LVDS Expansion Daughter Card



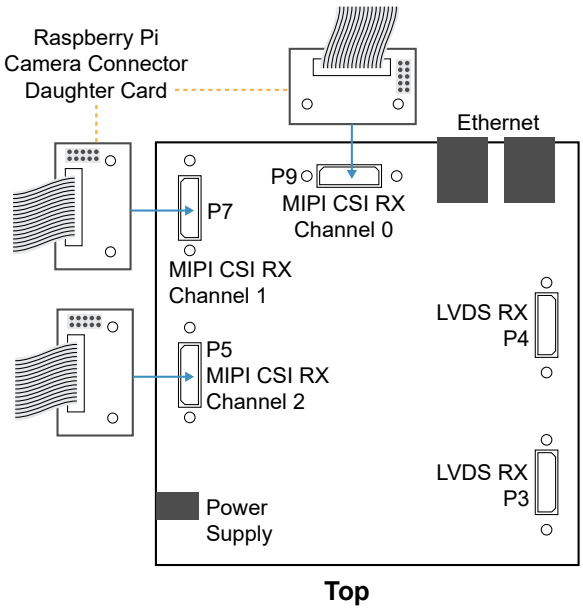
To connect the daughter card:

1. Remove power from the Trion® T120 BGA576 Development Board.
2. Attach standoffs to the MIPI and LVDS Expansion Daughter Card.
3. Attach the MIPI and LVDS Expansion Daughter Card to one of the LVDS or MIPI 40-pin headers on the Trion® T120 BGA576 Development Board.
4. Connect any cables to the GPIO as needed for your application.
5. Power up the Trion® T120 BGA576 Development Board.

Attaching Camera Connector Daughter Cards

The camera connector daughter card attaches to the high-speed MIPI TX or RX headers.

Figure 8: Attaching Camera Connector Daughter Cards (T120 BGA576 Board)



To connect a daughter card:

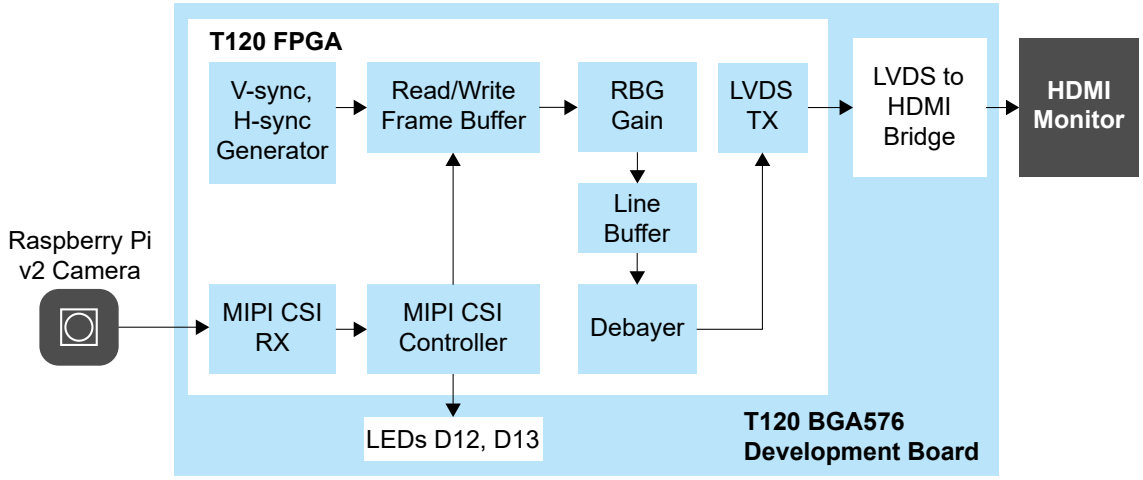
1. Remove power from the Trion® T120 BGA576 Development Board.
2. Attach standoffs to the daughter card.
3. Attach the daughter card to the 40-pin header on the board.
4. Connect the camera module or computer to the daughter card using a ribbon cable.
5. Power up the board.

Using the Example Design

Efinix® preloads the Trion® T120 BGA576 Development Board with a debayer filter design. A Raspberry Pi v2 camera captures video and sends it through the Trion® T120 FPGA's RX interface. The interface processes the video (1920 x 1080 resolution, RAW 10) using 2 MIPI lanes. The T120 FPGA manipulates the image data using an RGB gain filter and debayer filter. The T120 sends the resulting image to the HDMI interface, which you can view using an HDMI monitor.

This example design also illustrates the internal reconfiguration feature of Trion® FPGAs. One design, the golden image, initializes the LVDS to HDMI bridge chip (IT6263). The T120 then reconfigures itself with the debayer design, which controls the video streaming.

Figure 9: Debayer Filter Design Block Diagram



The example design uses the following hardware:

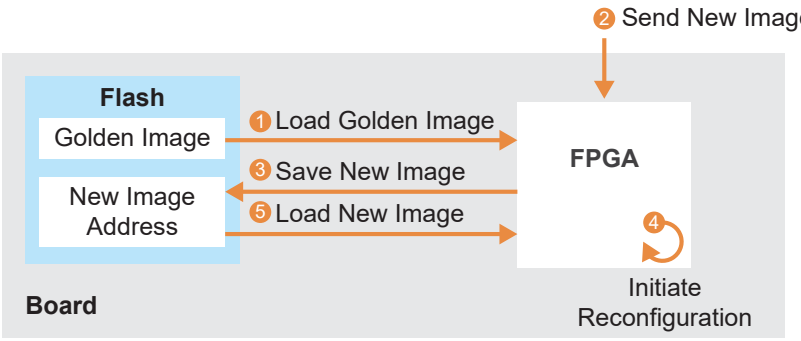
- Trion® T120 BGA576 Development Board
- Raspberry Pi Camera Connector Daughter Card
- Raspberry Pi v2 camera module
- 15-pin flat cable
- 1080p monitor with HDMI connector
- HDMI cable
- 12 V power adapter

About the Internal Reconfiguration Feature

Trion® and Titanium FPGAs have built-in hardware that supports an internal reconfiguration feature in which the FPGA can reconfigure itself from a bitstream image stored in flash memory. This feature is useful for performing system upgrades from a remote location. In these applications, the FPGA is the "brain" that controls the system functionality (that is, there is no microcontroller or CPU).

In a typical reconfiguration flow, the FPGA first configures itself using a "golden" bitstream image as usual. Then, the FPGA receives a new application image remotely, via Ethernet, Wi-Fi, etc., and saves it to flash memory. Then, the FPGA triggers itself to reconfigure using the new image.

Figure 10: Performing Remote Update Using Internal Reconfiguration



Learn more: Refer to AN 010: Using the Internal Reconfiguration Feature to Remotely Update Trion FPGAs for more information.

Example Design Project Files

This Raspberry Pi to HDMI example design has two projects:

- *mipi_pi_cam_debayer_i2c_top*—Golden image for I2C initialization of LVDS-HDMI bridge chip(On board IT6263).
- *mipi_pi_cam_debayer_wo_i2c_top*—Streams data from the Raspberry Pi camera to through the T120 FPGA to the HDMI monitor.

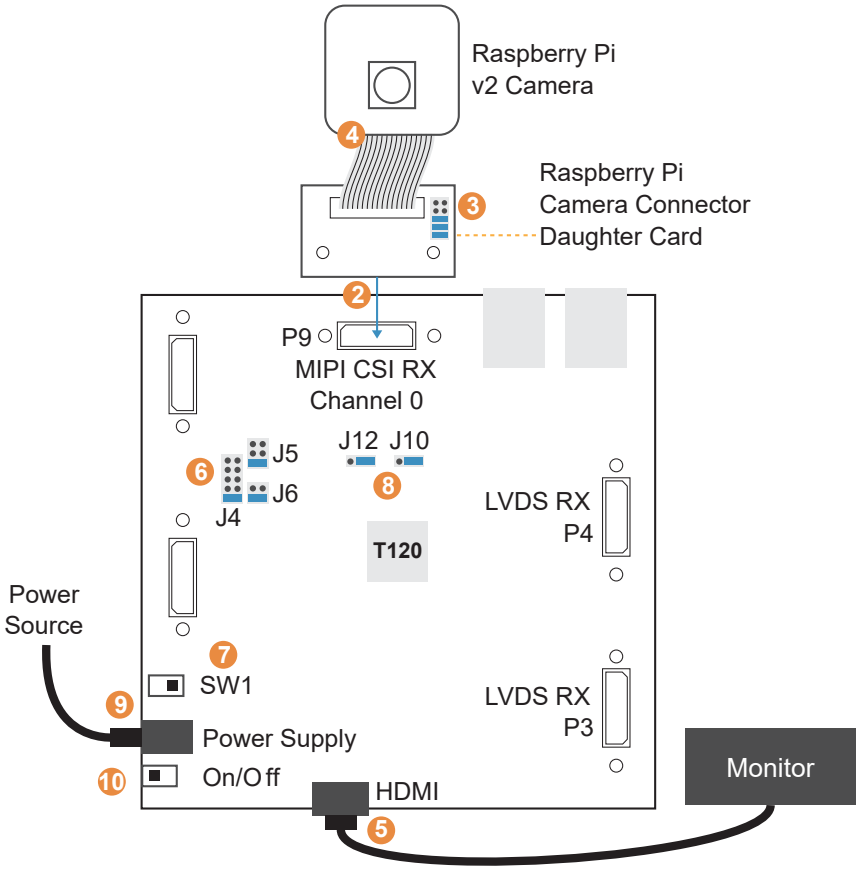
The hex files for these two projects are combined into the **mipi_pi_cam_debayer_preload_top.hex** file, which is pre-loaded onto the development board.

Download: You can download the project files from the Support Center.

Set Up the Hardware

The following figure shows the hardware setup steps:

Figure 11: Hardware Setup



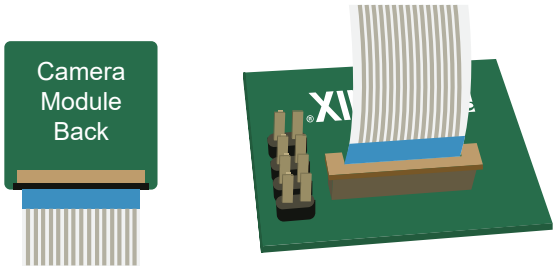
1. Attach standoffs to the board if you have not already done so.
2. Connect the Raspberry Pi Camera Connector Daughter Card to the board.
3. On the daughter card, connect the following pins with jumpers: 1 - 2, 3 - 4, and 5 - 6.
4. Connect the Raspberry Pi v2 camera module to the daughter card using the 15-pin flat cable.
5. Connect the HDMI cable to the HDMI connector and to an HDMI-compatible monitor.
6. Connect jumpers to set the camera power sequence:
   - *VSUP1 (J4)*—Connect pins 5 - 6 or 9 - 10 (default)
   - *VSUP2 (J5)*—Connect pins 5 - 6 (default)
   - *VSUP3 (J6)*—Connect pins 3 - 4 (default)
7. Slide SW1 to position 3, which enables the power up sequence circuit for the MIPI CSI-2 cameras.
8. Use a jumper to connect pins 2 and 3 on J10 and J12 to enable the on-board 10 MHz oscillator.
9. Connect the 12 V power cable to the board connector and to a power source.
10. Turn on the board's power switch.

Connecting the Raspberry Pi Cable

The 15-pin flat cable for the Raspberry Pi camera has a blue stripe on one side.

- When connecting to the camera, the stripe faces away from the camera.
- When connecting to the Raspberry Pi Camera Connector Daughter Card, the stripe faces away from the Efinix® logo.

Figure 12: Connecting Raspberry Pi Cable



Run the Example Design

After the FPGA configures, it outputs video to the monitor.

The design includes the **it6263_reg.mem** file that contains the register mapping for the 1080p resolution. To use a different resolution, modify the register map file. Each line represents the MSB or data.

- Line 1 is the MSB of the 8 bit register.
- Line 2 is the LSB of the 8 bit register.
- Line 3 is the 8-bit data.
- Line 4 is the MSB of the next register, and so on

For example:

```
30
00
01
30
05
01
30
06
00
```

Lines 1, 2, and 3 refer to register 3000 and data 01.

Lines 4, 5, and 6 refer to register 3005 and data 01.

Creating Your Own Design

The Trion® T120 BGA576 Development Board allows you to create and explore designs for the T120 device. Efinix® provides example code and designs to help you get started:

- Our Support Center includes examples targeting the board.
- The Efinity software includes also example designs that you can use as a starting point for your own project, and includes a step-by-step **tutorial**.
- **AN 027: Using the Raspberry Pi to HDMI Example Designs (T120 BGA576)** includes example designs with additional features for Trion® T120 BGA576 Development Board.

Appendix 1: Shared Resources

Some of the resources available on the Trion® T120 BGA576 Development Board are connected to more than one I/Os. You need to ensure there are no overlapping assignments when using these resources. The following table lists the resources shared by more than one I/Os. You can refer to this table to help you plan the resources available in the Trion® T120 BGA576 Development Board

Note: Resources that are not listed are only available from one I/O (see Headers on page 12).

Table 38: Trion® T120 BGA576 Development Board Shared Resources

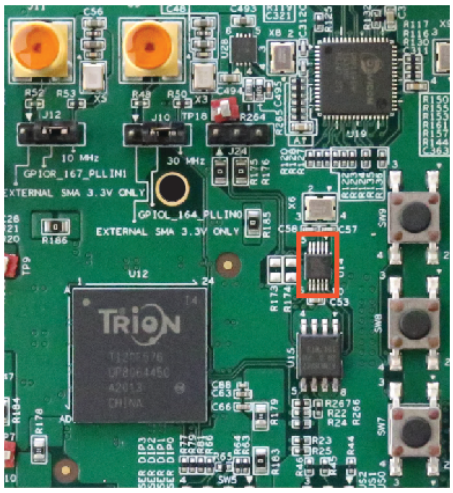
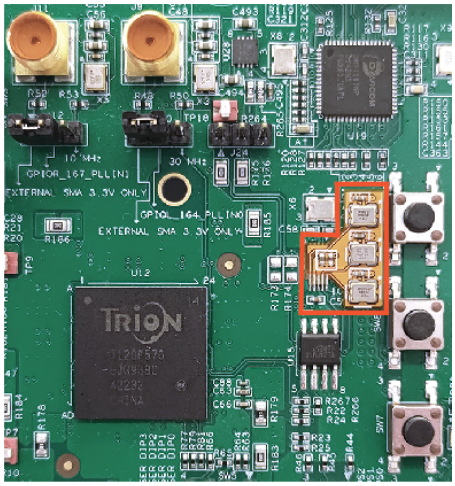
<header name>.<pin name/number>

Resource	Connection 1	Connection 2
GPIOB_RXN21	J13.3	P10.32
GPIOB_RXN22	J13.4	P10.38
GPIOB_RXN23	J13.8	P9.40
GPIOB_RXN24	J13.1	P9.32
GPIOB_RXN25	J14.7	P7.34
GPIOB_RXN26	J14.1	P7.32
GPIOB_RXN27	J14.3	P8.32
GPIOB_RXN28	J14.10	P8.40
GPIOB_RXP21	J13.9	P10.34
GPIOB_RXP22	J13.10	P10.40
GPIOB_RXP23	J13.2	P9.38
GPIOB_RXP24	J13.7	P9.34
GPIOB_RXP25	J14.9	P8.34
GPIOB_RXP26	J14.8	P7.40
GPIOB_RXP27	J14.2	P7.38
GPIOB_RXP28	J14.4	P8.38
GPIOT_RXN20	J15.7	P5.34
GPIOT_RXN21	J15.8	P5.40
GPIOT_RXN22	J15.9	P6.34
GPIOT_RXN23	J15.10	P6.40
GPIOT_RXN24	J16.7	P10.39
GPIOT_RXN27	J16.8	P8.39
GPIOT_RXN28	J16.9	P6.39
GPIOT_RXP20	J15.1	P5.32
GPIOT_RXP21	J15.2	P5.38
GPIOT_RXP22	J15.3	P6.32
GPIOT_RXP23	J15.4	P6.38

Resource	Connection 1	Connection 2
GPIOT_RXP24	J16.1	P9.39
GPIOT_RXP27	J16.2	P7.39
GPIOT_RXP28	J16.3	P5.39
GPIOT_TXN15	J17.9	J23 HDMI.HDMI_PCSDA
GPIOT_TXP15	J17.3	J23 HDMI.HDMI_PCSCL

Appendix 2: Board Revisions

There Trion® T120 BGA576 Development Board has two board revisions, rev. BBA and rev. B1. The following figures illustrate the different parts on the development board.

Rev. BBA (Discontinued)	Rev. B1
	

Revision History

Table 39: Revision History

Date	Version	Description
May 2023	2.3	Corrected hardware set up to include required jumper on header J10. (DOC-1201)
January 2023	2.2	Updated kit part number.
November 2022	2.1	Added Rev. B1 board information. (DOC-973)
September 2022	2.0	Updated Installing Windows Driver.
June 2022	1.9	Added Appendix 1: Shared resources.
December 2021	1.8	Corrected the MIPI and LVDS Expansion Card headers.
September 2021	1.7	Added USB driver installation topics. (DOC-463) Added link to AN: 027 Using the Raspberry Pi to HDMI Example Designs (T120 BGA576) for more example designs.
February 2021	1.6	Added note about referring to the power-up sequence in the data sheet when designing a board and recommending supervisor IC for `CRESET_N` (DOC-388).
December 2020	1.5	Corrected pin numbers in PMOD headers. (DOC-345) Added note about power cable supplied is type A plug (U.S. style). (DOC-345) Updated Raspberry Pi camera connector daughter card header pin names. (DOC-345)
July 2020	1.4	Added a step to connect a jumper on J12 when setting up the example design hardware.
June 2020	1.3	Corrected the jumper settings. Added a topic on how to connect the Raspberry Pi flat cable.
June 2020	1.2	Corrected the number of MIPI lanes used for video processing. Corrected the debayer filter design block diagram.
May 2020	1.1	Updated the example design description.
May 2020	1.0	Initial release.