Titanium Packaging User Guide

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Introduction

Efinix offers Titanium FPGAs in packages that are designed for the devices' maximum number of user's I/O pins. This document describes the Titanium FPGAs' pin and package specifications as well as solder reflow guidelines.

Learn more: Refer to the following documents for more information:
FPGA pinout specification
FPGA data sheet for pin definitions

Available Package Options

Table 1: Titanium Package Options

Package	Pitch (mm)	Size (mm)	Ti35	Ti60	Ti90	Ti120	Ti165	Ti180	Ti240	Ti375
64-ball WLCSP	0.4	3.5x3.4		✓						
100-ball FBGA	0.5	5.5x5.5	✓	✓						
225-ball FBGA	0.65	10x10	✓	✓						
256-ball FBGA	0.8	13x13	✓	✓						
361-ball FBGA	0.65	13x13			✓	✓		✓		
400-ball FBGA	0.8	16x16			✓	✓		✓		
484-ball FBGA	0.8	18x18			✓	✓		✓		✓
529-ball FBGA	0.8	19x19			✓	✓	✓	✓	✓	✓
1156-ball FBGA	1.0	35x35					✓		✓	✓

Refer to the FPGA data sheet for information on the number of GPIO and other resources in each FPGA/package combination.

Device Pinout File

Efinix provides pinout files for Titanium FPGAs. For each device/package combination, these files contain the pin name, I/O bank number for each pin, configuration function, and pin location.

Download: Download the pinout files from the Documentation page in the Support section of the Efinix® web site (www.efinixinc.com/support)

Pinout Description

The following tables describe the pinouts for power, ground, configuration, and interfaces.

Table 2: Power and Ground Pinouts

xx indicates the bank location.

Function	Description
VCC	Core power supply.
VCCA_*xx*	PLL analog power supply.
VDD_SOC	Hardened RISC-V block power supply.
VCCAUX	1.8 V auxiliary power supply.
VCCIO33_*xx*	HVIO bank power supply.
VCCIO33_*xx*_*yy*_*zz*	Power for HVIO banks that are shorted together. *xx*, *yy*, and *zz* are the bank locations. For example: VCCIO33_BR1_BR2 shorts banks BR1 and BR2.
VCCIO*xx*	HSIO bank power supply.
VCCIO*xx*_*yy*_*zz*	Power for HSIO banks that are shorted together. *xx*, *yy*, and *zz* are the bank locations. For example: VCCIO1B_1C shorts banks 1B and 1C
VQPS	1.8 V supply for security fuse. During configuration and normal operation, keep this pin at 0 V. When you want to blow the security fuses, power this pin up to 1.8 V.
GND	Ground.

Table 3: GPIO Pinouts

x indicates the location (T, B, L, or R); *xx* indicates the bank location; *n* indicates the number; *yyyy* indicates the function.

Function	Direction	Description
GPIO*x*_*n*	I/O	HVIO for user function. User I/O pins are single-ended.
GPIO*x*_*n*_*yyyy*	I/O	HVIO or multi-function pin.
GPIO*x*_N_*n* GPIO*x*_P_*n*	I/O	HSIO transmitter, receiver, or both.
GPIO*x*_N_*n*_*yyyy* GPIO*x*_P_*n*_*yyyy*	I/O	HSIO transmitter, receiver, both, or multi-function.

Function	Direction	Description
REF_RES_*xx*	–	REF_RES is a reference resistor to generate constant current for the related circuits. Connect the following REF_RES pins to ground through a 10 kΩ resistor with a tolerance of ±1% : • REF_RES_ 2A and REF_RES_4A pins must be connected. • REF_RES pin of the particular bank, if pins in the bank are used as LVDS TX or MIPI TX lane. • REF_RES_3A pin, if internal oscillator is used. • REF_RES_3A pin, if blowing of fuses for FPGA security is required. You can leave the REF_RES pins floating if none of the above are applicable. Connect the following REF_RES pins to ground through a 10 kΩ resistor with a tolerance of ±1% : • REF_RES_ 2A, REF_RES_2C, REF_RES_4A, and REF_RES_4C pins must be connected. • REF_RES pin of the particular bank, if pins in the bank are used as LVDS TX or MIPI TX lane. • REF_RES_3A pin, if the internal oscillator is used. • REF_RES_3A pin, if blowing of fuses for FPGA security is required. You can leave the REF_RES pins floating if none of the above are applicable. Connect all REF_RES pins to ground through a 10 kΩ resistor with a tolerance of ±1%.

Table 4: Alternate Function Pinouts

n is the number.

Function	Direction	Description
CLK*n*	Input	Single ended input for global clock and control network resource. The number of inputs is package dependent.
CLK*n*_P/N	Input	Differential input pair for global clock and control network resource. P pins can access to global clock and control network resource if it is in single-ended configuration.
EXTFB	Input	PLL external feedback CLKIN.
PLLIN*n*	Input	PLL reference clock resource. The number of reference clock resources is package dependent.

Configuration Pins

Some configuration pins are dedicated, and some are dual-purpose.

- Dedicated pins cannot be used as general purpose I/O.
- During configuration, use dual-purpose pins as described in this document for the configuration mode you are using. After configuration (in user mode), you can use these pins as general-purpose I/O.

Table 5: Dedicated Configuration Pins

These pins cannot be used as general-purpose I/O after configuration.

All the pins are in internal weak pull-up during configuration mode except for `TCK` and `TDO`.

Calculate the resistor value as described in **Resistors in Configuration Circuitry** in **AN 033: Configuring Titanium FPGAs**.

Pins	Direction	Description	External Weak Pull Up/ Pull Down Requirement
CDONE	I/O	Configuration done status pin. CDONE is an open drain output; connect it to an external pull-up resistor to VCCIO. When CDONE = 1, the configuration is complete and the FPGA enters user mode. You can hold CDONE low and release it to synchronize the FPGAs entering user mode.	Pull up
CRESET_N	Input	Active-low FPGA reset and re-configuration trigger. Pulse CRESET_N low for a duration of t_{creset_N} before releasing CRESET_N from low to high to initiate FPGA re-configuration. This pin does not perform a system reset.	Pull up
TCK	Input	JTAG test clock input (TCK). The rising edge loads signals applied at the TAP input pins (TMS and TDI). The falling edge clocks out signals through the TAP TDO pin.	Pull up
TMS	Input	JTAG test mode select input (TMS). The I/O sequence on this input controls the test logic operation . The signal value typically changes on the falling edge of TCK. TMS is typically a weak pull-up; when it is not driven by an external source, the test logic perceives a logic 1.	Pull up
TDI	Input	JTAG test data input (TDI). Data applied at this serial input is fed into the instruction register or into a test data register depending on the sequence previously applied at TMS. Typically, the signal applied at TDI changes state following the falling edge of TCK while the registers shift in the value received on the rising edge. Like TMS, TDI is typically a weak pull-up; when it is not driven from an external source, the test logic perceives a logic 1.	Pull up
TDO	Output	JTAG test data output (TDO). This serial output from the test logic is fed from the instruction register or a test data register depending on the sequence previously applied at TMS. The shift out content is based on the issued instruction. The signal driven through TDO changes state following the falling edge of TCK. When data is not being shifted through the device, TDO is set to an inactive drive state (e.g., high-impedance).	Pull up
JTAG_VCCIO_SEL	Input	JTAG voltage select pin. This pin affects the BR4 bank voltage, or any banks merged with the BR4 bank. Supply VCCIO33_BR4 with 1.8 V and connect a 1 kΩ external resistor between this pin and ground to use JTAG at 1.8 V. Leave this pin floating to use the default JTAG at 3.3 V or 2.5 V. Available on Ti85, Ti135, Ti165, Ti240, and Ti375 FPGAs only.	Floating or pull down

(1) CDONE has a drive strength of 12 mA at 1.8 V.

Table 6: Dual-Purpose Configuration Pins

In user mode (after configuration), you can use these dual-purpose pins as general I/O.

Calculate the resistor value as described in **Resistors in Configuration Circuitry** in **AN 033: Configuring Titanium FPGAs**.

Configuration Functions	Direction	Description	External Weak Pull Up/ Pull Down Requirement
CBSEL[1:0]	Input	Multi-image configuration selection pin. This function is not applicable to single-image bitstream configuration or internal reconfiguration (remote update). Connect CBSEL[1:0] to the external resistors for the image you want to use: 00 for image 1 01 for image 2 10 for image 3 11 for image 4 0: Connect to an external weak pull down. 1: Connect to an external weak pull up.	Pull up or pull down
CCK	I/O	Passive SPI input configuration clock or active SPI output configuration clock.	Optional pull up if required by external load
CDI*n*	I/O	Data input for SPI configuration. *n* is a number from 0 to 31 depending on the SPI configuration data width. CDI0 is an output in x1 active configuration mode and is a bidirectional pin in all other active configuration modes. CDI4 is a bidirectional pin in x8 active configuration mode. In a multi-bit daisy chain connection, CDI[31:0] connects to the data bus in parallel.	Optional pull up if required by external load
CSI	Input	Chip select. 0: The FPGA is not selected or enabled and will not be configured. 1: Select the FPGA for allSPI configuration modes. Ti35 and Ti60 FPGAs require this setting for JTAG configuration mode. This pin is not bonded out in some of the smaller packages, such as the W64, F100S3F2, and F100.	Pull up
CSO	Output	Chip select output. Asserted after configuration is complete. Connect this pin to the chip select pin of the next FPGA for daisy chain configuration. [2] This pin is not bonded out in some of the smaller packages, such as the F100.	-
NSTATUS	Output	Indicates a configuration error. When the FPGA drives this pin low, it indicates an ID mismatch, the bitstream CRC check has failed, or remote update has failed.	-

[2] Cascaded configuration is not supported in the F100S3F2 package.

Configuration Functions	Direction	Description	External Weak Pull Up/ Pull Down Requirement
SSL_N	I/O	SPI configuration mode select. The FPGA senses the value of SSL_N when it comes out of reset (i.e., CRESET_N transitions from low to high). 0: Passive mode; connect to external weak pull down. 1: Active mode; connect to external weak pull up. In active configuration mode, SSL_N is an active-low chip select to the flash device (CDI0 - CDI3).	Pull up or pull down
SSU_N	Output	Active-low chip select to the upper flash device (CDI4 - CDI17) in active x8 configuration mode (dual quad mode). Not available on W64, F100S3F2, and F100 packages.	Optional pull up if required by external load
EXT_CONFIG_CLK	Input	Alternative clock in active configuration mode.	Optional pull up if required by external load
TEST_N	Input	Active-low test mode enable signal. Set to 1 to disable test mode. During all configuration modes, rely on the external weak pull-up or drive this pin high.	Pull up

Note: Refer to the column Configuration Functions in the pinout file.

Dedicated DDR Pinout

Table 7: Dedicated DDR Pinout

n indicates the number.

Function	Direction	Description
DDR_A[*n*]	Output	Address signals to the memories.
DDR_CKE	Output	Active-high clock enable signals to the memories.
DDR_CK DDR_CK_N	Output	Differential clock output pins to the memories.
DDR_CS_N	Output	Active-low chip select signals to the memories.
DDR_DQ[*n*]	I/O	Data bus to/from the memories.
DDR_DM[*n*]	I/O	Active-high data-mask signals to the memories.
DDR_DQS[*n*] DDR_DQS_N[*n*]	I/O	Differential data strobes to/from the memories.
DDR_RST_N	Output	Active-low reset signals to the memories.
DDR_CAL	Input	240 Ω to ground reference resistor port.
VDD_PHY_DDR*n*	-	DDR digital power supply.
VDDQ_PHY_DDR*n*	-	DDR I/O power supply.
VDDQX_PHY_DDR*n*	-	DDR I/O pre-driver power supply.
VDDPLL_MCB_TOP_PHY_DDR*n*	-	DDR PLL power supply.
VDDQ_CK_PHY_DDR*n*	-	DDR I/O power supply for clock.

Dedicated MIPI D-PHY Pinout

Table 8: Dedicated MIPI D-PHY Pinout

m and *n* indicates the number. *L* indicates the lane

Function	Direction	Description
VCC18A_MIPI*m*_*n*_TX	-	Power supply for the MIPI D-PHY TX block. *m* and *n* are the MIPI channel numbers. For example: VCC18A_MIPI0_1_TX displays the power of MIPI D-PHY TX channel 0 and channel 1 being shorted together.
VCC18A_MIPI*m*_*n*_RX	-	Power supply for the MIPI D-PHY RX block. *m* and *n* are the MIPI interface numbers. For example: VCC18A_MIPI0_1_RX displays the power of MIPI D-PHY RX channel 0 and channel 1 being shorted together.
MIPI*n*_TXDP*L* MIPI*n*_TXDN*L*	I/O	MIPI differential transmit data lane.
MIPI*n*_RXDP*L* MIPI*n*_RXDN*L*	I/O	MIPI differential receive data lane.

Table 9: Dedicated MIPI D-PHY Pinouts

n indicates the number. *L* indicates the lane

Function	Direction	Description
VCC18A_MIPI*n*_TX	-	Power supply for the MIPI D-PHY TX block.
VCC18A_MIPI*n*_RX	-	Power supply for the MIPI D-PHY RX block.
MIPI*n*_TXDP*L* MIPI*n*_TXDN*L*	Output	MIPI differential transmit data lane.
MIPI*n*_RXDP*L* MIPI*n*_RXDN*L*	Input	MIPI differential receive data lane.

Dedicated Transceiver Pinout

Table 10: Dedicated Transceiver Pinout

n indicates the bank number; *L* indicates the lane; *nn* indicates the merged transceiver bank numbers.

Function	Direction	Description
VCC_SERDES*nn*	-	Transceiver digital PCS and PCIe controller power supplies.
VDDA_C_Q*nn*	-	Transceiver analog bias power supply.
VDDA_D_Q*nn*	-	Transceiver digital and analog data path power supplies.
VDDA_H_Q*nn*	-	Transceiver analog power supply for I/O.
PERST_Q*n*_N	Input	Active-low PCIe reset pin.
Q*n*_CAL_RES	Input	Transceiver calibration resistor. Connect an external resistor between this pin and ground. The resistor value is 3.01 kΩ with 1% tolerance.
Q*n*_REFCLK*n*_N Q*n*_REFCLK*n*_P	Input	Transceiver differential external reference clock input. REFCLK0: Main clock. REFCLK1: Alternative clock.
Q*n*_RXDP*L* Q*n*_RXDN*L*	Input	Transceiver differential receive serial data inputs. Q0 and Q2 include the PCIe controller.
Q*n*_TXDP*L* Q*n*_TXDN*L*	Output	Transceiver differential transmitter serial data inputs Q0 and Q2 include the PCIe controller.

64-Ball WLCSP Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

Figure 1: 64-Ball WLCSP Pinout Diagram

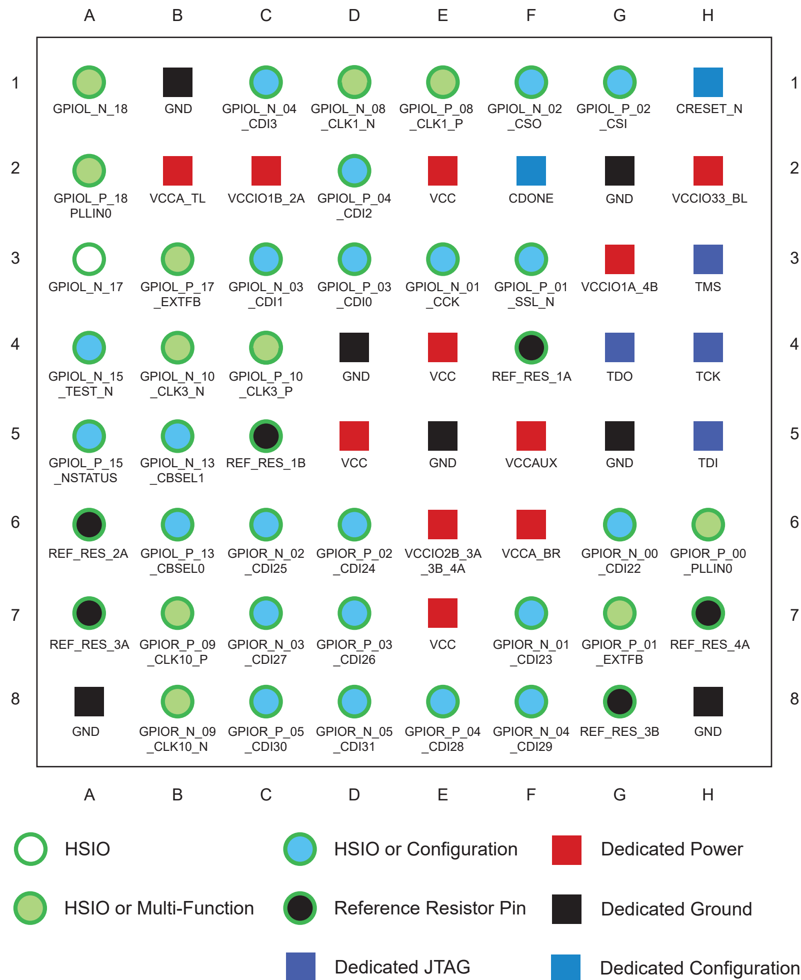


Figure 2: 64-Ball WLCSP I/O Bank Diagram

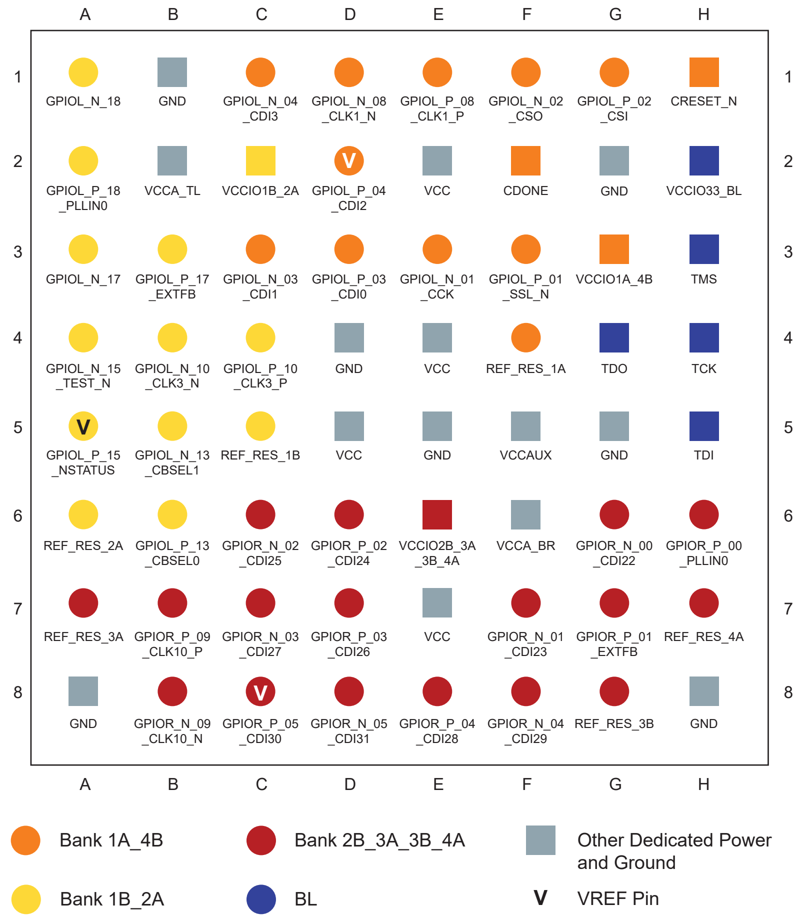


Figure 3: 64-Ball WLCSP Emulated MIPI RX Groups

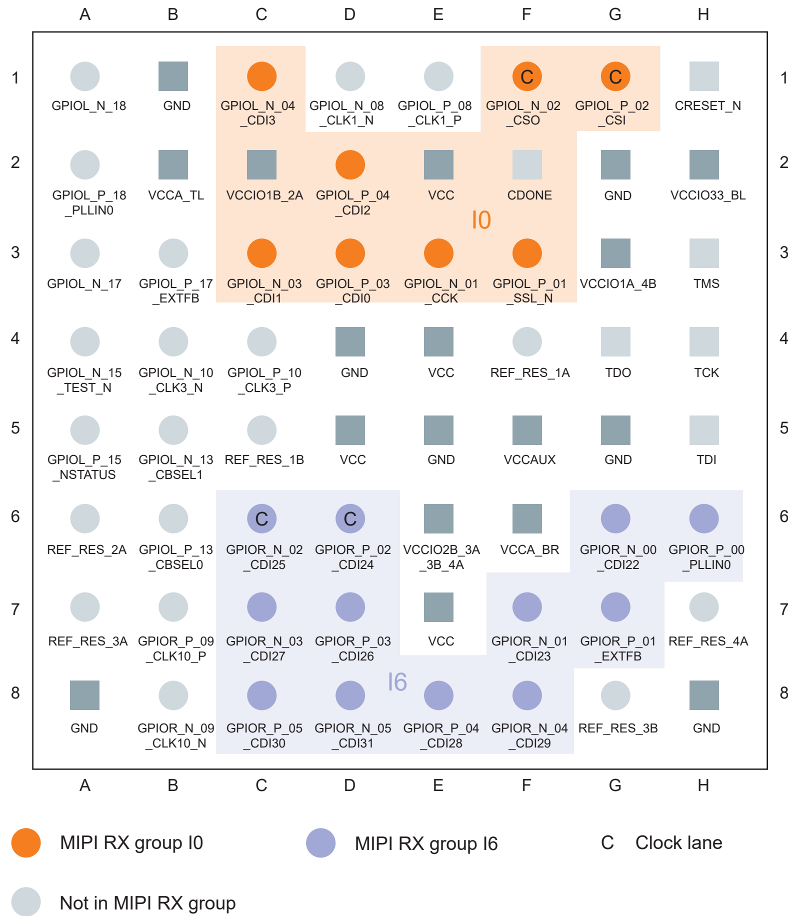


Figure 4: 64-Ball WLCSP Package Marking

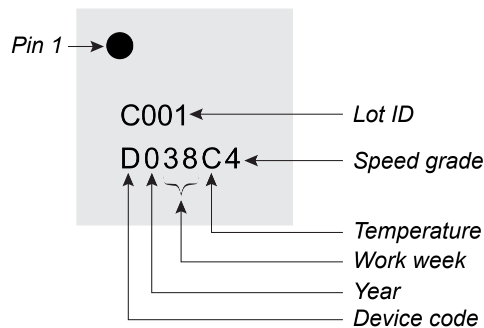
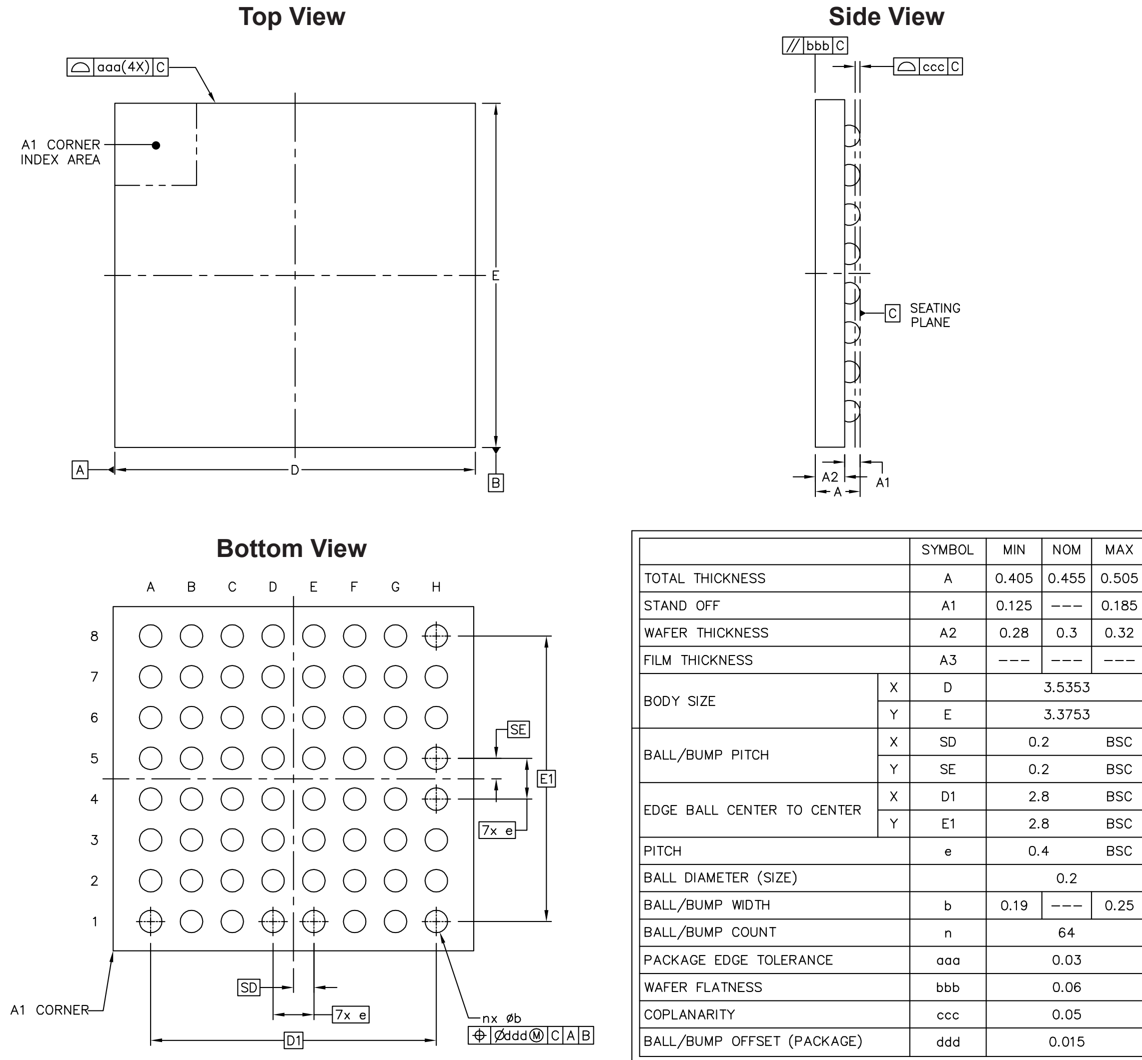


Figure 5: 64-Ball WLCSP Package Outline



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.405	0.455	0.505
STAND OFF		A1	0.125	---	0.185
WAFER THICKNESS		A2	0.28	0.3	0.32
FILM THICKNESS		A3	---	---	---
BODY SIZE	X	D	3.5353		
	Y	E	3.3753		
BALL/BUMP PITCH	X	SD	0.2		BSC
	Y	SE	0.2		BSC
EDGE BALL CENTER TO CENTER	X	D1	2.8		BSC
	Y	E1	2.8		BSC
PITCH		e	0.4		BSC
BALL DIAMETER (SIZE)				0.2	
BALL/BUMP WIDTH		b	0.19	---	0.25
BALL/BUMP COUNT		n		64	
PACKAGE EDGE TOLERANCE		aaa		0.03	
WAFER FLATNESS		bbb		0.06	
COPLANARITY		ccc		0.05	
BALL/BUMP OFFSET (PACKAGE)		ddd		0.015	

100-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

F100S3F2 Package Specifications

Important: For devices with the letter 'S' in the lot number, pin A5 has the `VQPS` function. For devices without the letter 'S' in the lot number, pin A5 has the `GND` function. See PCN-2405-001 for details.

Figure 6: 100-Ball FBGA Pinout Diagram

	1	2	3	4	5	6	7	8	9	10
A	GND	VCCA_TL	REF_RES_1B	GPIOT_P_01	VQPS_GND	VCCIO2A_2B	VCCA_TR	GND	GPIOR_P_19_PLLIN0	GPIOR_N_19
B	GPIOL_P_13_CBSEL0	GPIOL_N_18	GPIOL_P_18_PLLIN0	GPIOL_P_17_EXTFB	REF_RES_2A	VCCAUX	REF_RES_3A	GPIOR_N_13	GPIOR_P_14	GPIOR_N_14
C	GPIOL_N_13_CBSEL1	GPIOL_N_12	GPIOL_P_12	GPIOL_N_17	GPIOL_P_15_NSTATUS	VCC	GPIOR_N_10_CLK9_N	GPIOR_P_13	VCCIO3A	GPIOR_N_12
D	GPIOL_N_10_CLK3_N	GND	VCCIO1B	GND	GPIOL_N_15_TEST_N	GPIOR_P_10_CLK9_P	VCC	GPIOR_P_11_CLK8_P	GPIOR_N_11_CLK8_N	GPIOR_P_12
E	GPIOL_P_10_CLK3_P	GPIOL_P_11	GPIOL_N_11	GPIOL_P_08_CLK1_P	GPIOL_N_08_CLK1_N	VCC	GPIOR_N_08_CLK11_N	GPIOR_P_09_CLK10_P	GPIOR_N_09_CLK10_N	GND
F	GPIOL_N_06	GPIOL_N_09_CLK2_N	GPIOL_P_09_CLK2_P	GPIOL_P_07_CLK0_P	GPIOL_N_07_CLK0_N	VCC	GPIOR_P_08_CLK11_P	GPIOR_N_07	GPIOR_P_06_CDI20	GPIOR_N_06_CDI21
G	GPIOL_P_06	VCCIO1A_4B	GPIOL_N_05	GPIOL_P_05	VCC	VCCAUX	GND	GPIOR_P_07	VCCIO3B_4A	GPIOR_N_04_CDI29
H	GPIOL_N_03_CDI1	GPIOL_P_03_CDI0	CDONE	REF_RES_1A	GPIOR_N_00_CDI22	GPIOR_P_03_CDI26	VCC	GPIOR_N_05_CDI31	GPIOR_P_05_CDI30	GPIOR_P_04_CDI28
J	GPIOL_P_01_SSL_N	GPIOL_N_01_CCK	VCCIO33_BL	TDO	GPIOR_P_00_PLLIN0	GPIOR_N_03_CDI27	GPIOR_N_02_CDI25	GPIOR_P_02_CDI24	GND	GPIOR_N_01_CDI23
K	CRESET_N	GND	TCK	TMS	TDI	GND	VCCA_BR	REF_RES_4A	REF_RES_3B	GPIOR_P_01_EXTFB

Legend:
- HVIO
- HSIO
- HSIO or Configuration
- Dedicated Power
- HVIO or Multi-Function
- HSIO or Multi-Function
- Reference Resistor Pin
- Dedicated Ground
- VQPS_GND
- Dedicated JTAG
- Dedicated Configuration

Figure 7: 100-Ball FBGA I/O Bank Diagram

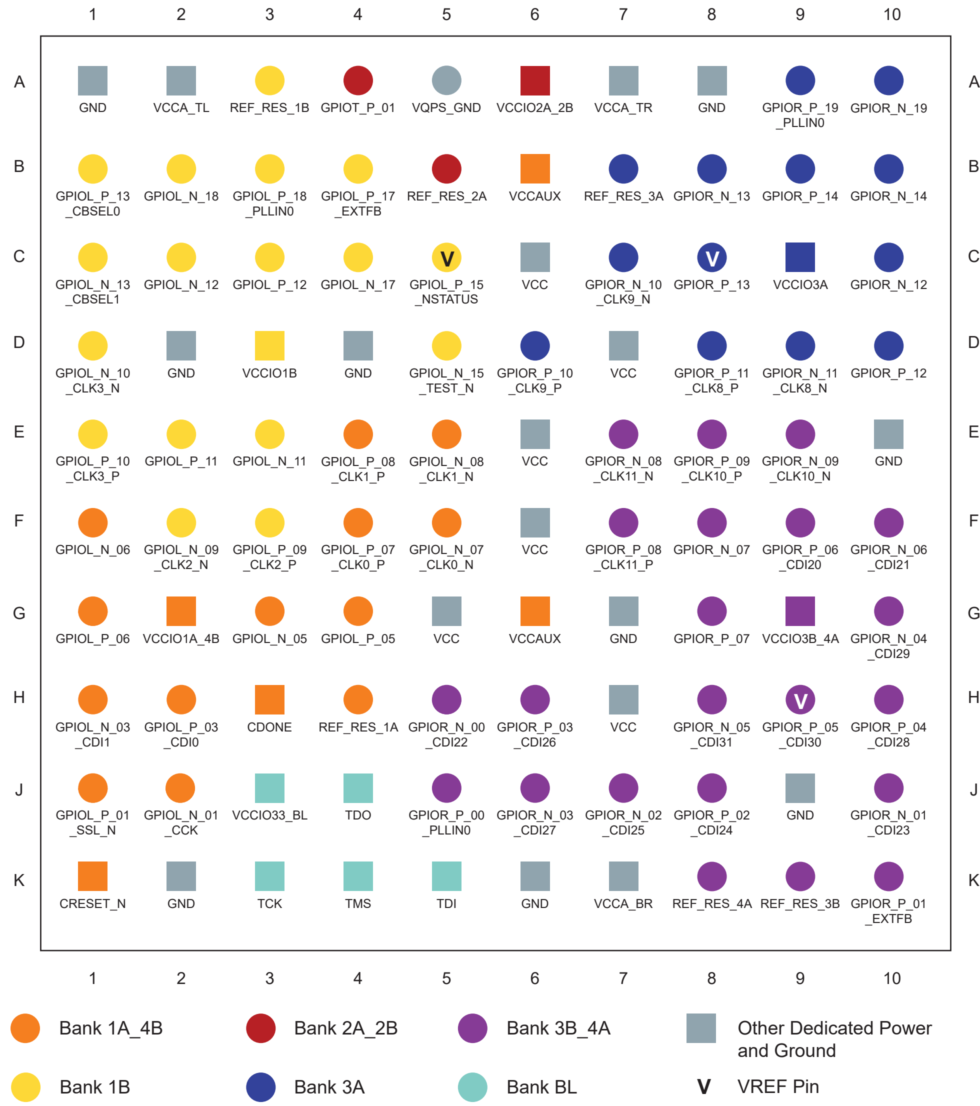


Figure 8: 100-Ball FBGA Emulated MIPI RX Groups

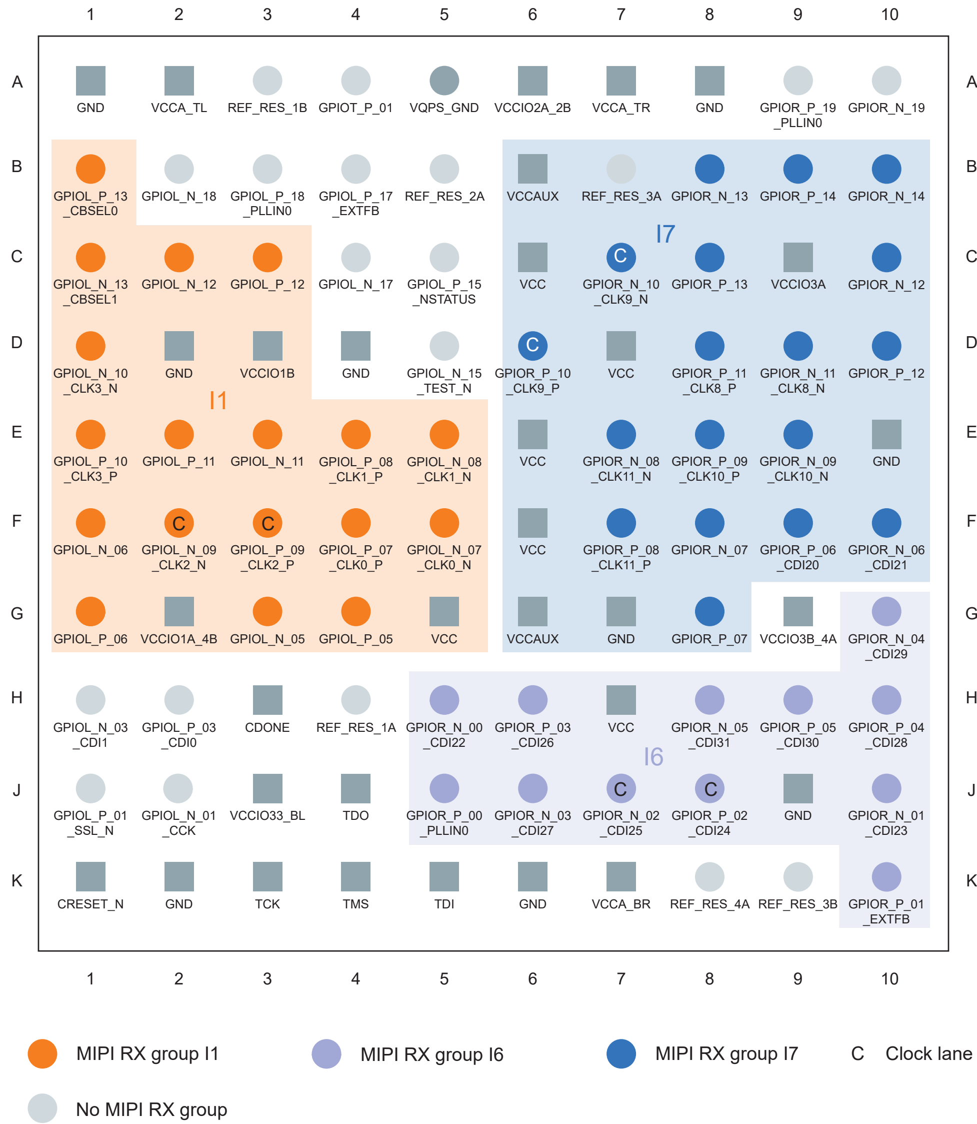


Figure 9: 100-Ball FPGA Package Marking

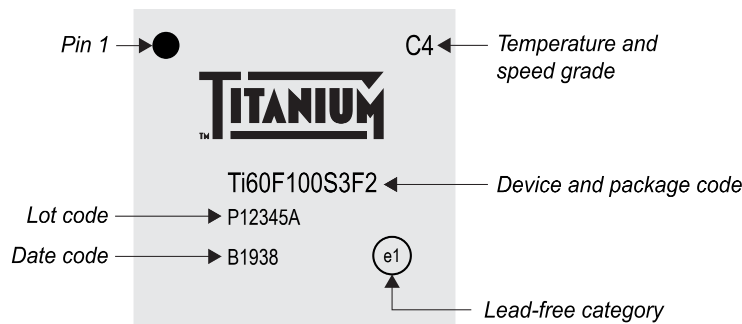
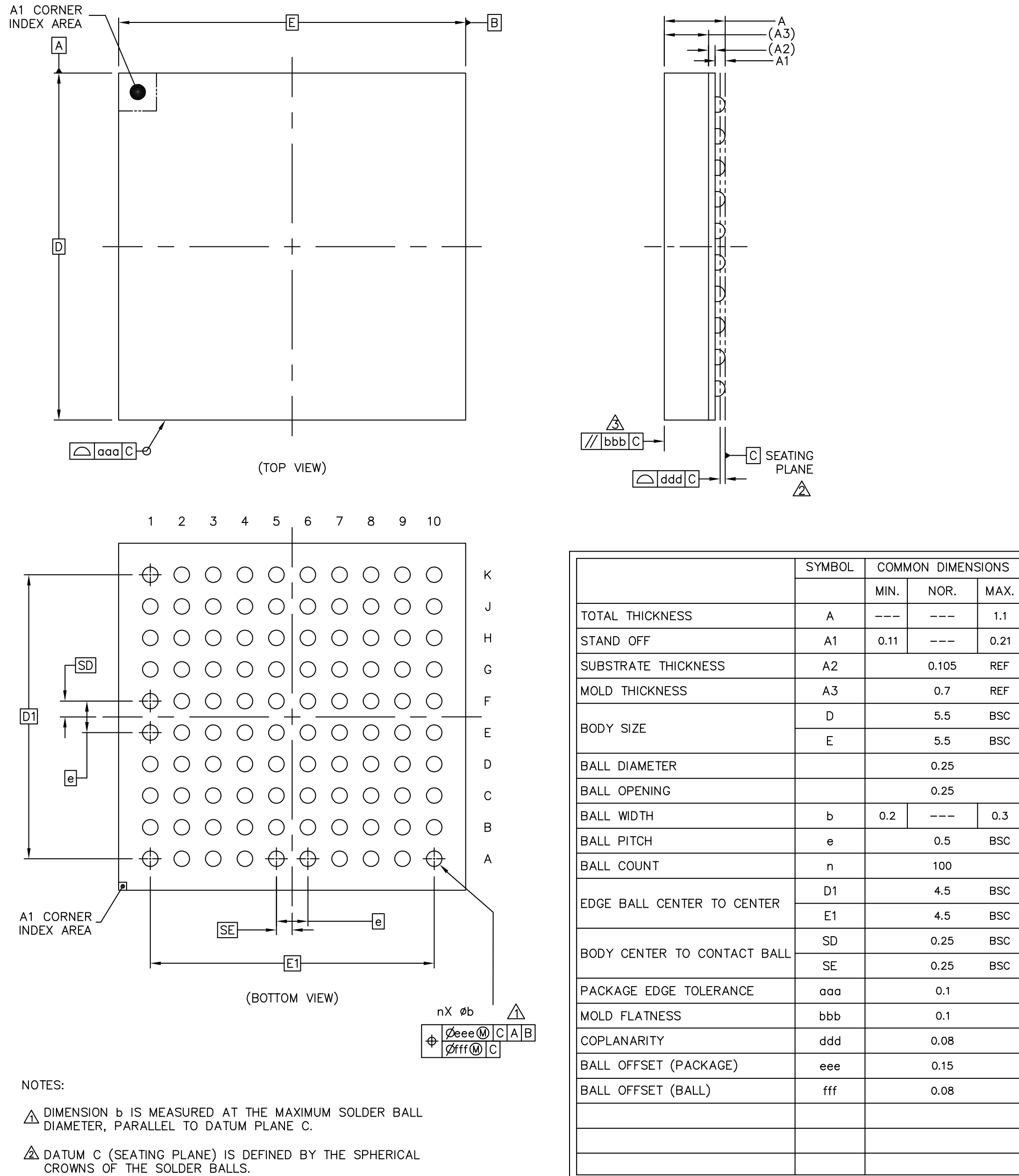


Figure 10: 100-Ball FBGA Package Outline



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1.1
STAND OFF	A1	0.11	---	0.21
SUBSTRATE THICKNESS	A2		0.105	REF
MOLD THICKNESS	A3		0.7	REF
BODY SIZE	D		5.5	BSC
	E		5.5	BSC
BALL DIAMETER			0.25	
BALL OPENING			0.25	
BALL WIDTH	b	0.2	---	0.3
BALL PITCH	e		0.5	BSC
BALL COUNT	n		100	
EDGE BALL CENTER TO CENTER	D1		4.5	BSC
	E1		4.5	BSC
BODY CENTER TO CONTACT BALL	SD		0.25	BSC
	SE		0.25	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

F100 Package Specifications

The F100 package is similar to the F100S3F2 package in terms of pin, I/O bank locations, package top-side marking, and outlines. You can refer to the F100S3F2 package for reference. However, pin A5 in the F100 package is named `VQPS` for all lot numbers.

225-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

Note: Refer to the F225 Escape Routing on page 84 for an escape routing example.

Important: For devices with the letter 'S' in the lot number, pin G6 has the `VQPS` function. For devices without the letter 'S' in the lot number, pin G6 has the `GND` function. See PCN-2405-001 for details.

Figure 11: 225-Ball FBGA Pinout Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	GND	GPIOL_N_18	GPIOL_03	GPIOL_09	GPIOT_P_03	GPIOT_N_03	GPIOT_N_06	GPIOT_N_07_CLK4_N	GPIOT_N_11	GPIOT_P_14	GPIOT_P_17_PLLIN1	GPIOR_13	GPIOR_12	GPIOR_19	GND
B	GPIOL_P_17_EXTFB	GPIOL_P_18_PLLIN0	GPIOL_04	VCCIO33_TL	GPIOL_10	GPIOT_P_01	GPIOT_P_06	GPIOT_P_07_CLK4_P	GPIOT_P_11	GPIOT_N_14	GPIOT_N_17	GPIOR_15	VCCIO33_TR	GPIOR_18	REF_RES_3A
C	GPIOL_N_16	GPIOL_N_17	GPIOL_06	GPIOL_07	GPIOL_11_PLLIN2	GPIOT_N_01	VCCIO2A	GPIOT_P_10_CLK7_P	GPIOT_N_10_CLK7_N	GPIOT_P_13	VCCIO2B	GPIOR_16	GPIOR_P_17	GPIOR_P_19_PLLIN0	GPIOR_N_19
D	GPIOL_P_16	VCCIO1B	GND	VCCAUX	GPIOT_N_00	VCCIO2A	GPIOT_N_05	GPIOT_N_09_CLK6_N	VCCIO2B	GPIOT_N_13	REF_RES_2B	GPIOR_20	GPIOR_N_17	GPIOR_N_18	GPIOR_P_18
E	GPIOL_P_15_NSTATUS	GPIOL_N_15_TEST_N	GPIOL_N_13_CBSEL1	REF_RES_1B	VCCA_TL	GPIOT_P_00_PLLIN1	GPIOT_P_05	GPIOT_P_09_CLK6_P	GPIOT_N_12	GPIOT_P_16_EXTFB	VCCAUX	GPIOR_N_15	VCC	GPIOR_N_16	GPIOR_P_16
F	GPIOL_P_14	GPIOL_N_14	GPIOL_P_13_CBSEL0	VCCIO1B	GPIOL_N_11	REF_RES_2A	GPIOT_P_04	GPIOT_N_04	GPIOT_P_12	GPIOT_N_16	GPIOR_N_14	GPIOR_P_15	GPIOR_N_12	VCCIO3A	GPIOR_N_13
G	GPIOL_N_09_CLK2_N	GPIOL_N_10_CLK3_N	GPIOL_P_12	GPIOL_N_12	GPIOL_P_11	VQPS	VCC	GND	VCC	VCCA_TR	GPIOR_P_14	VCCIO3A	GPIOR_P_12	GPIOR_N_11_CLK8_N	GPIOR_P_13
H	GPIOL_P_09_CLK2_P	GPIOL_P_10_CLK3_P	GPIOL_N_08_CLK1_N	GPIOL_N_04_CDI3	GPIOL_P_04_CDI2	VCC	GND	VCC	GND	GPIOR_P_08_CLK11_P	GPIOR_N_08_CLK11_N	GPIOR_N_10_CLK9_N	GPIOR_P_10_CLK9_P	GPIOR_P_11_CLK8_P	GPIOR_N_09_CLK10_N
J	GPIOL_N_07_CLK0_N	GPIOL_P_08_CLK1_P	GPIOL_N_05	VCCIO1A	CRESET_N	GND	VCC	GND	VCC	GPIOR_N_03_CDI27	VCCIO3B	GPIOR_N_04_CDI29	GPIOR_N_06_CDI21	GPIOR_N_07	GPIOR_P_09_CLK10_P
K	GPIOL_P_07_CLK0_P	GPIOL_N_06	GPIOL_P_06	GPIOL_P_05	REF_RES_1A	GPIOB_N_04	GPIOB_P_09_CLK13_P	GPIOB_P_11_CDI10	GPIOB_N_11_CDI11	GPIOR_P_03_CDI26	GPIOR_N_00_CDI22	GPIOR_P_04_CDI28	GPIOR_P_06_CDI20	GPIOR_P_07	GPIOR_N_05_CDI31
L	GPIOL_N_03_CDI1	VCCIO1A	CDONE	VCCAUX	VCCA_BL	GPIOB_P_04_SSU_N	GPIOB_N_06_CDI9	GPIOB_N_09_CLK13_N	GPIOB_N_10_CLK12_N	VCCA_BR	GPIOR_P_00_PLLIN0	GPIOR_P_01_EXTFB	GPIOR_N_01_CDI23	VCCIO3B	GPIOR_P_05_CDI30
M	GPIOL_P_03_CDI0	GPIOL_N_02_CSO	VCC	TDO	REF_RES_4B	GPIOB_N_03_CDI7	GPIOB_P_06_CDI8	GPIOB_N_08_CLK14_N	GPIOB_P_10_CLK12_P	GPIOB_N_13_CDI15	VCCAUX	REF_RES_3B	GND	GPIOR_P_02_CDI24	GPIOR_N_02_CDI25
N	GPIOL_N_01_CCK	GPIOL_P_02_CSI	TMS	TCK	VCCIO4B	GPIOB_P_03_CDI6	VCCIO4B	GPIOB_P_08_CLK14_P	VCCIO4A	GPIOB_P_13_CDI14	VCCIO4A	REF_RES_4A	GPIOR_24	GPIOR_21	VCCIO33_BR
P	GPIOL_P_01_SSL_N	GPIOL_P_00_PLLIN0	TDI	VCCIO33_BL	GPIOB_N_00	GPIOB_N_01	GPIOB_N_02_CDI5	GPIOB_N_07_CLK15_N	GPIOB_N_12_CDI13	GPIOB_N_14_CDI17	GPIOB_P_17_PLLIN1	GPIOB_N_17	GPIOR_27	GPIOR_22	GPIOR_25
R	GND	GPIOL_N_00	GPIOL_01	GPIOL_02	GPIOB_P_00_PLLIN1	GPIOB_P_01_EXTFB	GPIOB_P_02_CDI4	GPIOB_P_07_CLK15_P	GPIOB_P_12_CDI12	GPIOB_P_14_CDI16	GPIOB_N_15_CDI19	GPIOB_P_15_CDI18	GPIOR_29_PLLIN2	GPIOR_28	GND

Legend: HVIO; HSIO; HSIO or Configuration; Dedicated Power; Dedicated Configuration; HVIO or Multi-Function; HSIO or Multi-Function; Reference Resistor Pin; Dedicated Ground; Dedicated JTAG; VQPS

Figure 12: 225-Ball FBGA I/O Bank Diagram

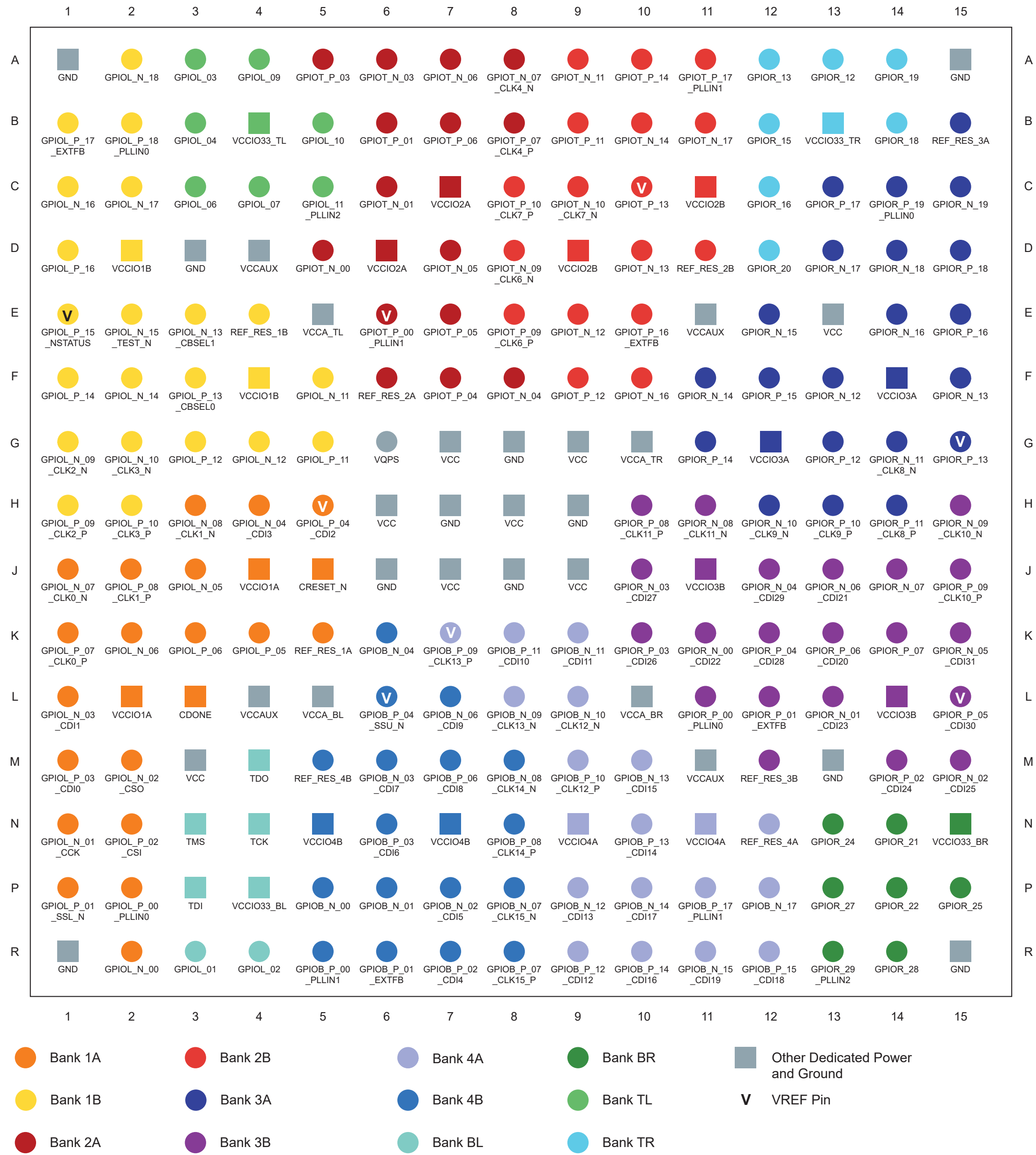


Figure 13: 225-Ball FBGA Emulated MIPI RX Groups

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	GND	GPIOL_N_18	GPIOL_03	GPIOL_09	GPIOT_P_03	GPIOT_N_03	GPIOT_N_06	GPIOT_N_07_CLK4_N	GPIOT_N_11	GPIOT_P_14	GPIOT_P_17_PLLIN1	GPIOR_13	GPIOR_12	GPIOR_19	GND
B	GPIOL_P_17_EXTFB	GPIOL_P_18_PLLIN0	GPIOL_04	VCCIO33_TL	GPIOL_10	GPIOT_P_01	GPIOT_P_06	GPIOT_P_07_CLK4_P	GPIOT_P_11	GPIOT_N_14	GPIOT_N_17	GPIOR_15	VCCIO33_TR	GPIOR_18	REF_RES_3A
C	GPIOL_N_16	GPIOL_N_17	GPIOL_06	GPIOL_07	GPIOL_11_PLLIN2	GPIOT_N_01	VCCIO2A	GPIOT_P_10_CLK7_P	GPIOT_N_10_CLK7_N	GPIOT_P_13	VCCIO2B	GPIOR_16	GPIOR_P_17	GPIOR_P_19_PLLIN0	GPIOR_N_19
D	GPIOL_P_16	VCCIO1B	GND	VCCAUX	GPIOT_N_00	VCCIO2A	GPIOT_N_05	GPIOT_N_09_CLK6_N	VCCIO2B	GPIOT_N_13	REF_RES_2B	GPIOR_20	GPIOR_N_17	GPIOR_N_18	GPIOR_P_18
E	GPIOL_P_15_NSTATUS	GPIOL_N_15_TEST_N	GPIOL_N_13_CBSEL1	REF_RES_1B	VCCA_TL	GPIOT_P_00_PLLIN1	GPIOT_P_05	GPIOT_P_09_CLK6_P	GPIOT_N_12	GPIOT_P_16_EXTFB	VCCAUX	GPIOR_N_15	VCC	GPIOR_N_16	GPIOR_P_16
F	GPIOL_P_14	GPIOL_N_14	GPIOL_P_13_CBSEL0	VCCIO1B	GPIOL_N_11	REF_RES_2A	GPIOT_P_04	GPIOT_N_04	GPIOT_P_12	GPIOT_N_16	GPIOR_N_14	GPIOR_P_15	GPIOR_N_12	VCCIO3A	GPIOR_N_13
G	GPIOL_N_09_CLK2_N	GPIOL_N_10_CLK3_N	GPIOL_P_12	GPIOL_N_12	GPIOL_P_11	VQPS	VCC	GND	VCC	VCCA_TR	GPIOR_P_14	VCCIO3A	GPIOR_P_12	GPIOR_N_11_CLK8_N	GPIOR_P_13
H	GPIOL_P_09_CLK2_P	GPIOL_P_10_CLK3_P	GPIOL_N_08_CLK1_N	GPIOL_N_04_CDI3	GPIOL_P_04_CDI2	VCC	GND	VCC	GND	GPIOR_P_08_CLK11_P	GPIOR_N_08_CLK11_N	GPIOR_N_10_CLK9_N	GPIOR_P_10_CLK9_P	GPIOR_P_11_CLK8_P	GPIOR_N_09_CLK10_N
J	GPIOL_N_07_CLK0_N	GPIOL_P_08_CLK1_P	GPIOL_N_05	VCCIO1A	CRESET_N	GND	VCC	GND	VCC	GPIOR_N_03_CDI27	VCCIO3B	GPIOR_N_04_CDI29	GPIOR_N_06_CDI21	GPIOR_N_07	GPIOR_P_09_CLK10_P
K	GPIOL_P_07_CLK0_P	GPIOL_N_06	GPIOL_P_06	GPIOL_P_05	REF_RES_1A	GPIOB_N_04	GPIOB_P_09_CLK13_P	GPIOB_P_11_CDI10	GPIOB_N_11_CDI11	GPIOR_P_03_CDI26	GPIOR_N_00_CDI22	GPIOR_P_04_CDI28	GPIOR_P_06_CDI20	GPIOR_P_07	GPIOR_N_05_CDI31
L	GPIOL_N_03_CDI1	VCCIO1A	CDONE	VCCAUX	VCCA_BL	GPIOB_P_04_SSU_N	GPIOB_N_06_CDI9	GPIOB_N_09_CLK13_N	GPIOB_N_10_CLK12_N	VCCA_BR	GPIOR_P_00_PLLIN0	GPIOR_P_01_EXTFB	GPIOR_N_01_CDI23	VCCIO3B	GPIOR_P_05_CDI30
M	GPIOL_P_03_CDI0	GPIOL_N_02_CSO	VCC	TDO	REF_RES_4B	GPIOB_N_03_CDI7	GPIOB_P_06_CDI8	GPIOB_N_08_CLK14_N	GPIOB_P_10_CLK12_P	GPIOB_N_13_CDI15	VCCAUX	REF_RES_3B	GND	GPIOR_P_02_CDI24	GPIOR_N_02_CDI25
N	GPIOL_N_01_CCK	GPIOL_P_02_CSI	TMS	TCK	VCCIO4B	GPIOB_P_03_CDI6	VCCIO4B	GPIOB_P_08_CLK14_P	VCCIO4A	GPIOB_P_13_CDI14	VCCIO4A	REF_RES_4A	GPIOR_24	GPIOR_21	VCCIO33_BR
P	GPIOL_P_01_SSL_N	GPIOL_P_00_PLLIN0	TDI	VCCIO33_BL	GPIOB_N_00	GPIOB_N_01	GPIOB_N_02_CDI5	GPIOB_N_07_CLK15_N	GPIOB_N_12_CDI13	GPIOB_N_14_CDI17	GPIOB_P_17_PLLIN1	GPIOB_N_17	GPIOR_27	GPIOR_22	GPIOR_25
R	GND	GPIOL_N_00	GPIOL_01	GPIOL_02	GPIOB_P_00_PLLIN1	GPIOB_P_01_EXTFB	GPIOB_P_02_CDI4	GPIOB_P_07_CLK15_P	GPIOB_P_12_CDI12	GPIOB_P_14_CDI16	GPIOB_N_15_CDI19	GPIOB_P_15_CDI18	GPIOR_29_PLLIN2	GPIOR_28	GND

- MIPI RX group I0
- MIPI RX group I1
- MIPI RX group I2
- MIPI RX group I3
- MIPI RX group I4
- MIPI RX group I5
- MIPI RX group I6
- MIPI RX group I7
- MIPI RX group I8
- MIPI RX group I9
- MIPI RX group I10
- MIPI RX group I11
- C Clock lane
- Not in MIPI RX group

Figure 14: 225-Ball FPGA Package Marking

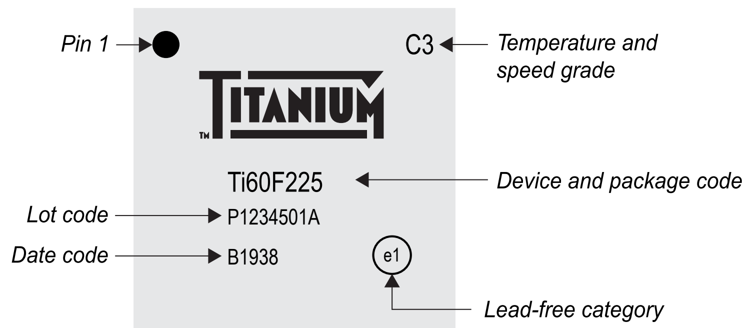
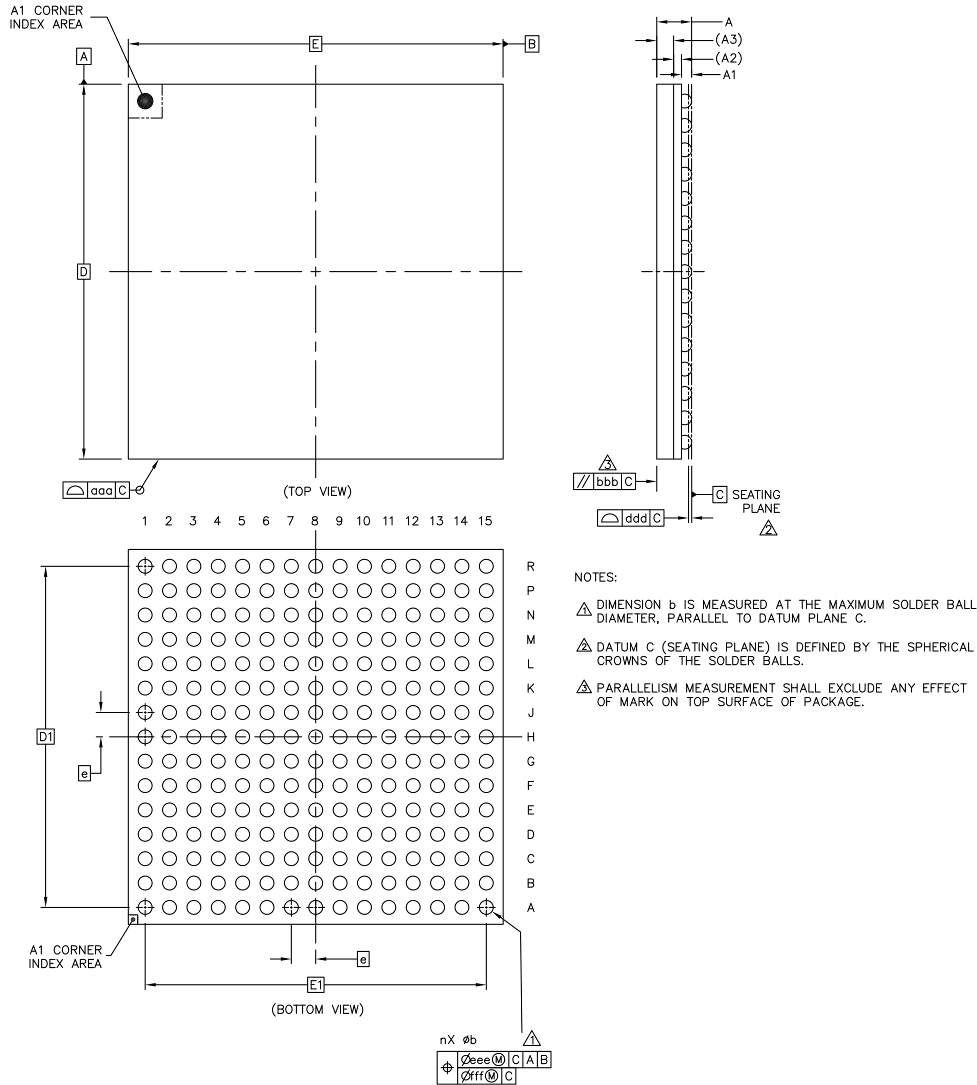


Figure 15: 225-Ball FBGA Package Outline



For Lot Number: 'CXXXXXX' and 'SXXXXXX'

	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1.1
STAND OFF	A1	0.22	---	0.32
SUBSTRATE THICKNESS	A2		0.21	REF
MOLD THICKNESS	A3		0.54	REF
BODY SIZE	D		10	BSC
	E		10	BSC
BALL DIAMETER			0.35	
BALL OPENING			0.3	
BALL WIDTH	b	0.32	---	0.42
BALL PITCH	e		0.65	BSC
BALL COUNT	n		225	
EDGE BALL CENTER TO CENTER	D1		9.1	BSC
	E1		9.1	BSC
BODY CENTER TO CONTACT BALL	SD		---	BSC
	SE		---	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

For Other Lot Numbers

	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1
STAND OFF	A1	0.22	---	0.32
SUBSTRATE THICKNESS	A2		0.21	REF
MOLD THICKNESS	A3		0.45	REF
BODY SIZE	D		10	BSC
	E		10	BSC
BALL DIAMETER			0.35	
BALL OPENING			0.3	
BALL WIDTH	b	0.32	---	0.42
BALL PITCH	e		0.65	BSC
BALL COUNT	n		225	
EDGE BALL CENTER TO CENTER	D1		9.1	BSC
	E1		9.1	BSC
BODY CENTER TO CONTACT BALL	SD		---	BSC
	SE		---	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

256-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

Figure 16: 256-Ball FBGA Pinout Diagram

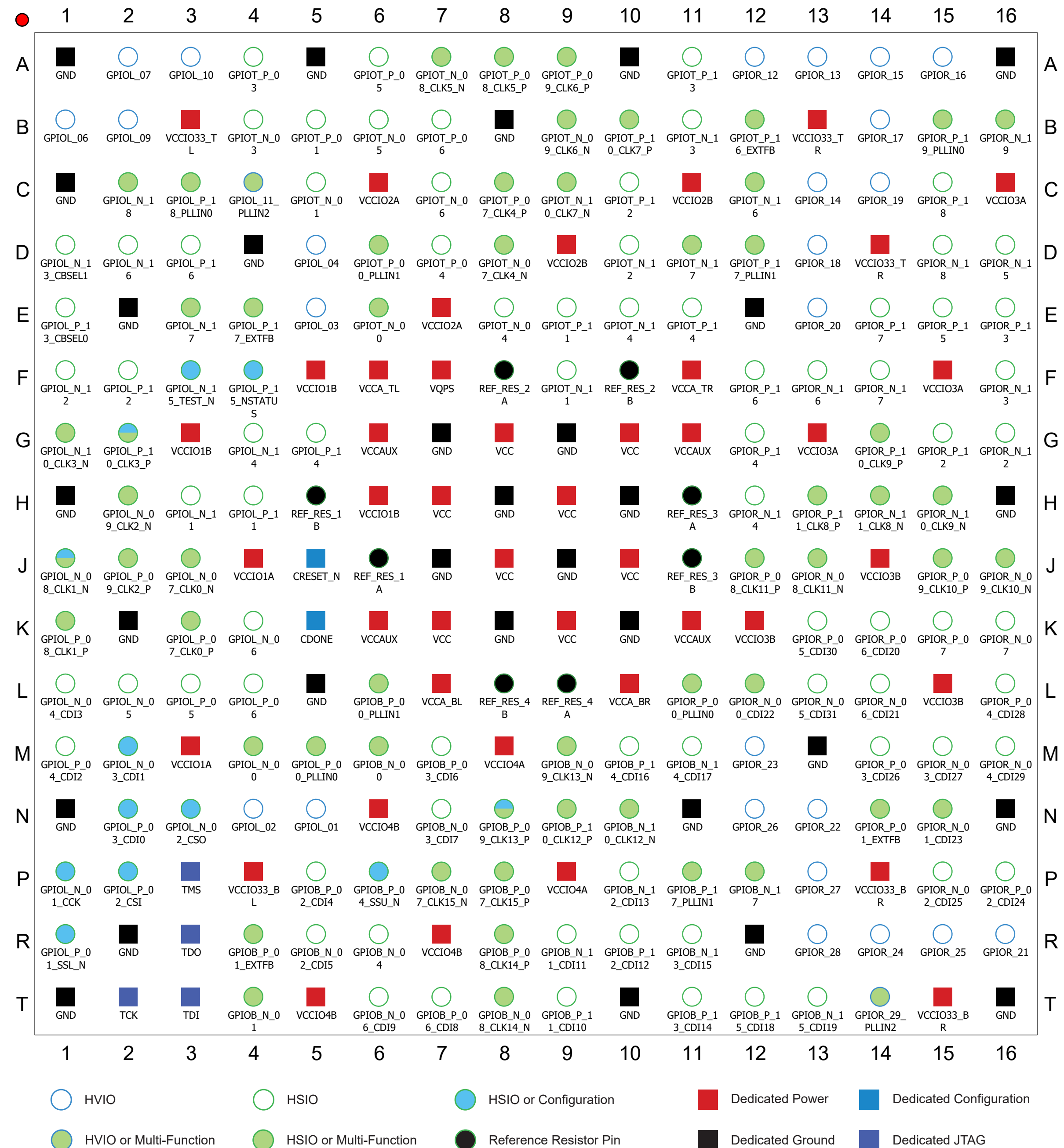


Figure 17: 256-Ball FBGA I/O Bank Diagram

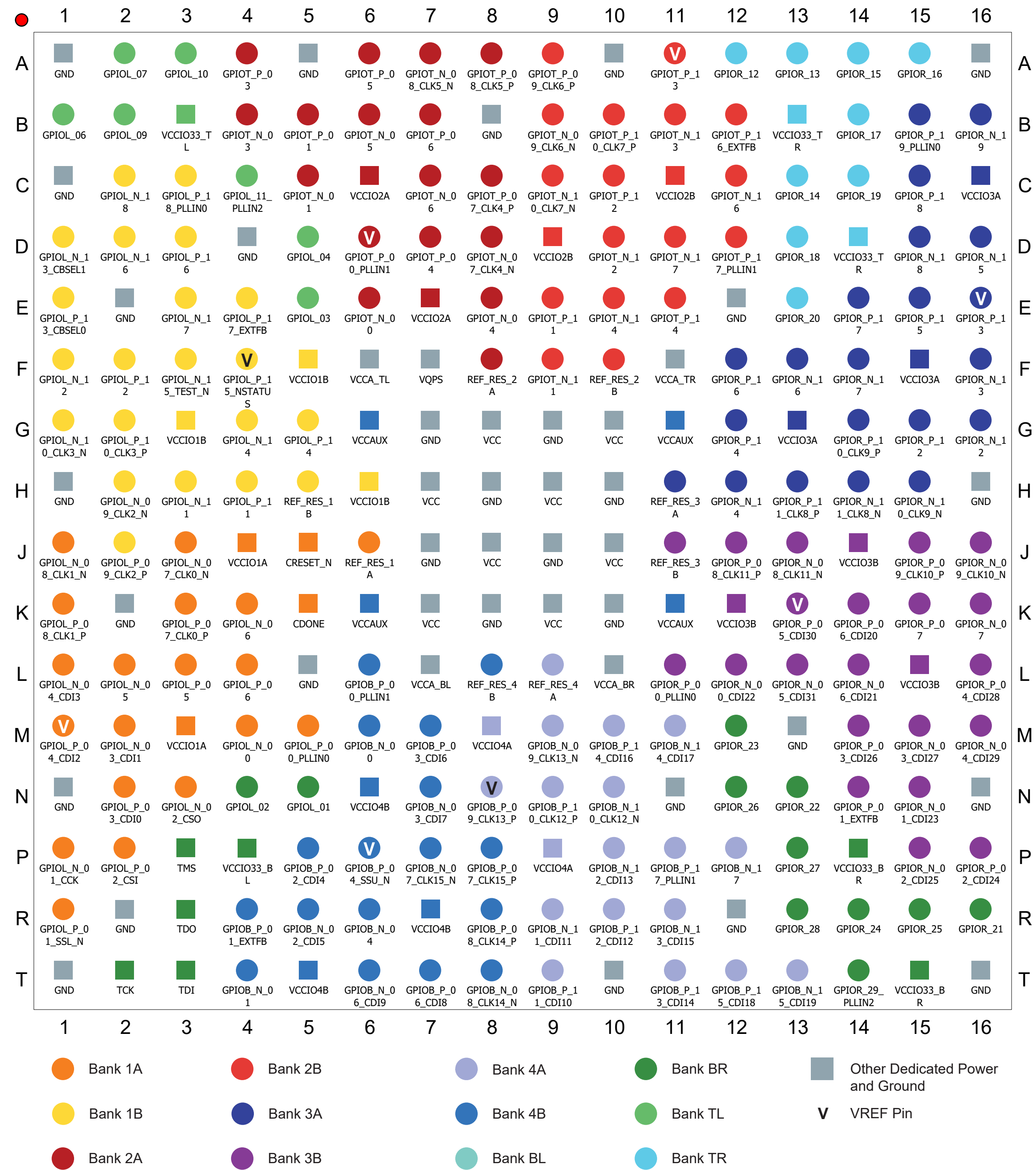


Figure 18: 256-Ball FBGA Emulated MIPI RX Groups

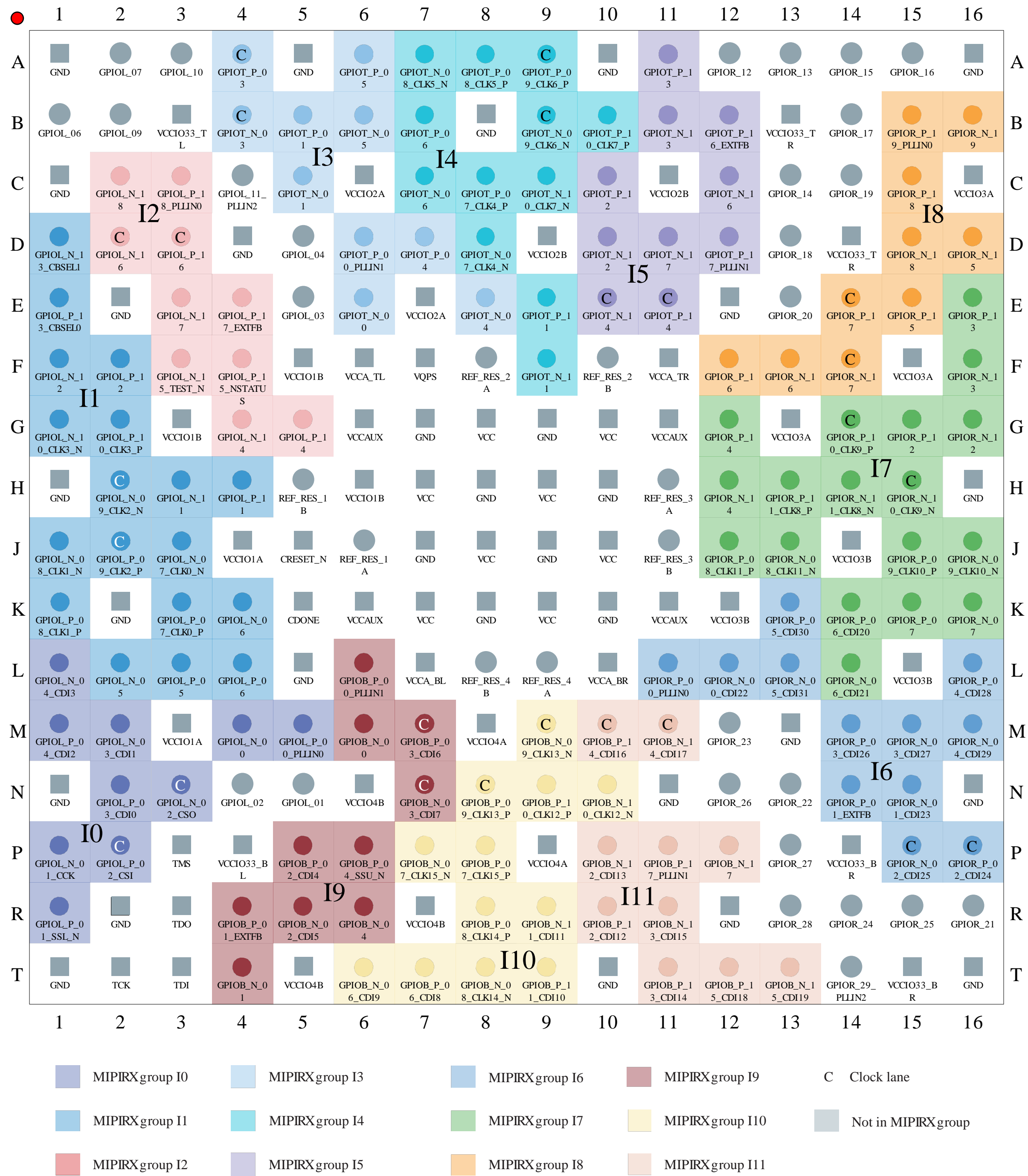


Figure 19: 256-Ball FPGA Package Marking

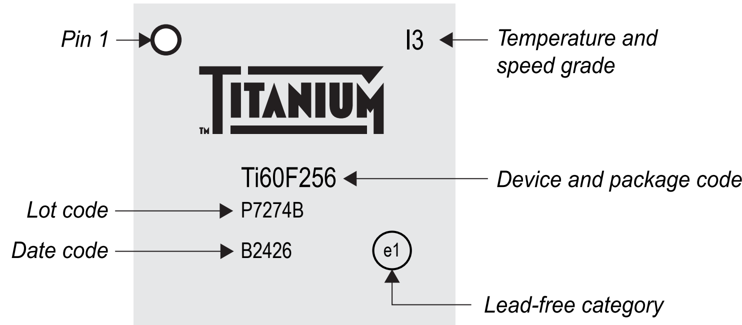
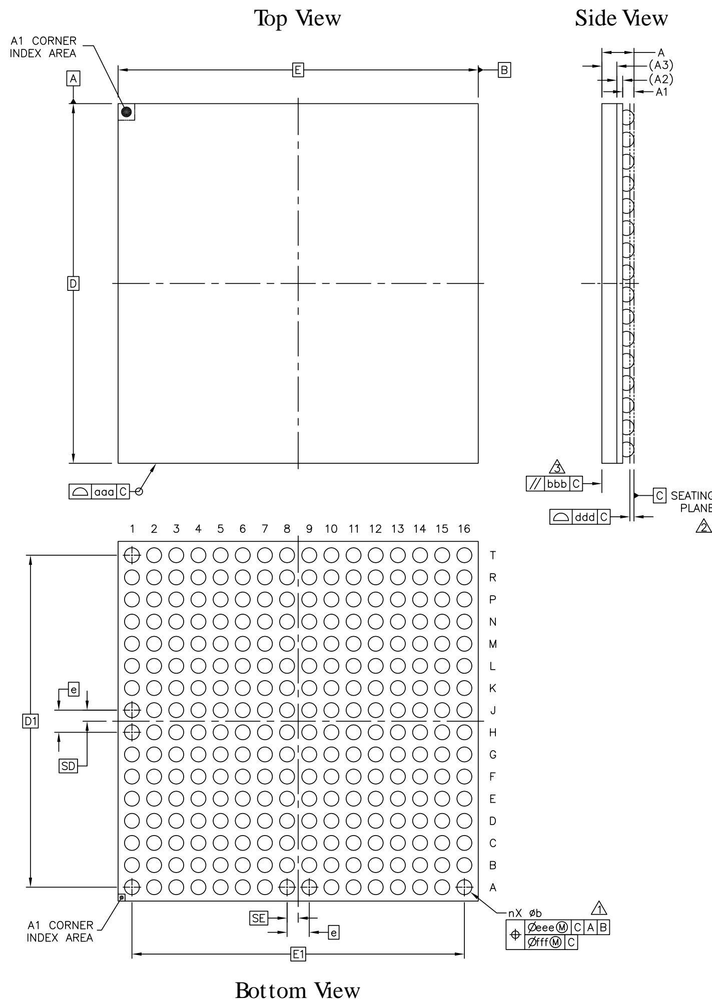


Figure 20: 256-Ball FBGA Package Outline



NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1.235
STAND OFF	A1	0.36	---	0.46
SUBSTRATE THICKNESS	A2		0.21	REF
MOLD THICKNESS	A3		0.54	REF
BODY SIZE	D		13	BSC
	E		13	BSC
BALL DIAMETER			0.5	
BALL OPENING			0.4	
BALL WIDTH	b	0.44	---	0.64
BALL PITCH	e		0.8	BSC
BALL COUNT	n		256	
EDGE BALL CENTER TO CENTER	D1		12	BSC
	E1		12	BSC
BODY CENTER TO CONTACT BALL	SD		0.4	BSC
	SE		0.4	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.15	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

361-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

Figure 21: 361-Ball FBGA Pinout Diagram

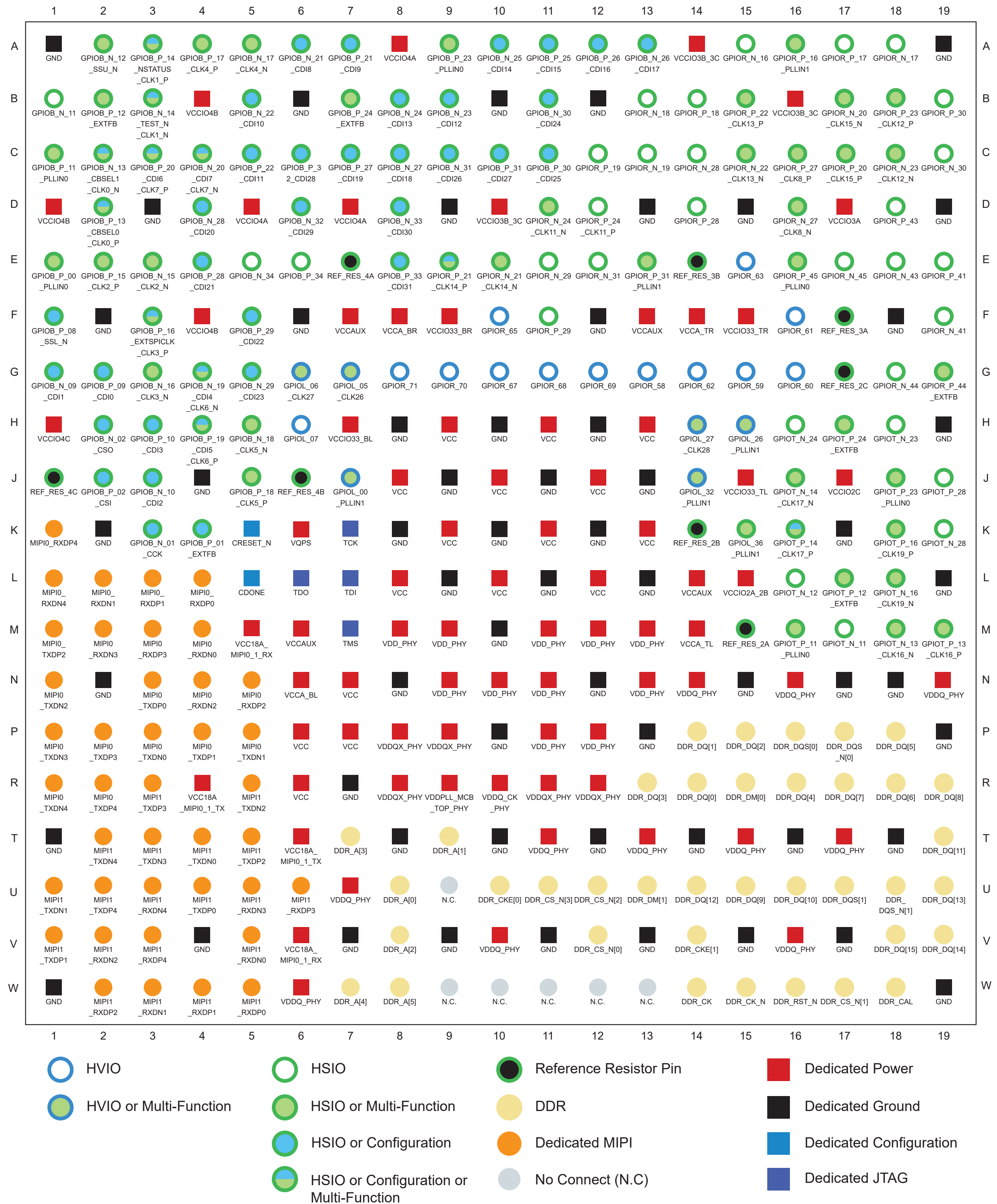


Figure 22: 361-Ball FBGA I/O Bank Diagram

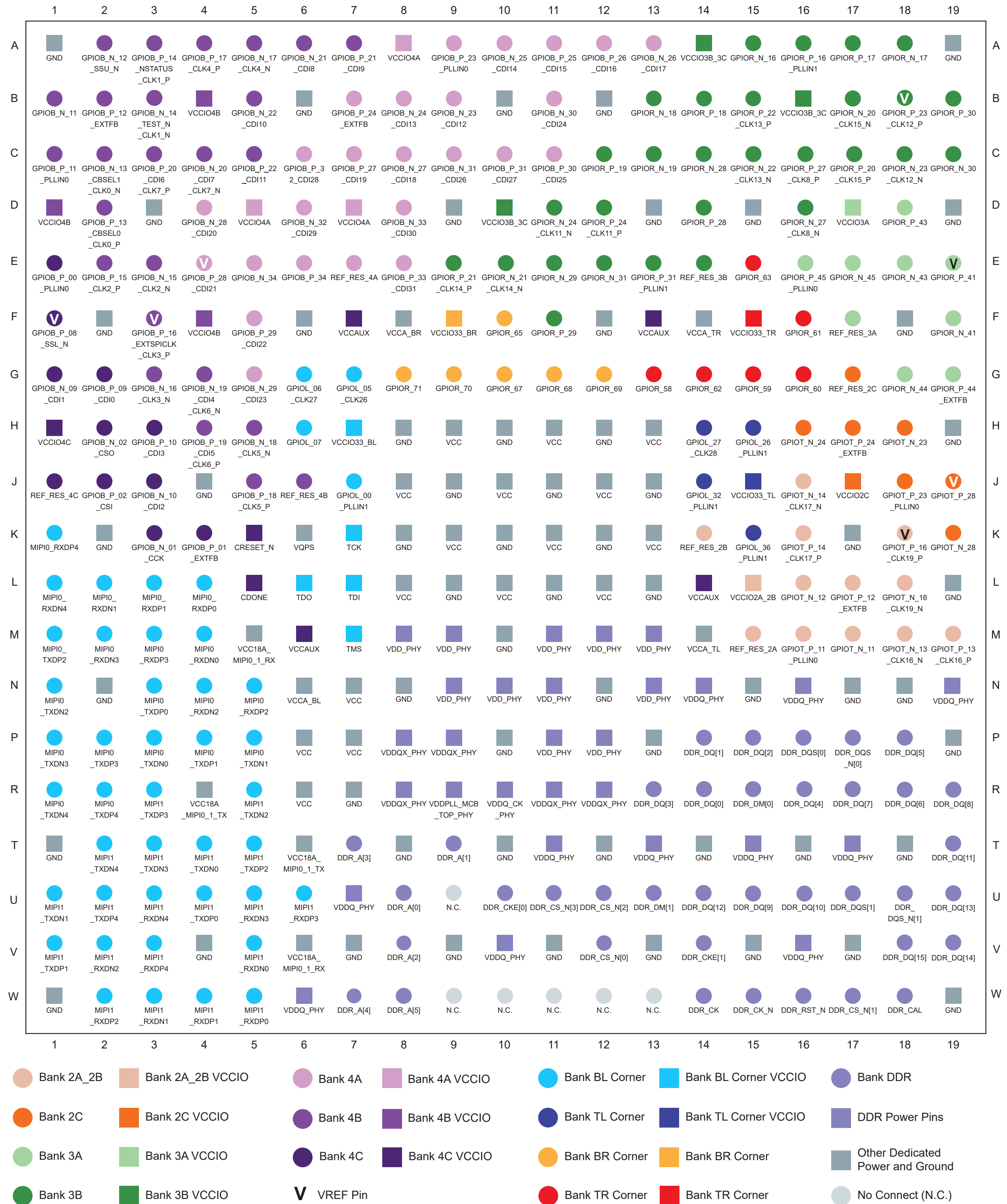


Figure 23: 361-Ball FBGA Emulated MIPI RX Groups

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A	GND	GPIOB_N_12_SSU_N	GPIOB_P_14_NSTATUS_CLK1_P	GPIOB_P_17_CLK4_P	GPIOB_N_17_CLK4_N	GPIOB_N_21_CDI8	GPIOB_P_21_CDI9	VCCIO4A	GPIOB_P_23_PLLIN0	GPIOB_N_25_CDI14	GPIOB_P_25_CDI15	GPIOB_P_26_CDI16	GPIOB_N_26_CDI17	VCCIO3B_3C	GPIOR_N_16	GPIOR_P_16_PLLIN1	GPIOR_P_17	GPIOR_N_17	GND
B	GPIOB_N_11	GPIOB_P_12_EXTFB	GPIOB_N_14_TEST_N_CLK1_N	VCCIO4B	GPIOB_N_22_CDI10	GND	GPIOB_P_24_EXTFB	GPIOB_N_24_CDI13	GPIOB_N_23_CDI12	GND	GPIOB_N_30_CDI24	GND	GPIOR_N_18	GPIOR_P_18	GPIOR_P_22_CLK13_P	VCCIO3B_3C	GPIOR_N_20_CLK15_N	GPIOR_P_23_CLK12_P	GPIOR_P_30
C	GPIOB_P_11_PLLIN0	GPIOB_N_13_CBSEL1_CLK0_N	GPIOB_P_20_CDI6_CLK7_P	GPIOB_N_20_CDI7_CLK7_N	GPIOB_P_22_CDI11	GPIOB_P_32_CDI28	GPIOB_P_27_CDI19	GPIOB_N_27_CDI18	GPIOB_N_31_CDI26	GPIOB_P_31_CDI27	GPIOB_P_30_CDI25	GPIOR_P_19	GPIOR_N_19	GPIOR_N_28	GPIOR_N_22_CLK13_N	GPIOR_P_27_CLK8_P	GPIOR_P_20_CLK15_P	GPIOR_N_23_CLK12_N	GPIOR_N_30
D	VCCIO4B	GPIOB_P_13_CBSEL0_CLK0_P	GND	GPIOB_N_28_CDI20	VCCIO4A	GPIOB_N_32_CDI29	VCCIO4A	GPIOB_N_33_CDI30	GND	VCCIO3B_3C	GPIOR_N_24_CLK11_N	GPIOR_P_24_CLK11_P	GND	GPIOR_P_28	GND	GPIOR_N_27_CLK8_N	VCCIO3A	GPIOR_P_43	GND
E	GPIOB_P_00_PLLIN0	GPIOB_P_15_CLK2_P	GPIOB_N_15_CLK2_N	GPIOB_P_28_CDI21	GPIOB_N_34	GPIOB_P_34	REF_RES_4A	GPIOB_P_33_CDI31	GPIOR_P_21_CLK14_P	GPIOR_N_21_CLK14_N	GPIOR_N_29	GPIOR_N_31	GPIOR_P_31_PLLIN1	REF_RES_3B	GPIOR_63	GPIOR_P_45_PLLIN0	GPIOR_N_45	GPIOR_N_43	GPIOR_P_41
F	GPIOB_P_08_SSL_N	GND	GPIOB_P_16_EXTSPICLK_CLK3_P	VCCIO4B	GPIOB_P_29_CDI22	GND	VCCAUX	VCCA_BR	VCCIO33_BR	GPIOR_65	GPIOR_P_29	GND	VCCAUX	VCCA_TR	VCCIO33_TR	GPIOR_61	REF_RES_3A	GND	GPIOR_N_41
G	GPIOB_N_09_CDI1	GPIOB_P_09_CDI0	GPIOB_N_16_CLK3_N	GPIOB_N_19_CDI4_CLK6_N	GPIOB_N_29_CDI23	GPIOL_06_CLK27	GPIOL_05_CLK26	GPIOR_71	GPIOR_70	GPIOR_67	GPIOR_68	GPIOR_69	GPIOR_58	GPIOR_62	GPIOR_59	GPIOR_60	REF_RES_2C	GPIOR_N_44	GPIOR_P_44_EXTFB
H	VCCIO4C	GPIOB_N_02_CSO	GPIOB_P_10_CDI3	GPIOB_P_19_CDI5_CLK6_P	GPIOB_N_18_CLK5_N	GPIOL_07	VCCIO33_BL	GND	VCC	GND	VCC	GND	VCC	GPIOL_27_CLK28	GPIOL_26_PLLIN1	GPIOT_N_24	GPIOT_P_24_EXTFB	GPIOT_N_23	GND
J	REF_RES_4C	GPIOB_P_02_CSI	GPIOB_N_10_CDI2	GND	GPIOB_P_18_CLK5_P	REF_RES_4B	GPIOL_00_PLLIN1	VCC	GND	VCC	GND	VCC	GND	GPIOL_32_PLLIN1	VCCIO33_TL	GPIOT_N_14_CLK17_N	VCCIO2C	GPIOT_P_23_PLLIN0	GPIOT_P_28
K	MIPI0_RXDP4	GND	GPIOB_N_01_CCK	GPIOB_P_01_EXTFB	CRESET_N	VQPS	TCK	GND	VCC	GND	VCC	GND	VCC	REF_RES_2B	GPIOL_36_PLLIN1	GPIOT_P_14_CLK17_P	GND	GPIOT_P_16_CLK19_P	GPIOT_N_28
L	MIPI0_RXDN4	MIPI0_RXDN1	MIPI0_RXDP1	MIPI0_RXDP0	CDONE	TDO	TDI	VCC	GND	VCC	GND	VCC	GND	VCCAUX	VCCIO2A_2B	GPIOT_N_12	GPIOT_P_12_EXTFB	GPIOT_N_16_CLK19_N	GND
M	MIPI0_TXDP2	MIPI0_RXDN3	MIPI0_RXDP3	MIPI0_RXDN0	VCC18A_MIPI0_1_RX	VCCAUX	TMS	VDD_PHY	VDD_PHY	GND	VDD_PHY	VDD_PHY	VDD_PHY	VCCA_TL	REF_RES_2A	GPIOT_P_11_PLLIN0	GPIOT_N_11	GPIOT_N_13_CLK16_N	GPIOT_P_13_CLK16_P

Group labels: I15, I14, I13, I12, I9, I8, I6, I17, I2

- MIPI RX group I2
- MIPI RX group I9
- MIPI RX group I14
- Not part of MIPI RX Group
- MIPI RX group I6
- MIPI RX group I12
- MIPI RX group I15
- C Clock lane
- MIPI RX group I8
- MIPI RX group I13
- MIPI RX group I17

Figure 24: 361-Ball FPGA Package Marking

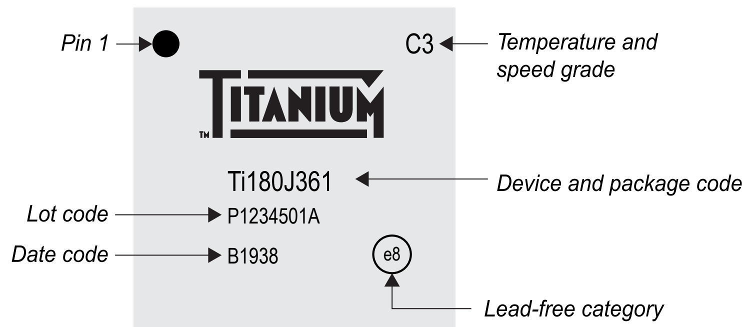
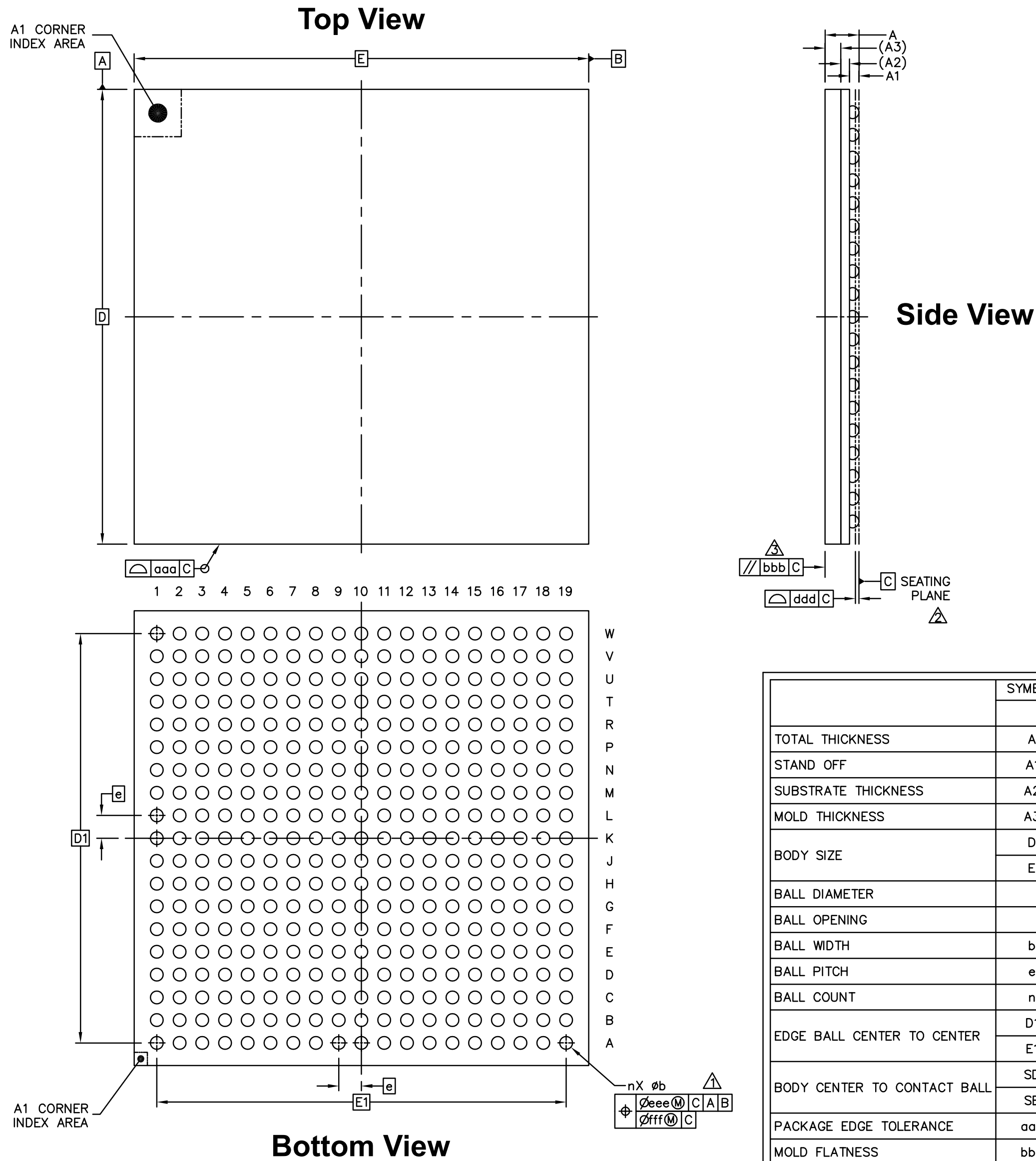


Figure 25: 361-Ball FBGA Package Outline



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	0.893	0.968	1.1
STAND OFF	A1	0.22	0.27	0.32
SUBSTRATE THICKNESS	A2		0.248	REF
MOLD THICKNESS	A3		0.45	REF
BODY SIZE	D		13	BSC
	E		13	BSC
BALL DIAMETER			0.35	
BALL OPENING			0.3	
BALL WIDTH	b	0.32	0.37	0.42
BALL PITCH	e		0.65	BSC
BALL COUNT	n		361	
EDGE BALL CENTER TO CENTER	D1		11.7	BSC
	E1		11.7	BSC
BODY CENTER TO CONTACT BALL	SD		---	BSC
	SE		---	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.1	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

400-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

Figure 26: 400-Ball FBGA Pinout Diagram

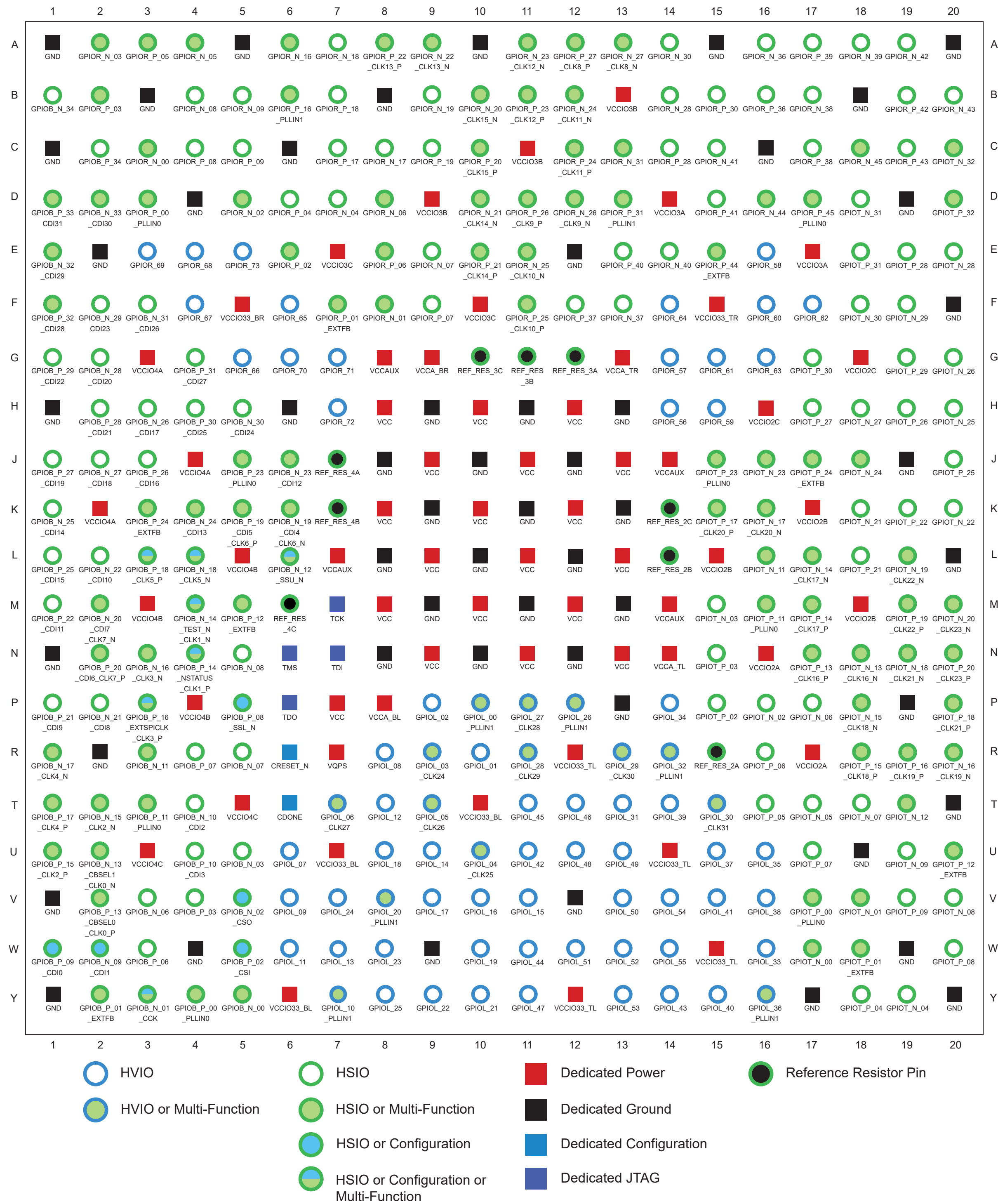


Figure 27: 400-Ball FBGA I/O Bank Diagram

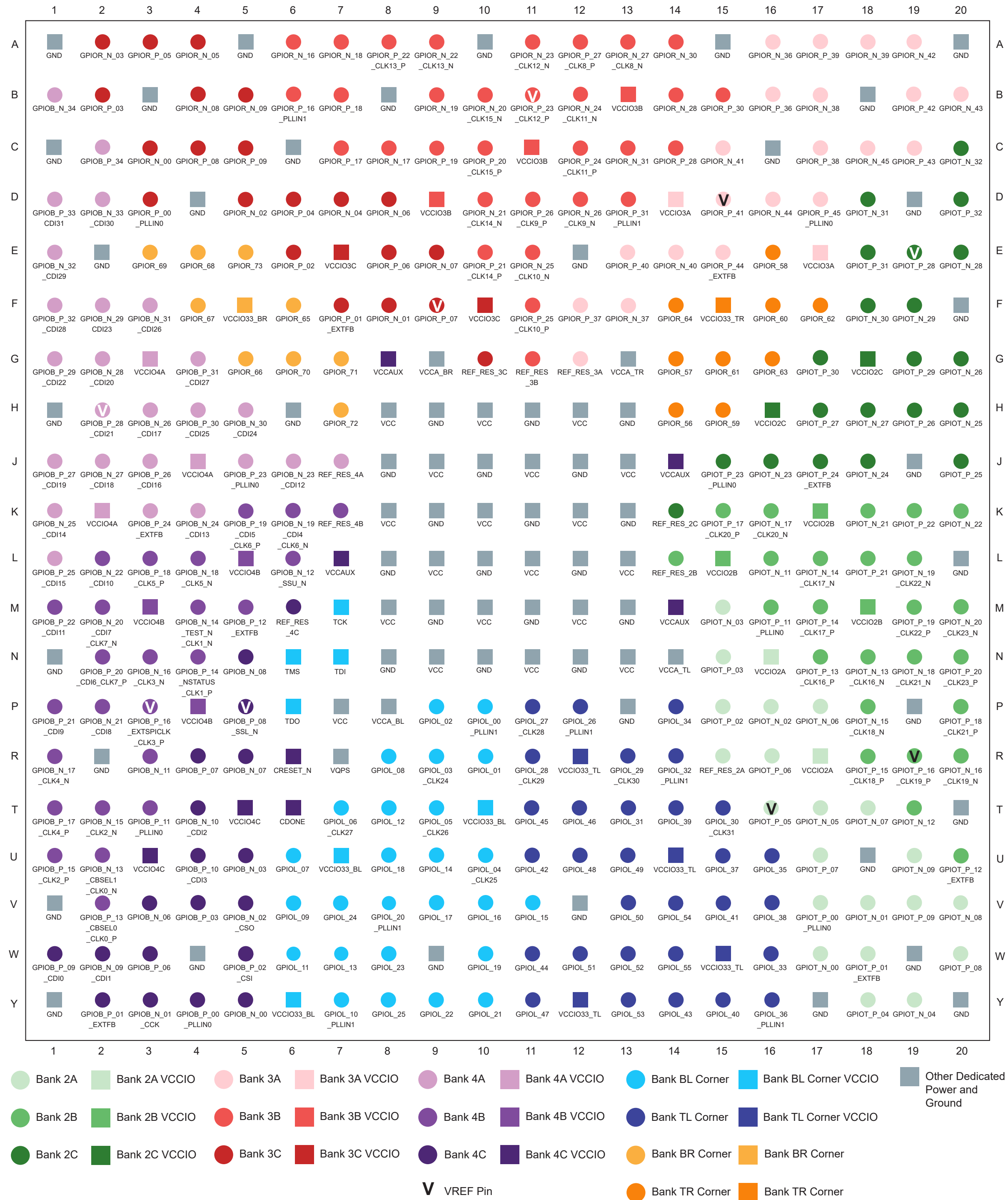


Figure 28: 400-Ball FBGA Emulated MIPI RX Groups

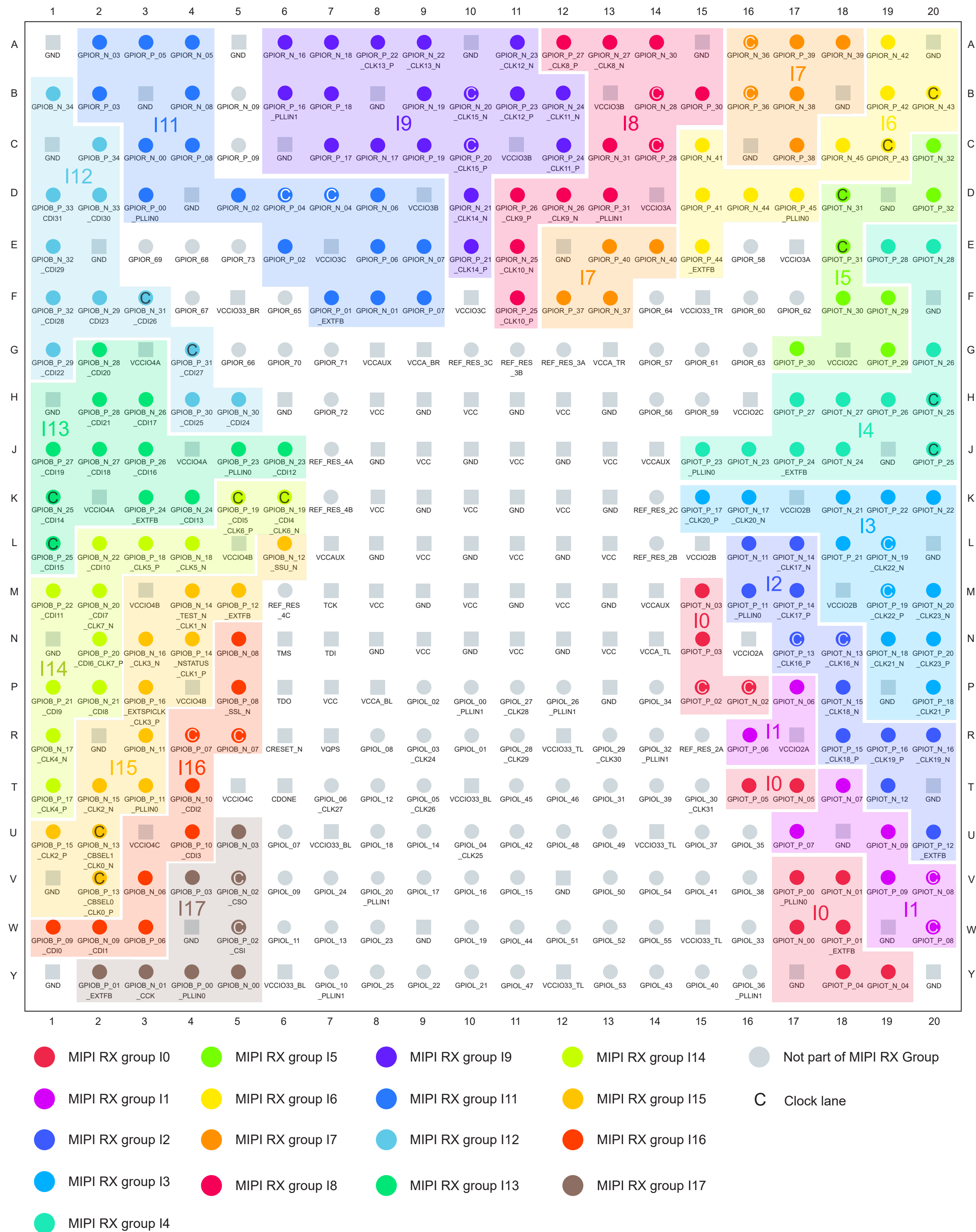


Figure 29: 400-Ball FPGA Package Marking

Preliminary.

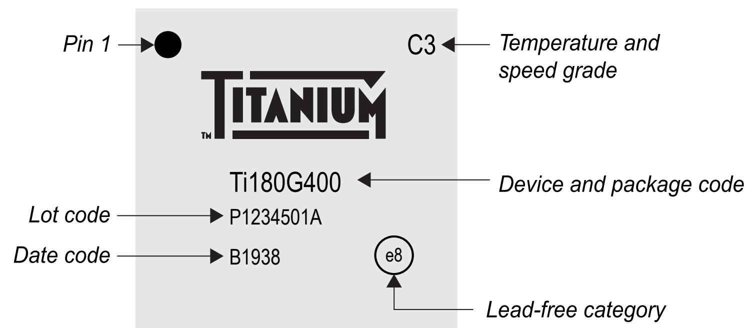
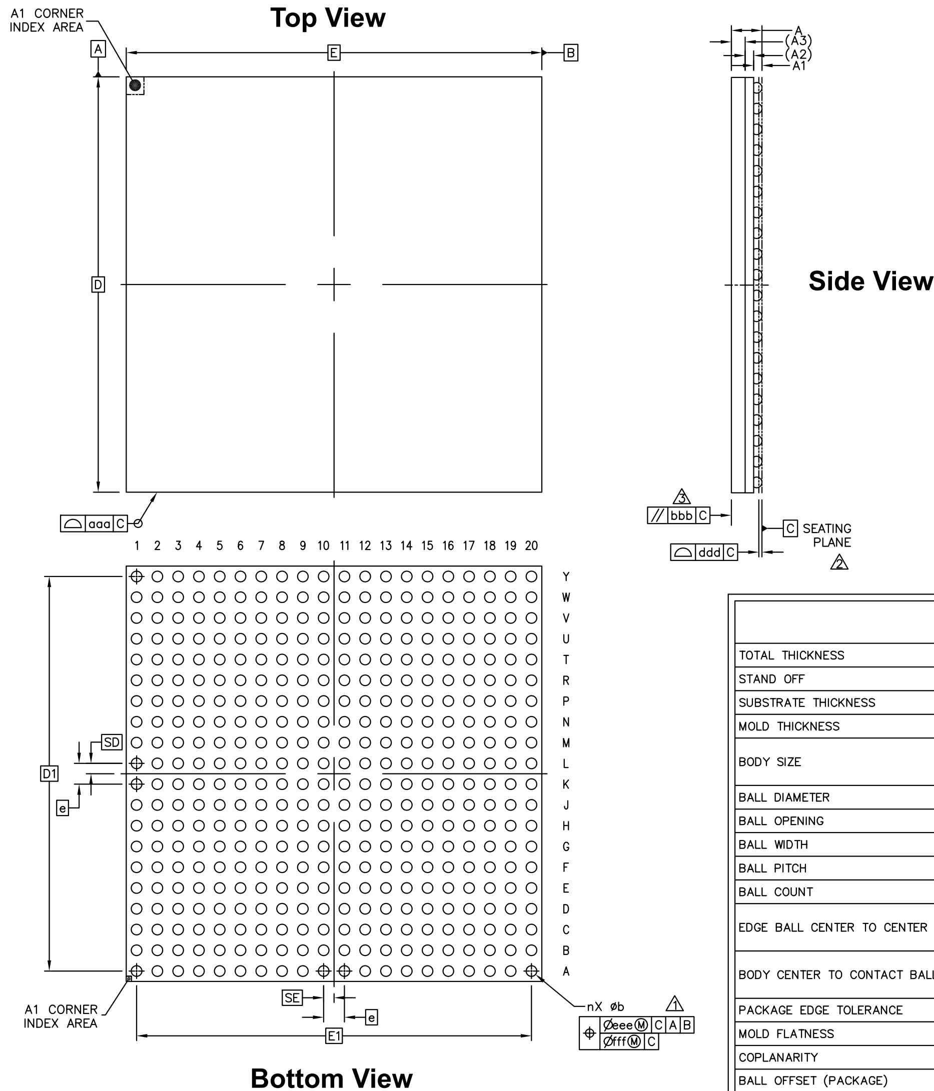


Figure 30: 400-Ball FBGA Package Outline



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	1.103	1.178	1.3
STAND OFF	A1	0.27	---	0.37
SUBSTRATE THICKNESS	A2		0.328	REF
MOLD THICKNESS	A3		0.53	REF
BODY SIZE	D		16	BSC
	E		16	BSC
BALL DIAMETER			0.4	
BALL OPENING			0.35	
BALL WIDTH	b	0.36	---	0.46
BALL PITCH	e		0.8	BSC
BALL COUNT	n		400	
EDGE BALL CENTER TO CENTER	D1		15.2	BSC
	E1		15.2	BSC
BODY CENTER TO CONTACT BALL	SD		0.4	BSC
	SE		0.4	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.15	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

484-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

484-Ball (J) FBGA Package Specifications

Figure 31: 484-Ball (J) FBGA Pinout Diagram

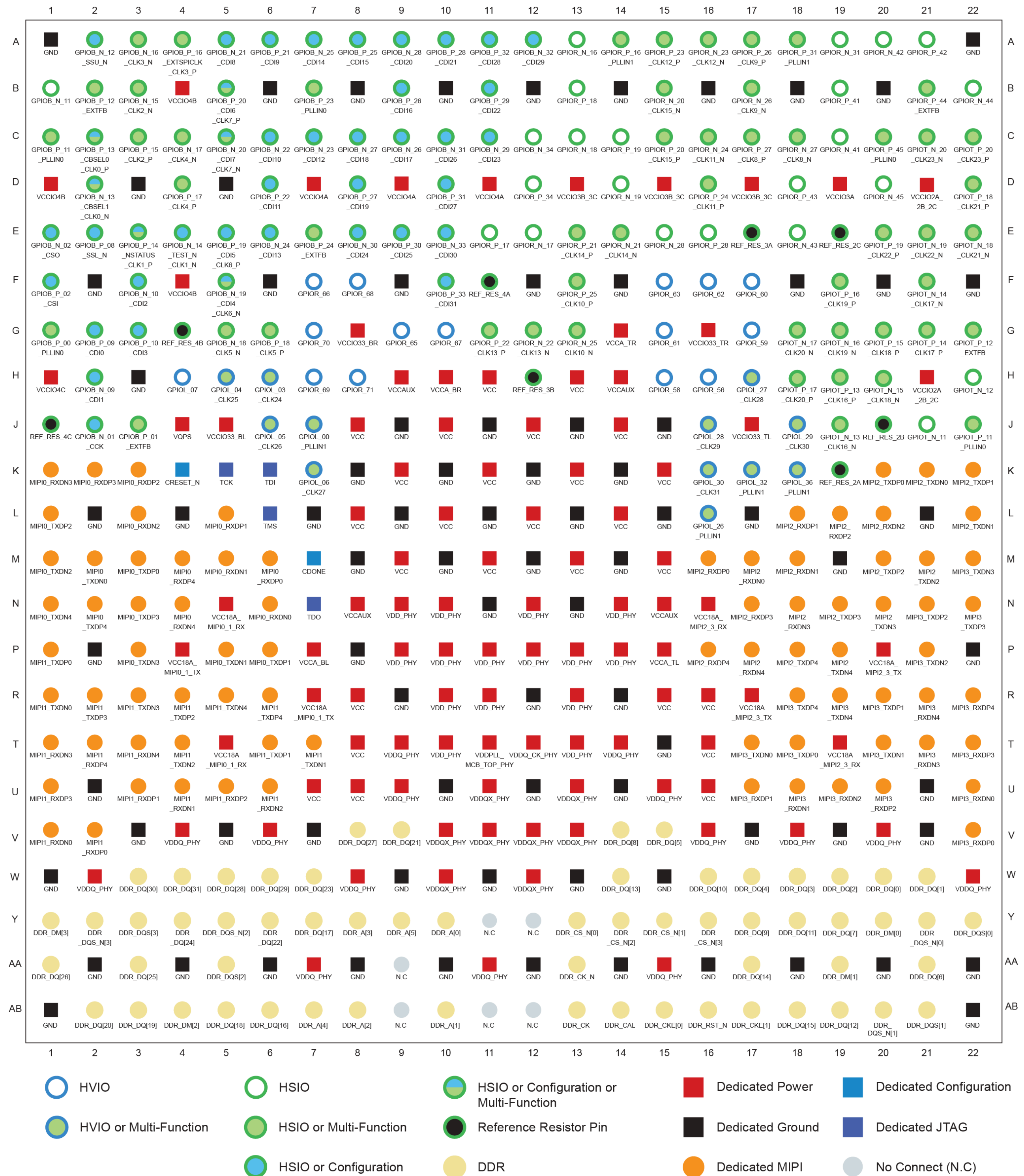


Figure 32: 484-Ball (J) FBGA I/O Bank Diagram

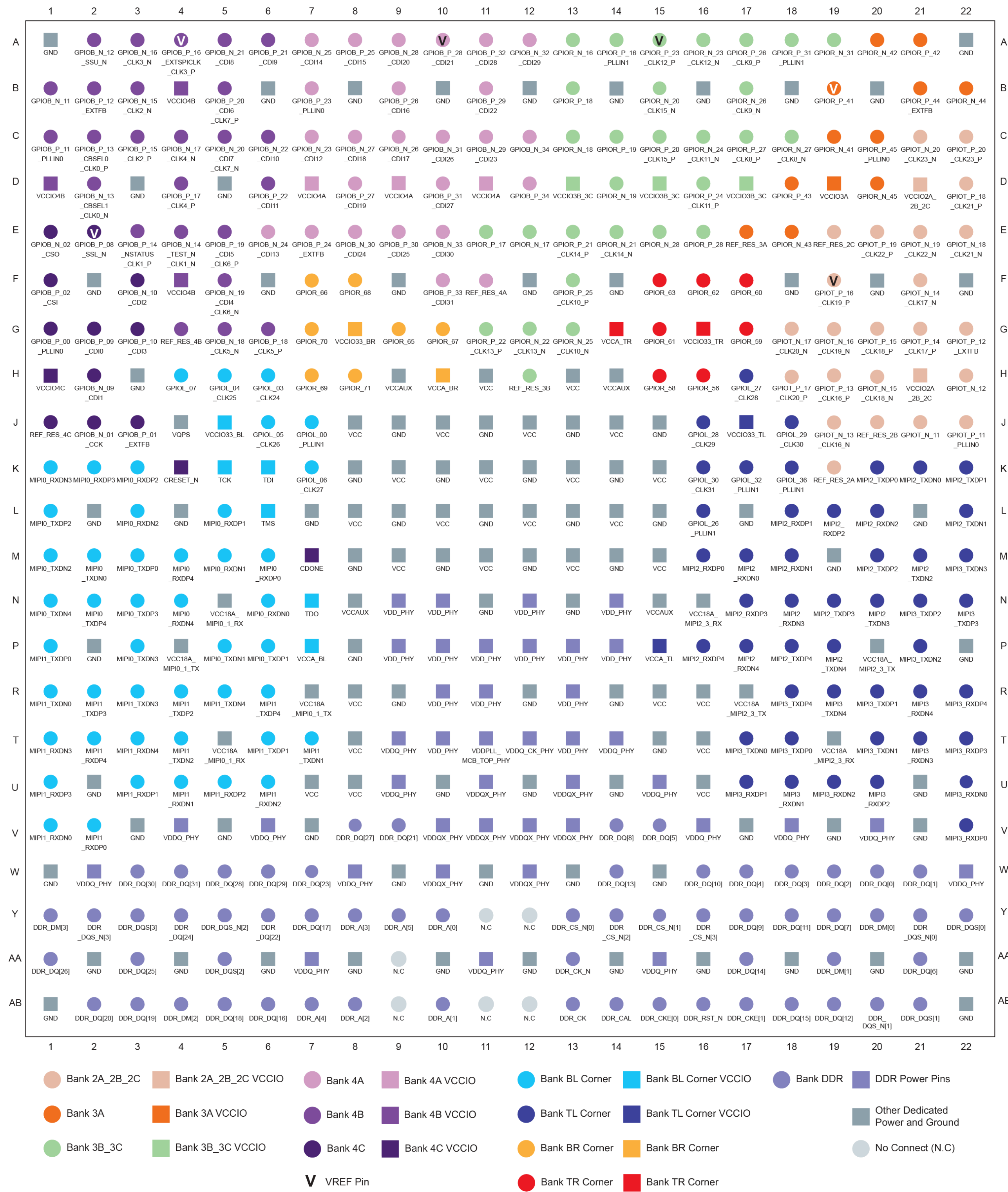


Figure 33: 484-Ball (J) FBGA Emulated MIPI RX Groups

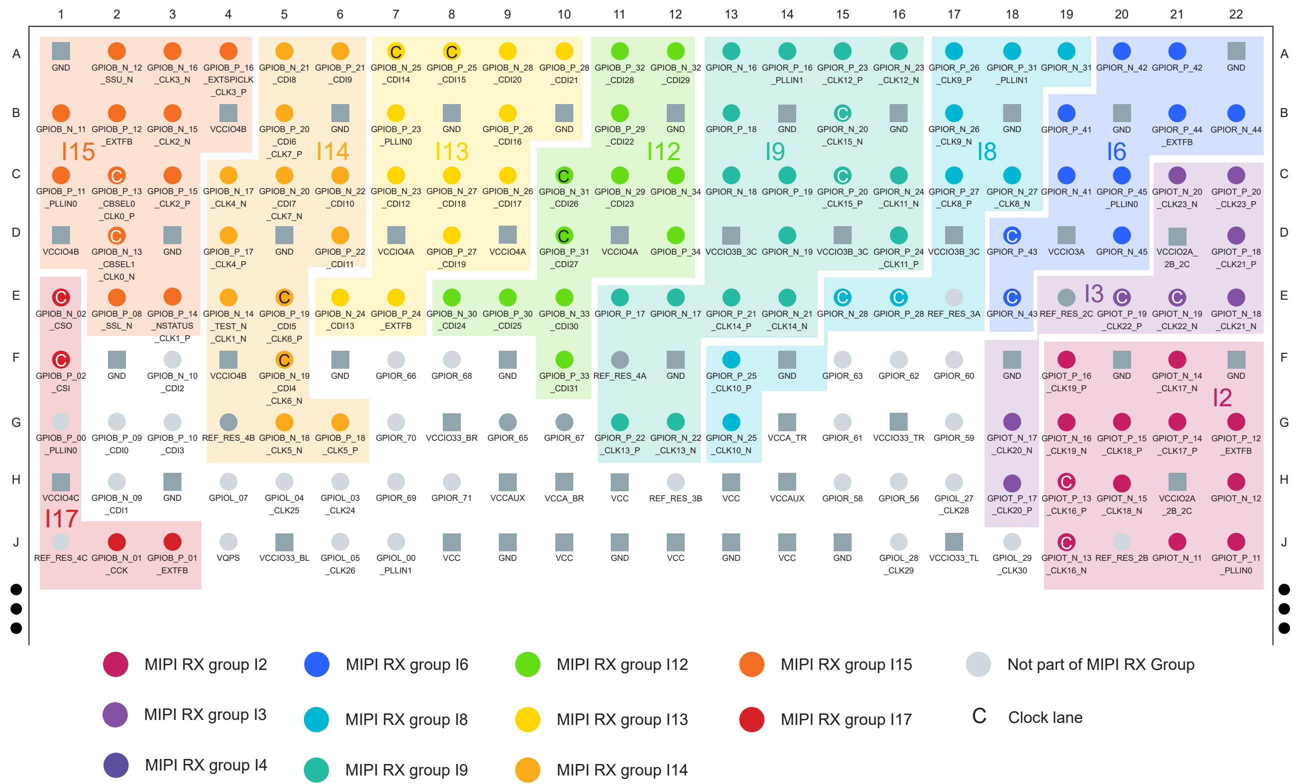


Figure 34: 484-Ball (J) FBGA Package Marking

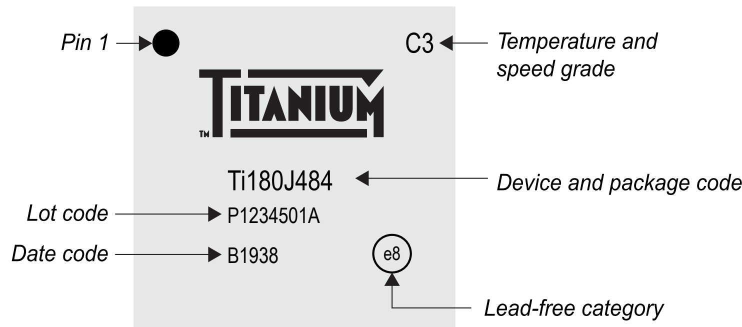
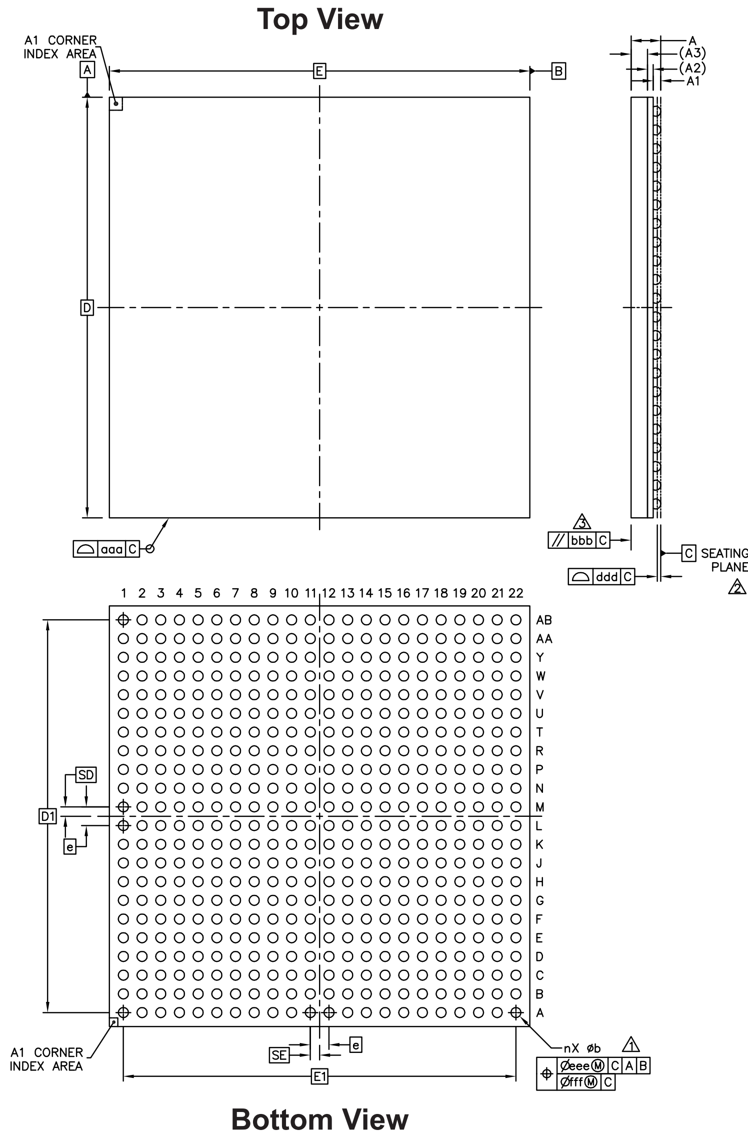


Figure 35: 484-Ball (J) FBGA Package Outline



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	1.193	1.268	1.4
STAND OFF	A1	0.27	0.32	0.37
SUBSTRATE THICKNESS	A2		0.248	REF
MOLD THICKNESS	A3		0.7	REF
BODY SIZE	D		18	BSC
	E		18	BSC
BALL DIAMETER			0.4	
BALL OPENING			0.35	
BALL WIDTH	b	0.38	0.43	0.48
BALL PITCH	e		0.8	BSC
BALL COUNT	n		484	
EDGE BALL CENTER TO CENTER	D1		16.8	BSC
	E1		16.8	BSC
BODY CENTER TO CONTACT BALL	SD		0.4	BSC
	SE		0.4	BSC
PACKAGE EDGE TOLERANCE	aaa		0.15	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.15	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

484-Ball (L) FBGA Package Specifications

Figure 36: 484-Ball (L) FBGA Pinout Diagram

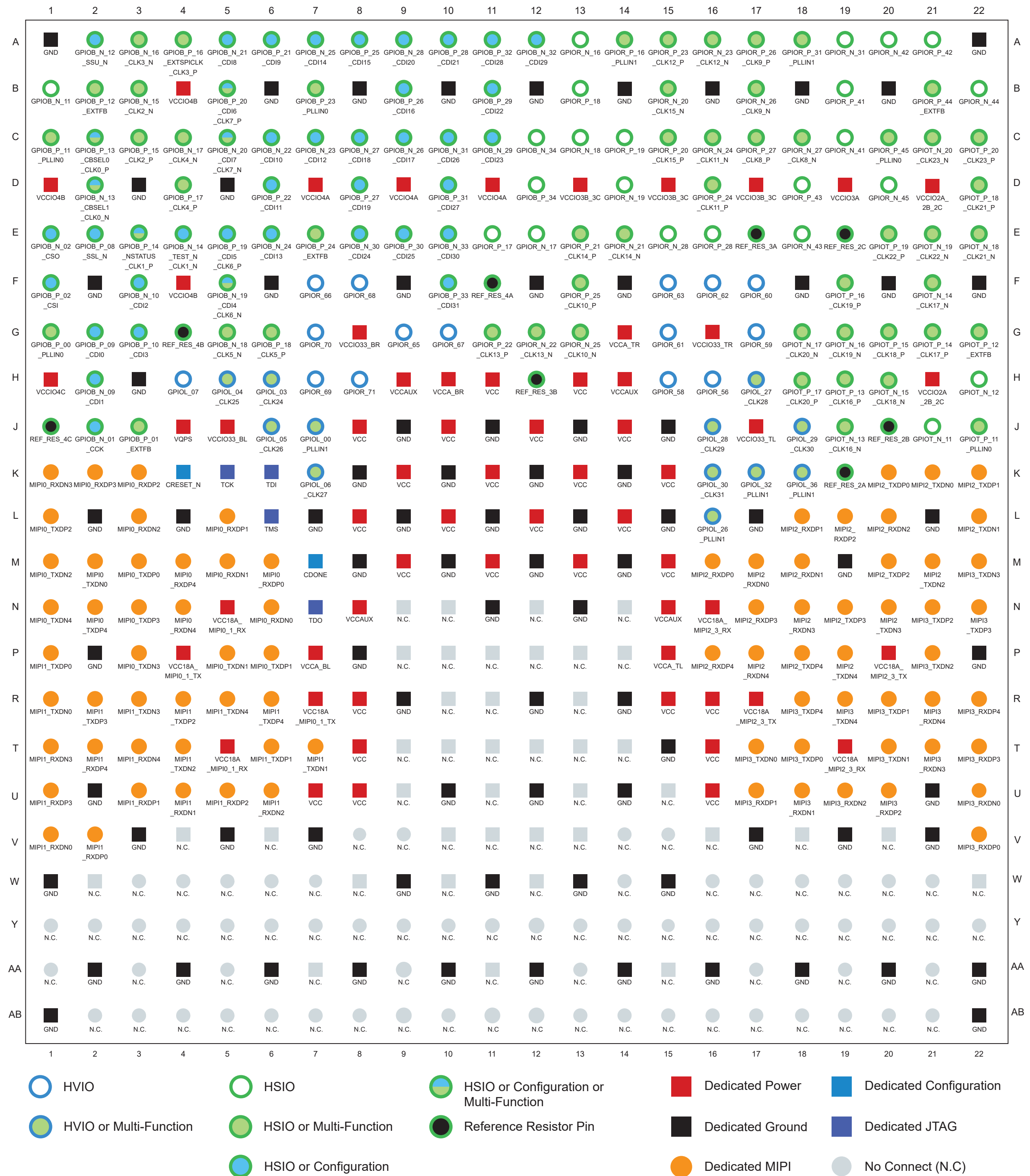


Figure 37: 484-Ball (L) FBGA I/O Bank Diagram

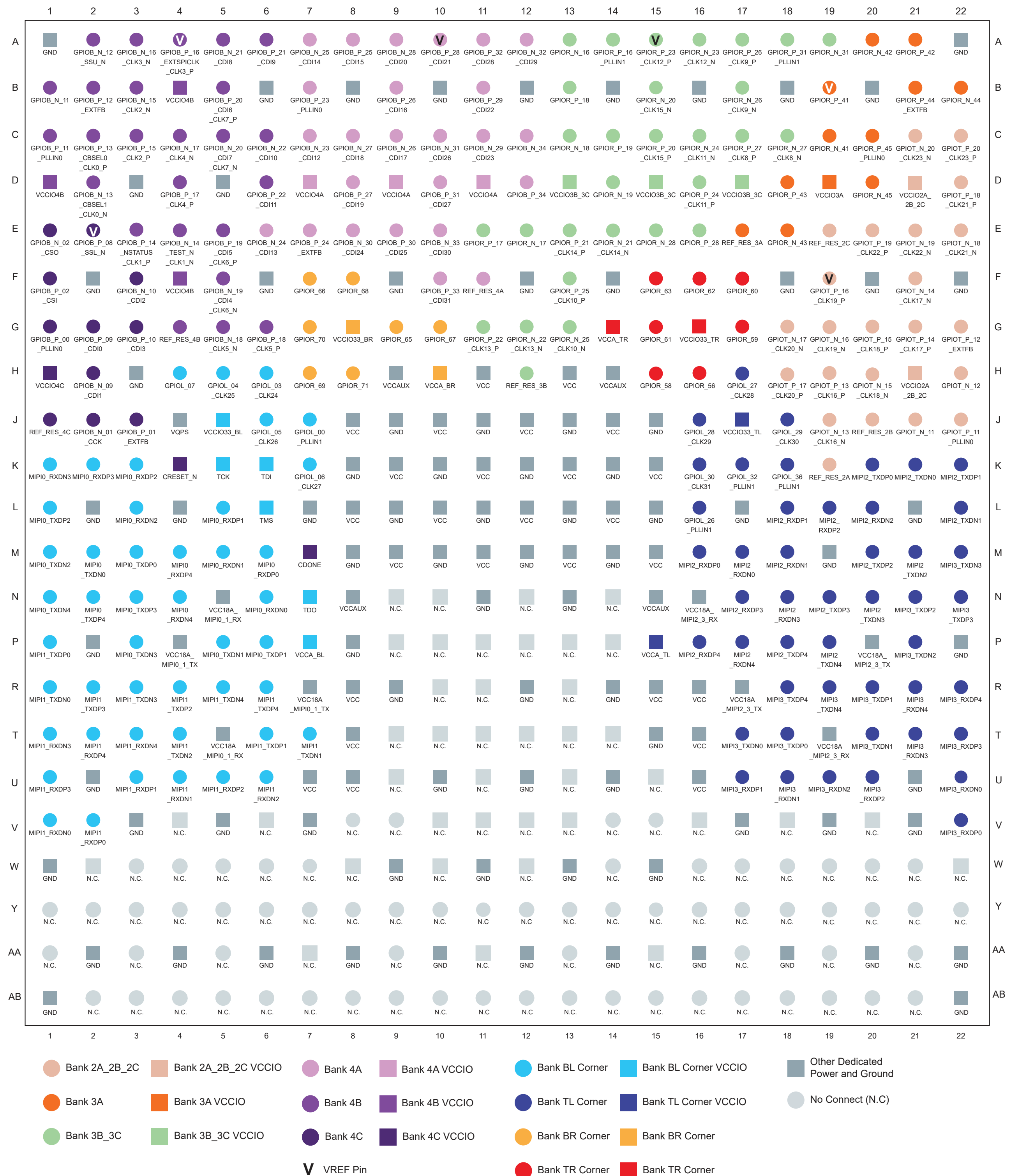


Figure 38: 484-Ball (L) FBGA Emulated MIPI RX Groups

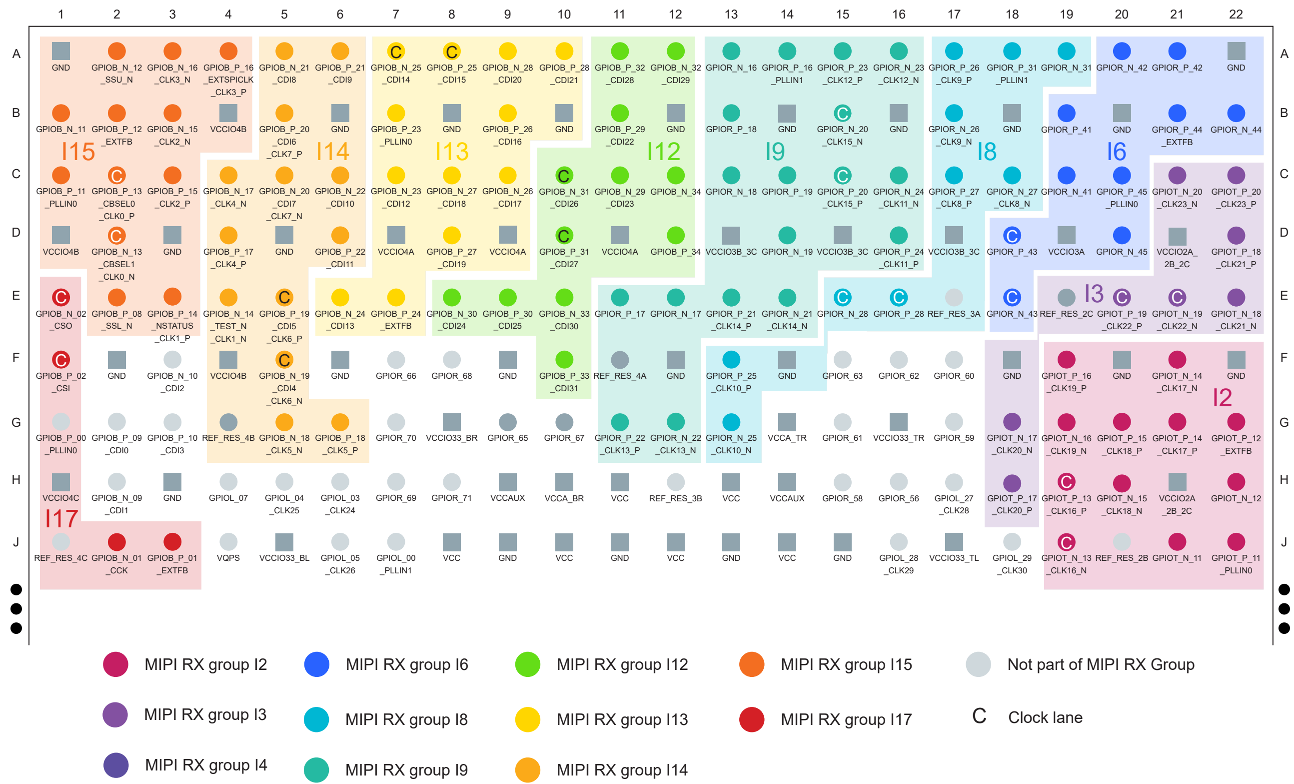


Figure 39: 484-Ball (L) FBGA Package Marking

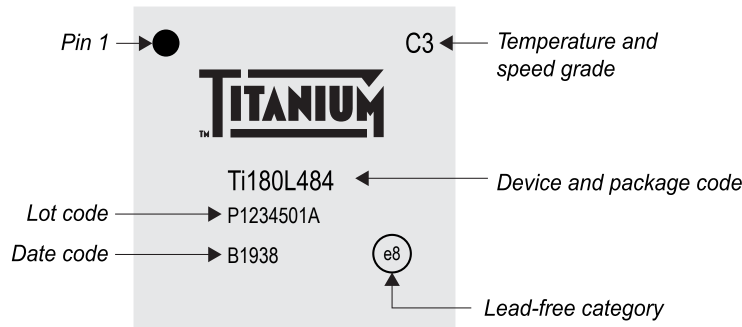
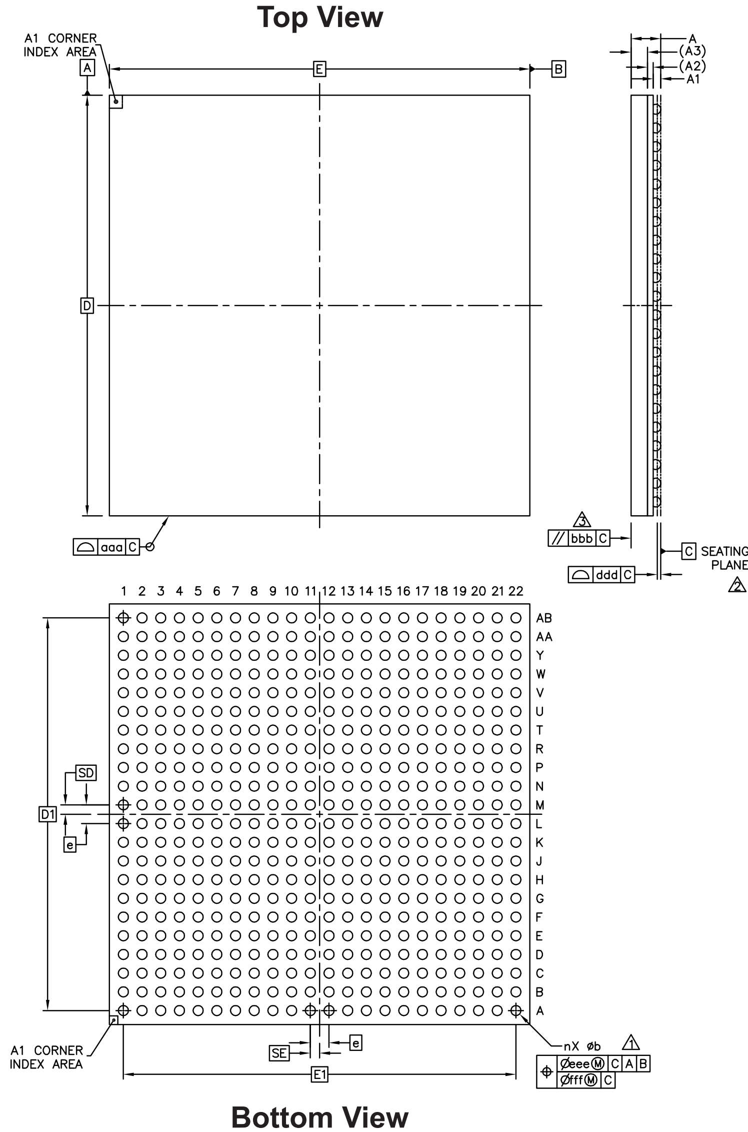


Figure 40: 484-Ball (L) FBGA Package Outline



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	1.193	1.268	1.4
STAND OFF	A1	0.27	0.32	0.37
SUBSTRATE THICKNESS	A2		0.248	REF
MOLD THICKNESS	A3		0.7	REF
BODY SIZE	D		18	BSC
	E		18	BSC
BALL DIAMETER			0.4	
BALL OPENING			0.35	
BALL WIDTH	b	0.38	0.43	0.48
BALL PITCH	e		0.8	BSC
BALL COUNT	n		484	
EDGE BALL CENTER TO CENTER	D1		16.8	BSC
	E1		16.8	BSC
BODY CENTER TO CONTACT BALL	SD		0.4	BSC
	SE		0.4	BSC
PACKAGE EDGE TOLERANCE	aaa		0.15	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.15	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

484-Ball (M) FBGA Package Specifications

Figure 41: 484-Ball (M) FBGA Pinout Diagram

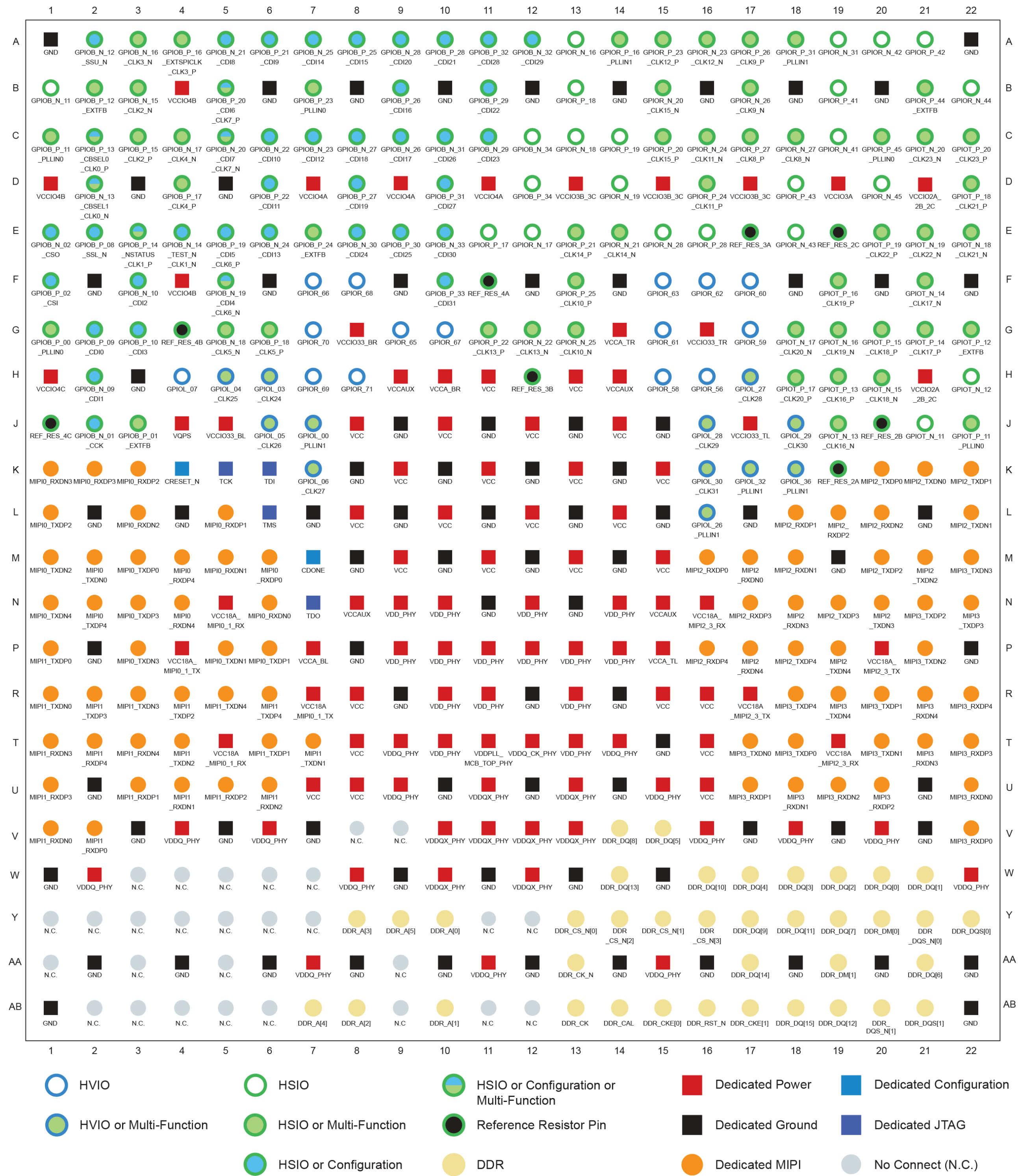


Figure 42: 484-Ball (M) FBGA I/O Bank Diagram

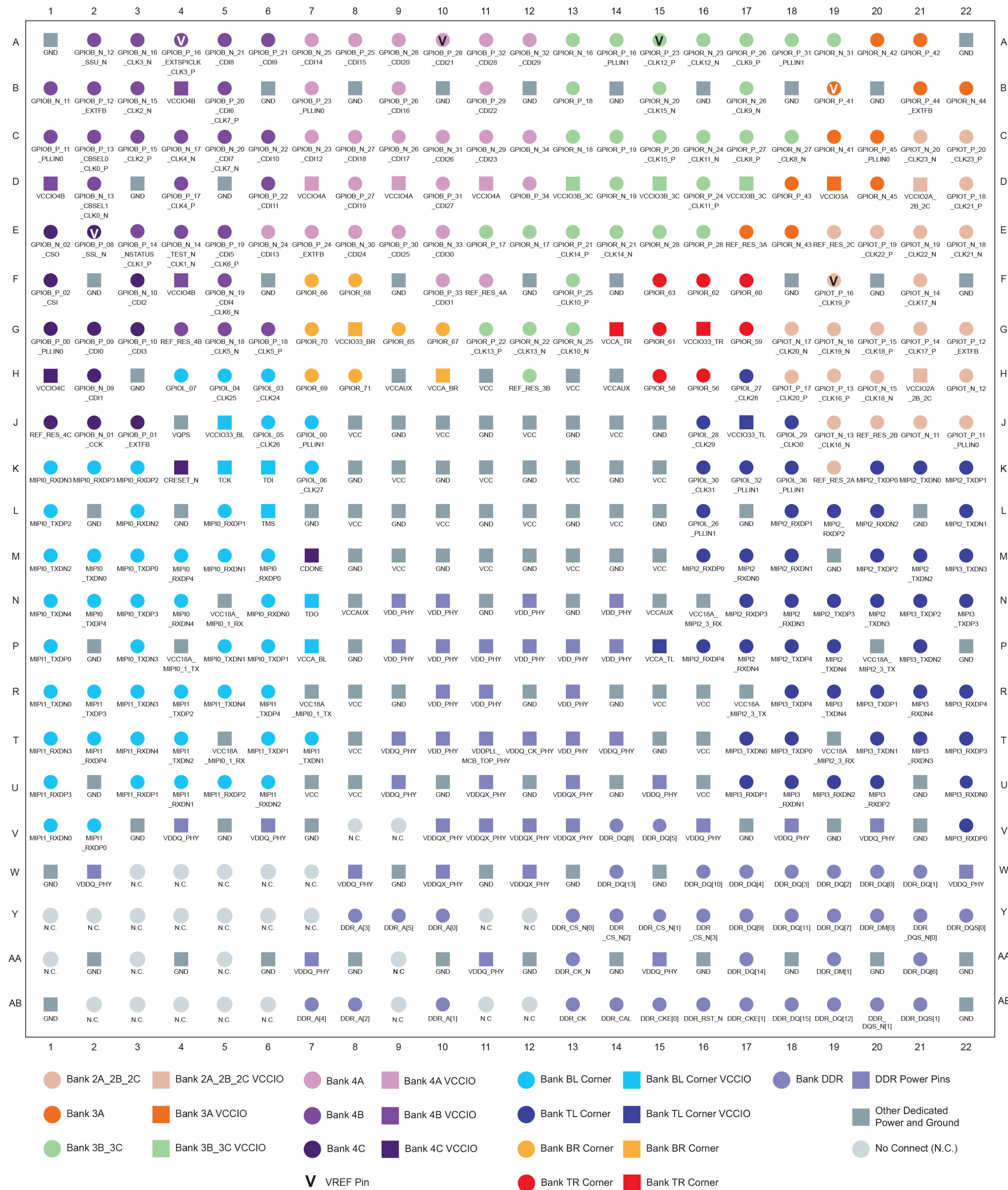


Figure 43: 484-Ball (M) FBGA Emulated MIPI RX Groups

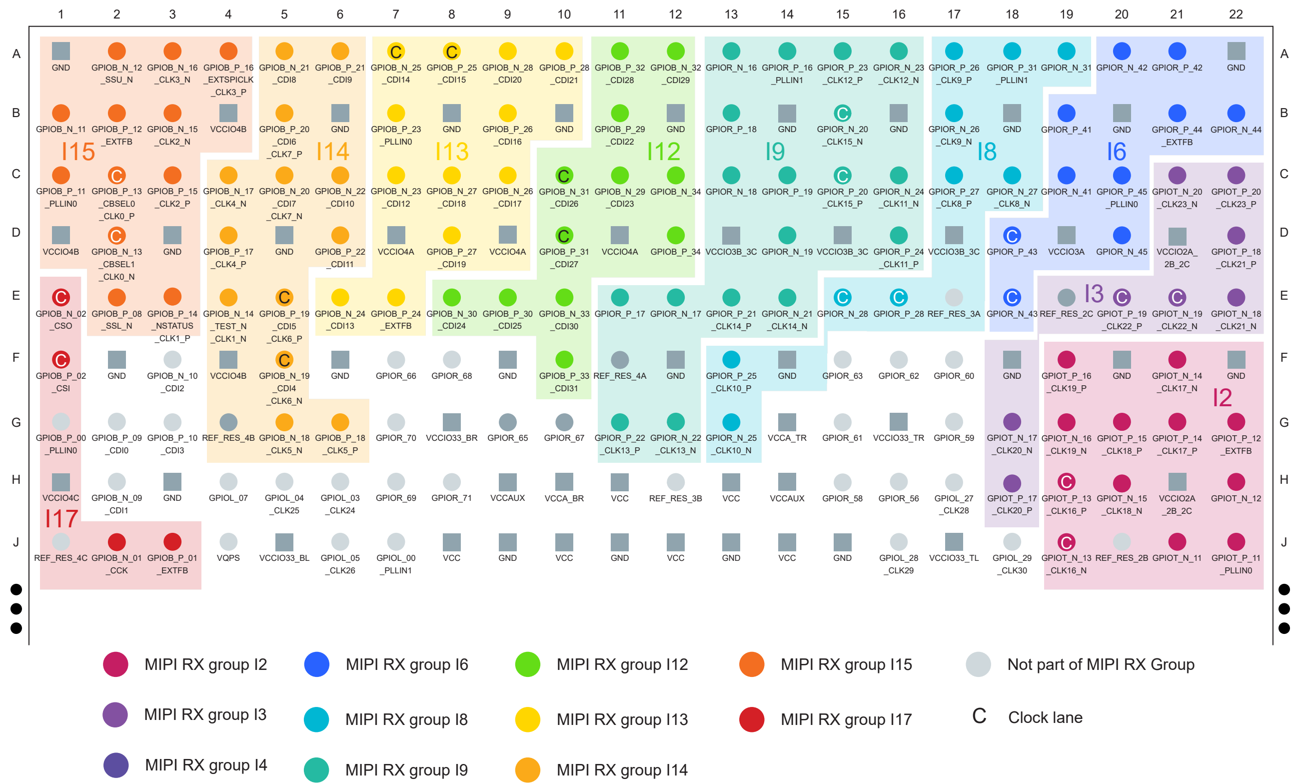


Figure 44: 484-Ball (M) FBGA Package Marking

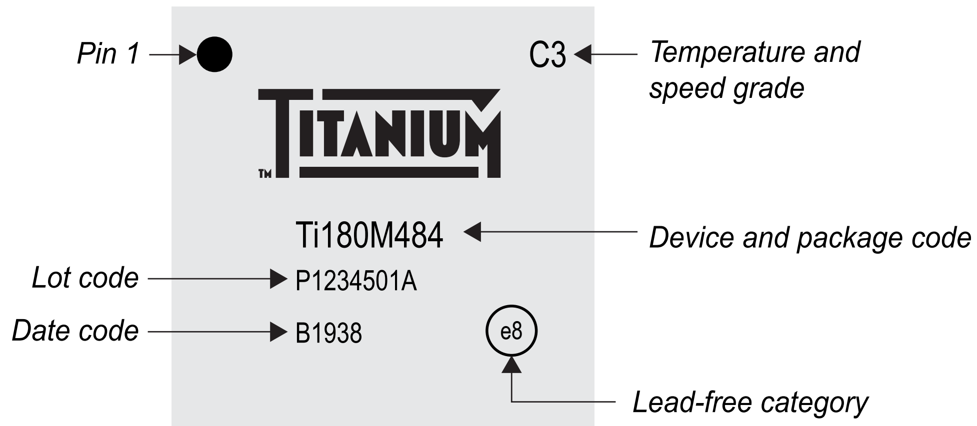
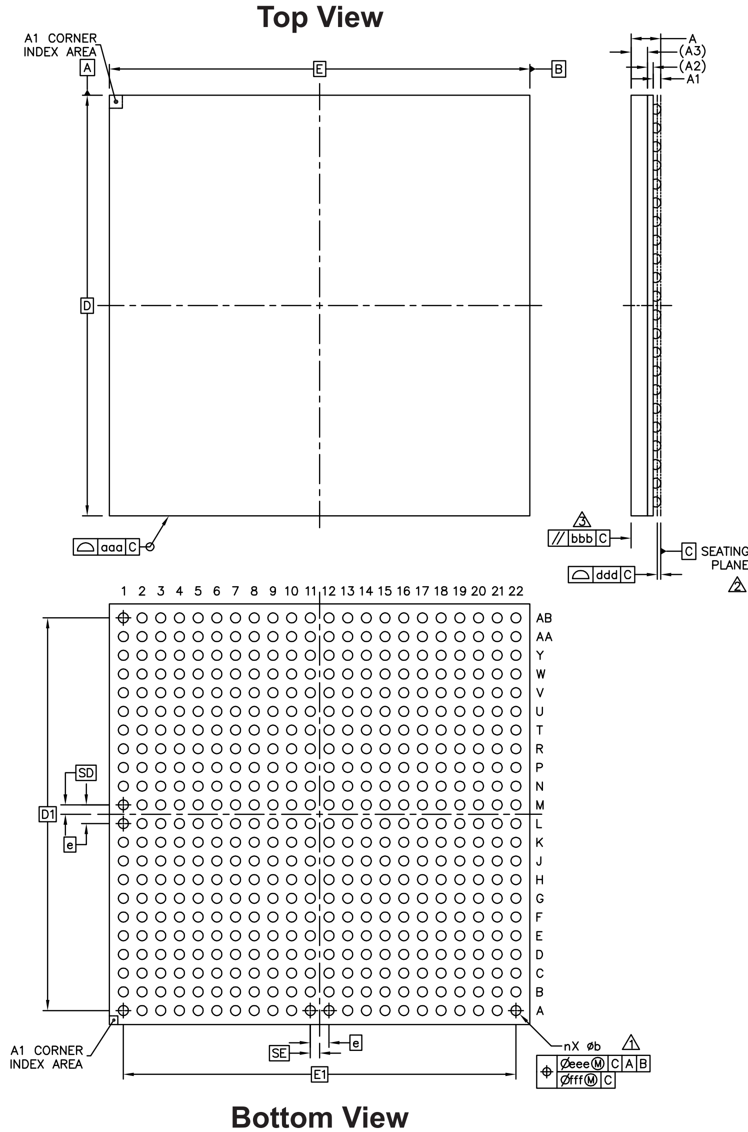


Figure 45: 484-Ball (M) FBGA Package Outline



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	1.193	1.268	1.4
STAND OFF	A1	0.27	0.32	0.37
SUBSTRATE THICKNESS	A2		0.248	REF
MOLD THICKNESS	A3		0.7	REF
BODY SIZE	D		18	BSC
	E		18	BSC
BALL DIAMETER			0.4	
BALL OPENING			0.35	
BALL WIDTH	b	0.38	0.43	0.48
BALL PITCH	e		0.8	BSC
BALL COUNT	n		484	
EDGE BALL CENTER TO CENTER	D1		16.8	BSC
	E1		16.8	BSC
BODY CENTER TO CONTACT BALL	SD		0.4	BSC
	SE		0.4	BSC
PACKAGE EDGE TOLERANCE	aaa		0.15	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.15	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

484-Ball (N) FBGA Package Specifications

Figure 46: 484-Ball (N) FBGA Pinout Diagram

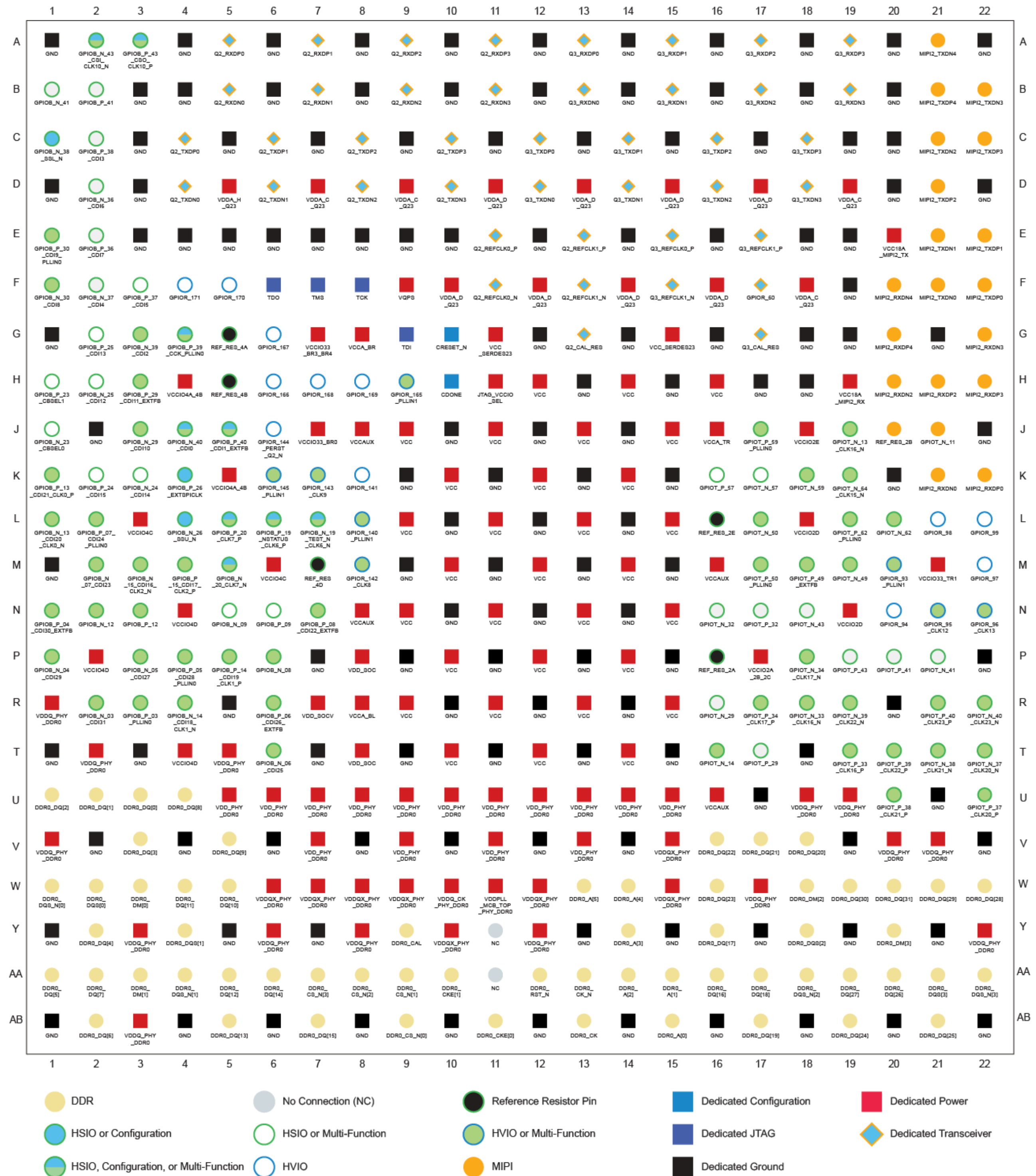


Figure 47: 484-Ball (N) FBGA I/O Bank Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
A	GND	GPIOB_N_43_CSI_CLK10_N	GPIOB_P_43_CSO_CLK10_P	GND	Q2_RXDP0	GND	Q2_RXDP1	GND	Q2_RXDP2	GND	Q2_RXDP3	GND	Q3_RXDP0	GND	Q3_RXDP1	GND	Q3_RXDP2	GND	Q3_RXDP3	GND	MIPI2_TXDN4	GND
B	GPIOB_N_41	GPIOB_P_41	GND	GND	Q2_RXDN0	GND	Q2_RXDN1	GND	Q2_RXDN2	GND	Q2_RXDN3	GND	Q3_RXDN0	GND	Q3_RXDN1	GND	Q3_RXDN2	GND	Q3_RXDN3	GND	MIPI2_TXDP4	MIPI2_TXDN3
C	GPIOB_N_38_SSL_N	GPIOB_P_38_CDI3	GND	Q2_TXDP0	GND	Q2_TXDP1	GND	Q2_TXDP2	GND	Q2_TXDP3	GND	Q3_TXDP0	GND	Q3_TXDP1	GND	Q3_TXDP2	GND	Q3_TXDP3	GND	GND	MIPI2_TXDN2	MIPI2_TXDP3
D	GND	GPIOB_N_36_CDI6	GND	Q2_TXDN0	VDDA_H_Q23	Q2_TXDN1	VDDA_C_Q23	Q2_TXDN2	VDDA_C_Q23	Q2_TXDN3	VDDA_D_Q23	Q3_TXDN0	VDDA_D_Q23	Q3_TXDN1	VDDA_D_Q23	Q3_TXDN2	VDDA_D_Q23	Q3_TXDN3	VDDA_C_Q23	GND	MIPI2_TXDP2	GND
E	GPIOB_P_30_CDI9_PLLIN0	GPIOB_P_36_CDI7	GND	GND	GND	GND	GND	GND	GND	GND	Q2_REFCLK0_P	GND	Q2_REFCLK1_P	GND	Q3_REFCLK0_P	GND	Q3_REFCLK1_P	GND	GND	VCC18A_MIPI2_TX	MIPI2_TXDN1	MIPI2_TXDP1
F	GPIOB_N_30_CDI8	GPIOB_N_37_CDI4	GPIOB_P_37_CDI5	GPIOR_171	GPIOR_170	TDO	TMS	TCK	VQPS	VDDA_D_Q23	Q2_REFCLK0_N	VDDA_D_Q23	Q2_REFCLK1_N	VDDA_D_Q23	Q3_REFCLK1_N	VDDA_D_Q23	GPIOR_60	VDDA_C_Q23	GND	MIPI2_RXDN4	MIPI2_TXDN0	MIPI2_TXDP0
G	GND	GPIOB_P_25_CDI13	GPIOB_N_39_CDI2	GPIOB_P_39_CCK_PLLIN0	REF_RES_4A	GPIOR_167	VCCIO33_BR3_BR4	VCCA_BR	TDI	CRESET_N	VCC_SERDES23	GND	Q2_CAL_RES	GND	VCC_SERDES23	GND	Q3_CAL_RES	GND	GND	MIPI2_RXDP4	GND	MIPI2_RXDN3
H	GPIOB_P_23_CBSEL1	GPIOB_N_25_CDI12	GPIOB_P_29_CDI11_EXTFB	VCCIO4A_4B	REF_RES_4B	GPIOR_166	GPIOR_168	GPIOR_169	GPIOR_165_PLLIN1	CDONE	JTAG_VCCIO_SEL	VCC	GND	VCC	GND	VCC	GND	GND	VCC18A_MIPI2_RX	MIPI2_RXDN2	MIPI2_RXDP2	MIPI2_RXDP3
J	GPIOB_N_23_CBSEL0	GND	GPIOB_N_29_CDI10	GPIOB_N_40_CDI0	GPIOB_P_40_CDI1_EXTFB	GPIOR_144_PERST_Q2_N	VCCIO33_BR0	VCCAUX	VCC	GND	VCC	GND	VCC	GND	VCC	VCCA_TR	GPIOT_P_59_PLLIN0	VCCIO2E	GPIOT_N_13_CLK16_N	REF_RES_2B	GPIOT_N_11	GND
K	GPIOB_P_13_CDI21_CLK0_P	GPIOB_P_24_CDI15	GPIOB_N_24_CDI14	GPIOB_P_26_EXTSPICLK	VCCIO4A_4B	GPIOR_145_PLLIN1	GPIOR_143_CLK9	GPIOR_141	GND	VCC	GND	VCC	GND	VCC	GND	GPIOT_P_57	GPIOT_N_57	GPIOT_N_59	GPIOT_N_64_CLK15_N	GND	MIPI2_RXDN0	MIPI2_RXDP0
L	GPIOB_N_13_CDI20_CLK0_N	GPIOB_P_07_CDI24_PLLIN0	VCCIO4C	GPIOB_N_26_SSU_N	GPIOB_P_20_CLK7_P	GPIOB_P_19_NSTATUS_CLK6_P	GPIOB_N_19_TEST_N_CLK6_N	GPIOR_140_PLLIN1	VCC	GND	VCC	GND	VCC	GND	VCC	REF_RES_2E	GPIOT_N_50	VCCIO2D	GPIOT_P_62_PLLIN0	GPIOT_N_62	GPIOR_98	GPIOR_99
M	GND	GPIOB_N_07_CDI23	GPIOB_N_15_CDI16_CLK2_N	GPIOB_P_15_CDI17_CLK2_P	GPIOB_N_20_CLK7_N	VCCIO4C	REF_RES_4D	GPIOR_142_CLK8	GND	VCC	GND	VCC	GND	VCC	GND	VCCAUX	GPIOT_P_50_PLLIN0	GPIOT_P_49_EXTFB	GPIOT_N_49	GPIOR_93_PLLIN1	VCCIO33_TR1	GPIOR_97
N	GPIOB_P_04_CDI30_EXTFB	GPIOB_N_12	GPIOB_P_12	VCCIO4D	GPIOB_N_09	GPIOB_P_09	GPIOB_P_08_CDI22_EXTFB	VCCAUX	VCC	GND	VCC	GND	VCC	GND	VCC	GPIOT_N_32	GPIOT_P_32	GPIOT_N_43	VCCIO2D	GPIOR_94	GPIOR_95_CLK12	GPIOR_96_CLK13
P	GPIOB_N_04_CDI29	VCCIO4D	GPIOB_N_05_CDI27	GPIOB_P_05_CDI28_PLLIN0	GPIOB_P_14_CDI19_CLK1_P	GPIOB_N_08	GND	VDD_SOC	GND	VCC	GND	VCC	GND	VCC	GND	REF_RES_2A	VCCIO2A_2B_2C	GPIOT_N_34_CLK17_N	GPIOT_P_43	GPIOT_P_41	GPIOT_N_41	GND
R	VDDQ_PHY_DDR0	GPIOB_N_03_CDI31	GPIOB_P_03_PLLIN0	GPIOB_N_14_CDI18_CLK1_N	GND	GPIOB_P_06_CDI26_EXTFB	VDD_SOCV	VCCA_BL	VCC	GND	VCC	GND	VCC	GND	VCC	GPIOT_N_29	GPIOT_P_34_CLK17_P	GPIOT_N_33_CLK16_N	GPIOT_N_39_CLK22_N	GND	GPIOT_P_40_CLK23_P	GPIOT_N_40_CLK23_N
T	GND	VDDQ_PHY_DDR0	GND	VCCIO4D	VDDQ_PHY_DDR0	GPIOB_N_06_CDI25	GND	VDD_SOC	GND	VCC	GND	VCC	GND	VCC	GND	GPIOT_N_14	GPIOT_P_29	GND	GPIOT_P_33_CLK16_P	GPIOT_P_39_CLK22_P	GPIOT_N_38_CLK21_N	GPIOT_N_37_CLK20_N
U	DDR0_DQ[2]	DDR0_DQ[1]	DDR0_DQ[0]	DDR0_DQ[8]	VDD_PHY_DDR0	VDD_PHY_DDR0	VDD_PHY_DDR0	VDD_PHY_DDR0	VDD_PHY_DDR0	VDD_PHY_DDR0	VDD_PHY_DDR0	VDD_PHY_DDR0	VDD_PHY_DDR0	VDD_PHY_DDR0	VDD_PHY_DDR0	VCCAUX	GND	VDDQ_PHY_DDR0	VDDQ_PHY_DDR0	GPIOT_P_38_CLK21_P	GND	GPIOT_P_37_CLK20_P
V	VDDQ_PHY_DDR0	GND	DDR0_DQ[3]	GND	DDR0_DQ[9]	GND	VDD_PHY_DDR0	GND	VDD_PHY_DDR0	GND	VDD_PHY_DDR0	GND	VDD_PHY_DDR0	GND	VDDQX_PHY_DDR0	DDR0_DQ[22]	DDR0_DQ[21]	DDR0_DQ[20]	GND	VDDQ_PHY_DDR0	VDDQ_PHY_DDR0	GND
W	DDR0_DQS_N[0]	DDR0_DQS[0]	DDR0_DM[0]	DDR0_DQ[11]	DDR0_DQ[10]	VDDQX_PHY_DDR0	VDDQX_PHY_DDR0	VDDQX_PHY_DDR0	VDDQX_PHY_DDR0	VDDQ_CK_PHY_DDR0	VDDPLL_MCB_TOP_PHY_DDR0	VDDQX_PHY_DDR0	DDR0_A[5]	DDR0_A[4]	VDDQX_PHY_DDR0	DDR0_DQ[23]	VDDQ_PHY_DDR0	DDR0_DM[2]	DDR0_DQ[30]	DDR0_DQ[31]	DDR0_DQ[29]	DDR0_DQ[28]
Y	GND	DDR0_DQ[4]	VDDQ_PHY_DDR0	DDR0_DQS[1]	GND	VDDQ_PHY_DDR0	GND	VDDQ_PHY_DDR0	DDR0_CAL	VDDQX_PHY_DDR0	NC	VDDQ_PHY_DDR0	GND	DDR0_A[3]	GND	DDR0_DQ[17]	GND	DDR0_DQS[2]	GND	DDR0_DM[3]	GND	VDDQ_PHY_DDR0
AA	DDR0_DQ[5]	DDR0_DQ[7]	DDR0_DM[1]	DDR0_DQS_N[1]	DDR0_DQ[12]	DDR0_DQ[14]	DDR0_CS_N[3]	DDR0_CS_N[2]	DDR0_CS_N[1]	DDR0_CKE[1]	NC	DDR0_RST_N	DDR0_CK_N	DDR0_A[2]	DDR0_A[1]	DDR0_DQ[16]	DDR0_DQ[18]	DDR0_DQS_N[2]	DDR0_DQ[27]	DDR0_DQ[26]	DDR0_DQS[3]	DDR0_DQS_N[3]
AB	GND	DDR0_DQ[6]	VDDQ_PHY_DDR0	GND	DDR0_DQ[13]	GND	DDR0_DQ[15]	GND	DDR0_CS_N[0]	GND	DDR0_CKE[0]	GND	DDR0_CK	GND	DDR0_A[0]	GND	DDR0_DQ[19]	GND	DDR0_DQ[24]	GND	DDR0_DQ[25]	GND

Bank 2A_2B_2C | Bank 2A_2B_2C | Bank 4A_4B | Bank 4A_4B | Bank BR3_BR4 | Bank BR3_BR4 | DDR0 | Bank BL

Bank 2D | Bank 2D | Bank 4D | Bank 4D | Bank 4C | Bank 4C | TR1 | SERDES

Bank 2E | Bank 2E | Bank BR0_BR1_BR2 | Bank BR0_BR1_BR2 | Not Applicable (NA) | Not Applicable (NA) | TR | V VREF Pin

Figure 48: 484-Ball (N) FBGA Emulated MIPI RX Groups

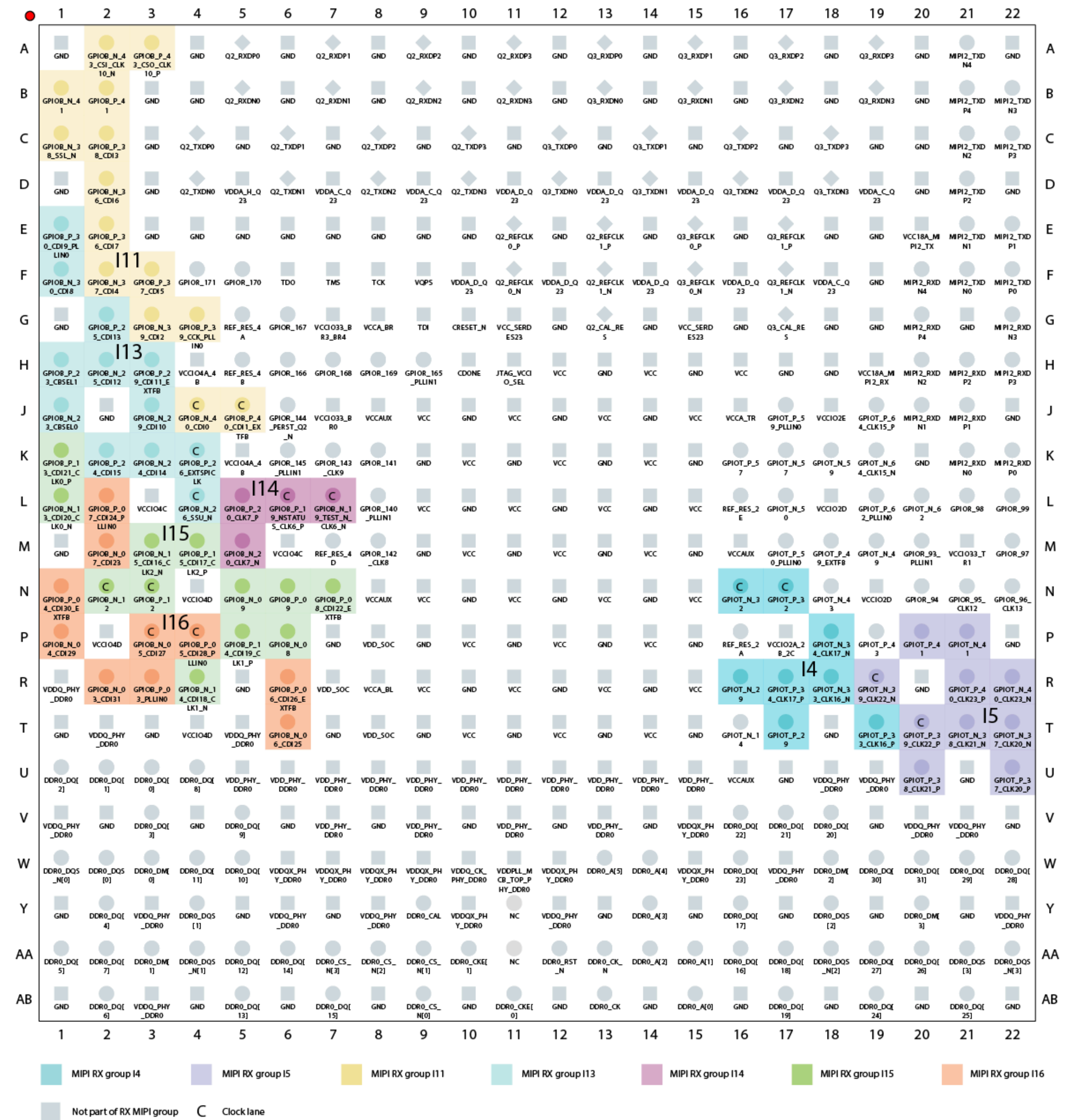


Figure 49: 484-Ball (N) FBGA Package Marking

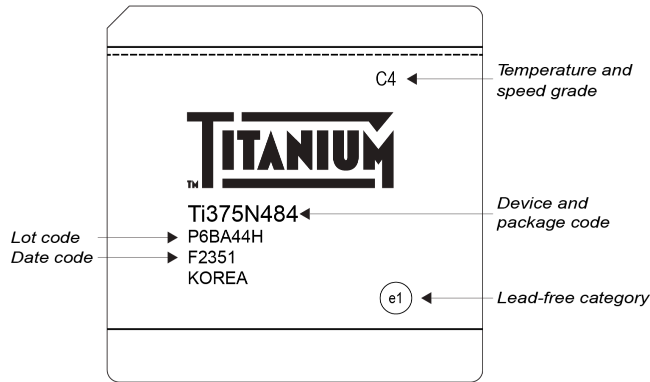


Figure 50: 484-Ball (N) FBGA Package Outline

Top View

Side View

Bottom View

DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A	2.035	2.188	2.341
A1	0.300	0.400	0.500
A2	1.672	1.788	1.904
b	0.400	0.500	0.600
NUMBER OF BALL 484			

NOTES:

1. All DIMENSIONS AND TOLERANCE CONFORM TO ASME Y14.5M-2018.
2. TERMINAL POSITIONS DESIGNATION PER JESD 95.
3. CORNER DETAILS PER JCET OPTION.
4. PIN 1 IDENTIFIER CAN BE CHAMFER, INK MARK, LASERED MARK, METALLIZED MARK.
5. BALL DIAMETER AFTER REFLOW.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM C.
7. USING ⌀0.500MM RAW SOLDER BALL SIZE DURING ASSEMBLY.

529-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

529-Ball (G) FBGA Package Specifications

Figure 51: 529-Ball (G) FBGA Pinout Diagram

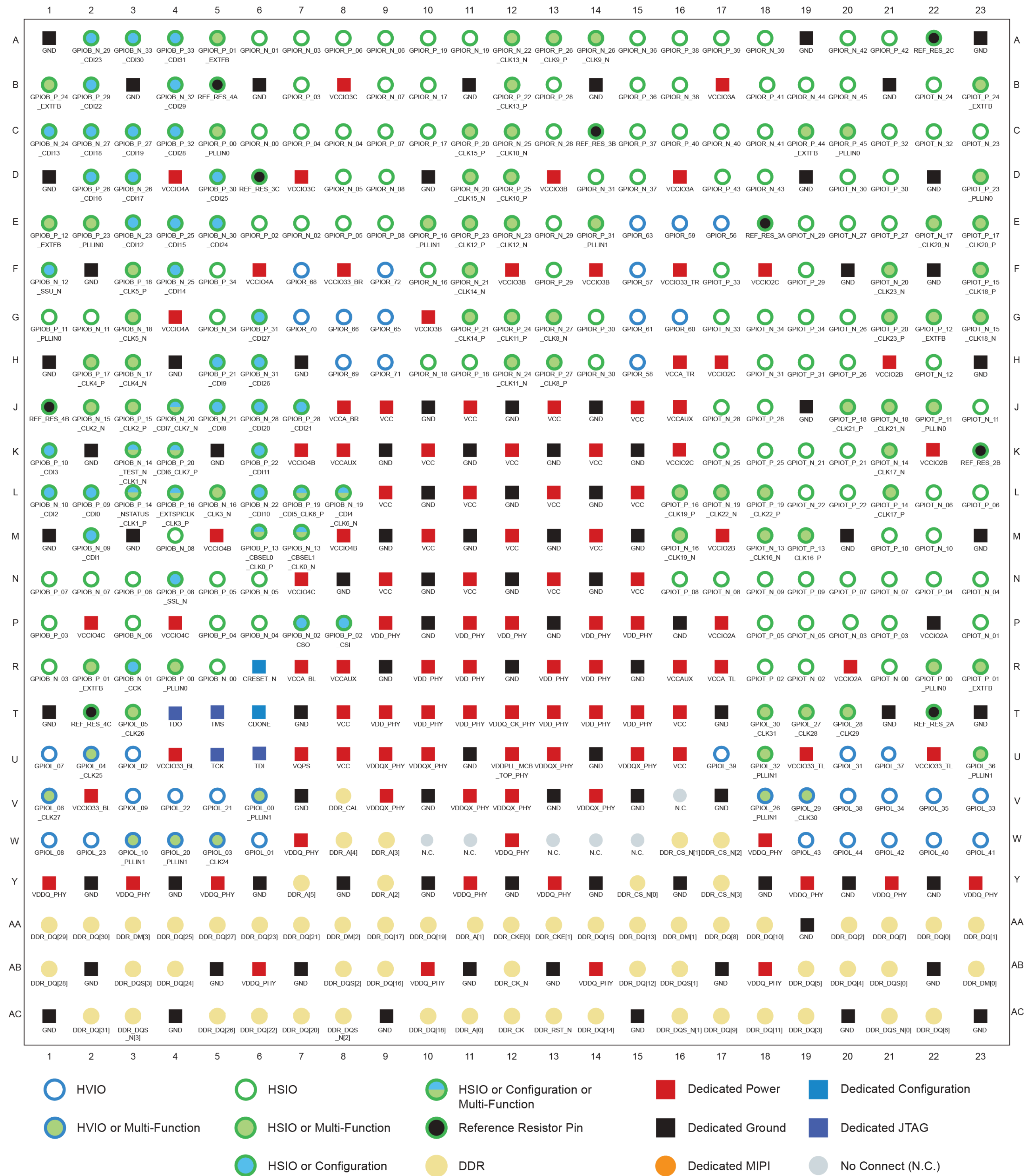


Figure 52: 529-Ball (G) FBGA I/O Bank Diagram

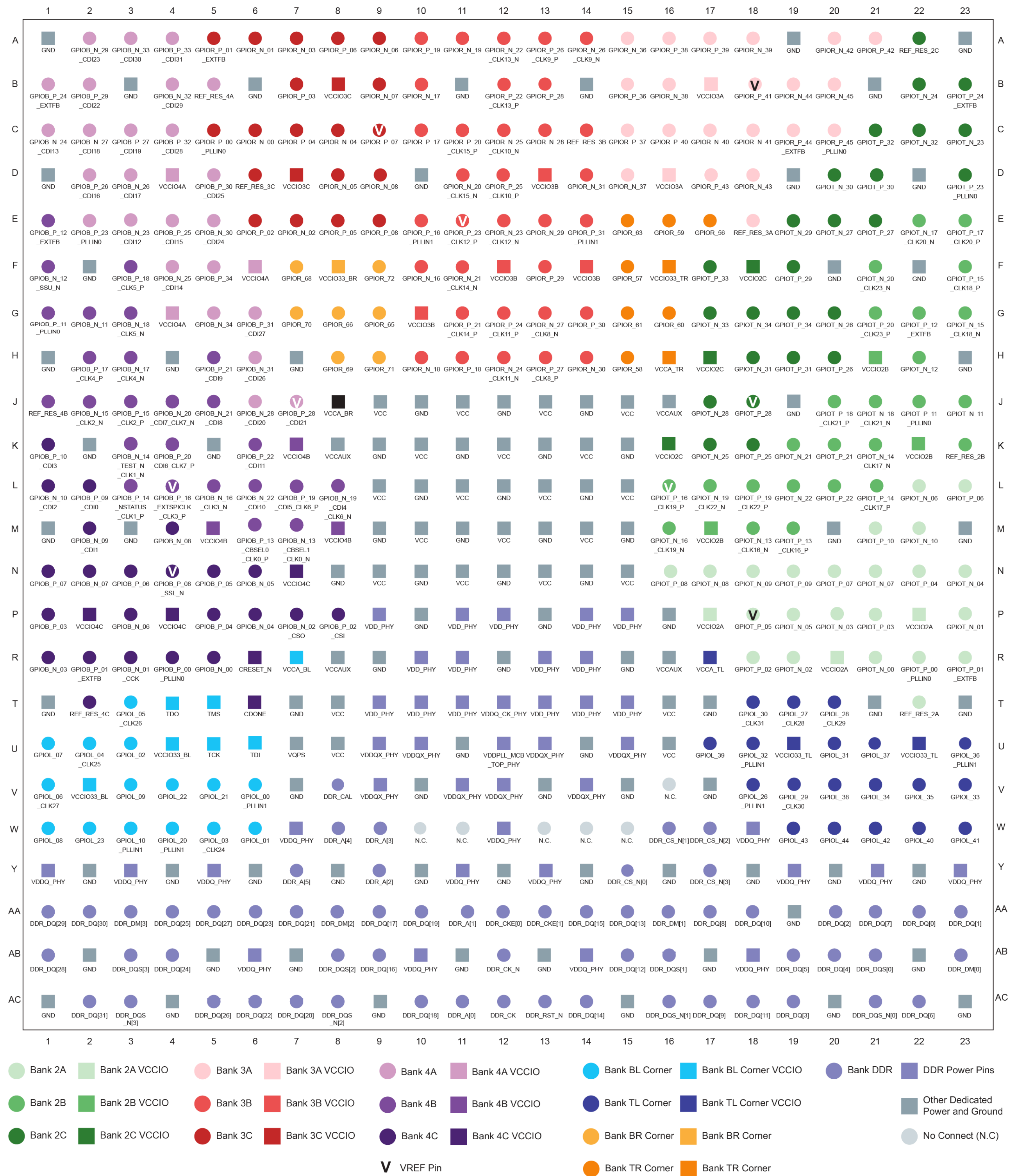


Figure 53: 529-Ball (G) FBGA Emulated MIPI RX Groups

MIPI RX group I0
MIPI RX group I1
MIPI RX group I2
MIPI RX group I3
MIPI RX group I4
MIPI RX group I5
MIPI RX group I6
MIPI RX group I7
MIPI RX group I8
MIPI RX group I9
MIPI RX group I11
MIPI RX group I12
MIPI RX group I13
MIPI RX group I14
MIPI RX group I15
MIPI RX group I16
MIPI RX group I17
Not part of MIPI RX Group
C Clock lane

Figure 54: 529-Ball (G) FBGA Package Marking

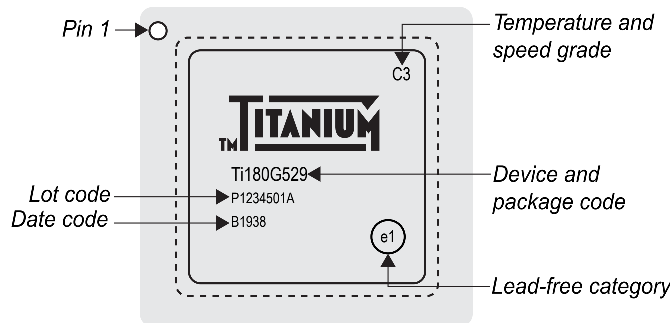
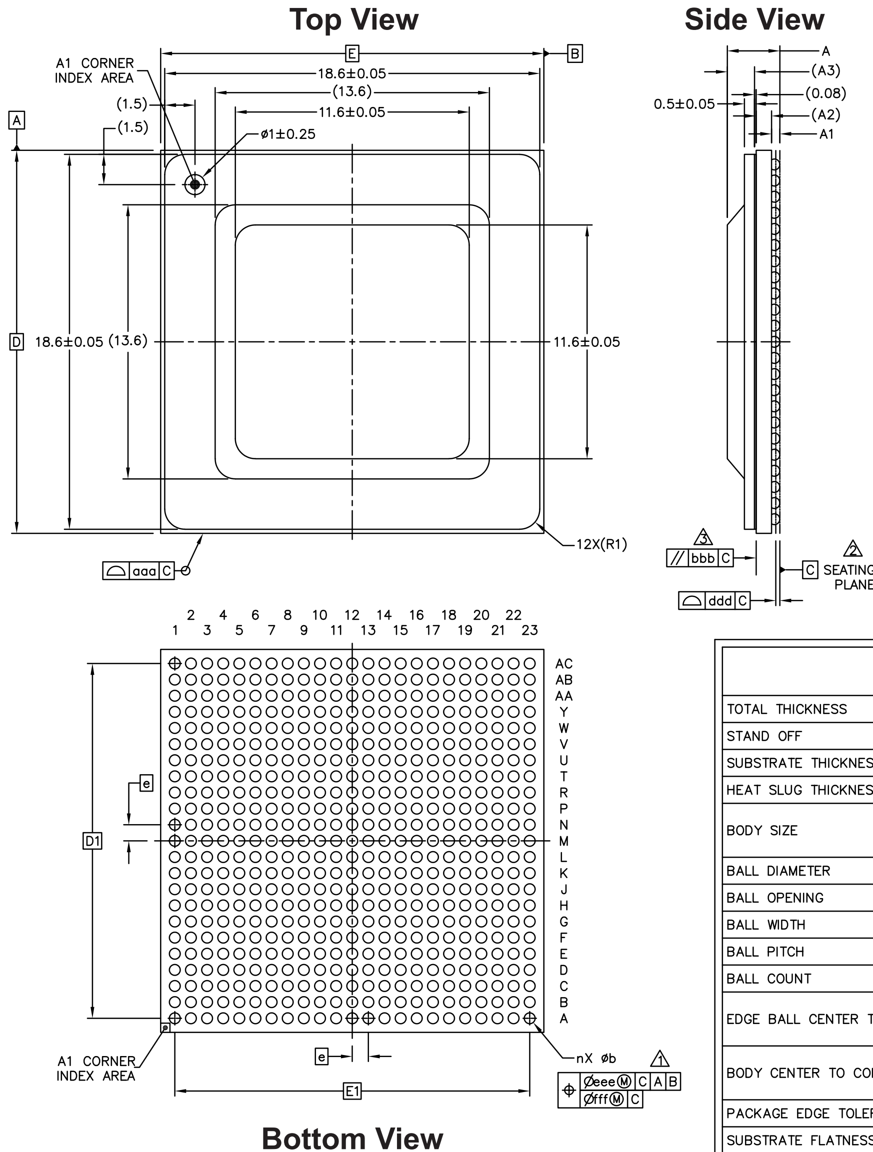


Figure 55: 529-Ball (G) FBGA Package Outline



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	2.72
STAND OFF	A1	0.36	---	0.46
SUBSTRATE THICKNESS	A2		0.765	REF
HEAT SLUG THICKNESS	A3		1.35	REF
BODY SIZE	D		19	BSC
	E		19	BSC
BALL DIAMETER			0.5	
BALL OPENING			0.4	
BALL WIDTH	b	0.44	---	0.64
BALL PITCH	e		0.8	BSC
BALL COUNT	n		529	
EDGE BALL CENTER TO CENTER	D1		17.6	BSC
	E1		17.6	BSC
BODY CENTER TO CONTACT BALL	SD		---	BSC
	SE		---	BSC
PACKAGE EDGE TOLERANCE	aaa		0.15	
SUBSTRATE FLATNESS	bbb		0.25	
COPLANARITY	ddd		0.2	
BALL OFFSET (PACKAGE)	eee		0.25	
BALL OFFSET (BALL)	fff		0.1	

NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

529-Ball (C) FBGA Package Specifications

Figure 56: 529-Ball (C) FBGA Pinout Diagram

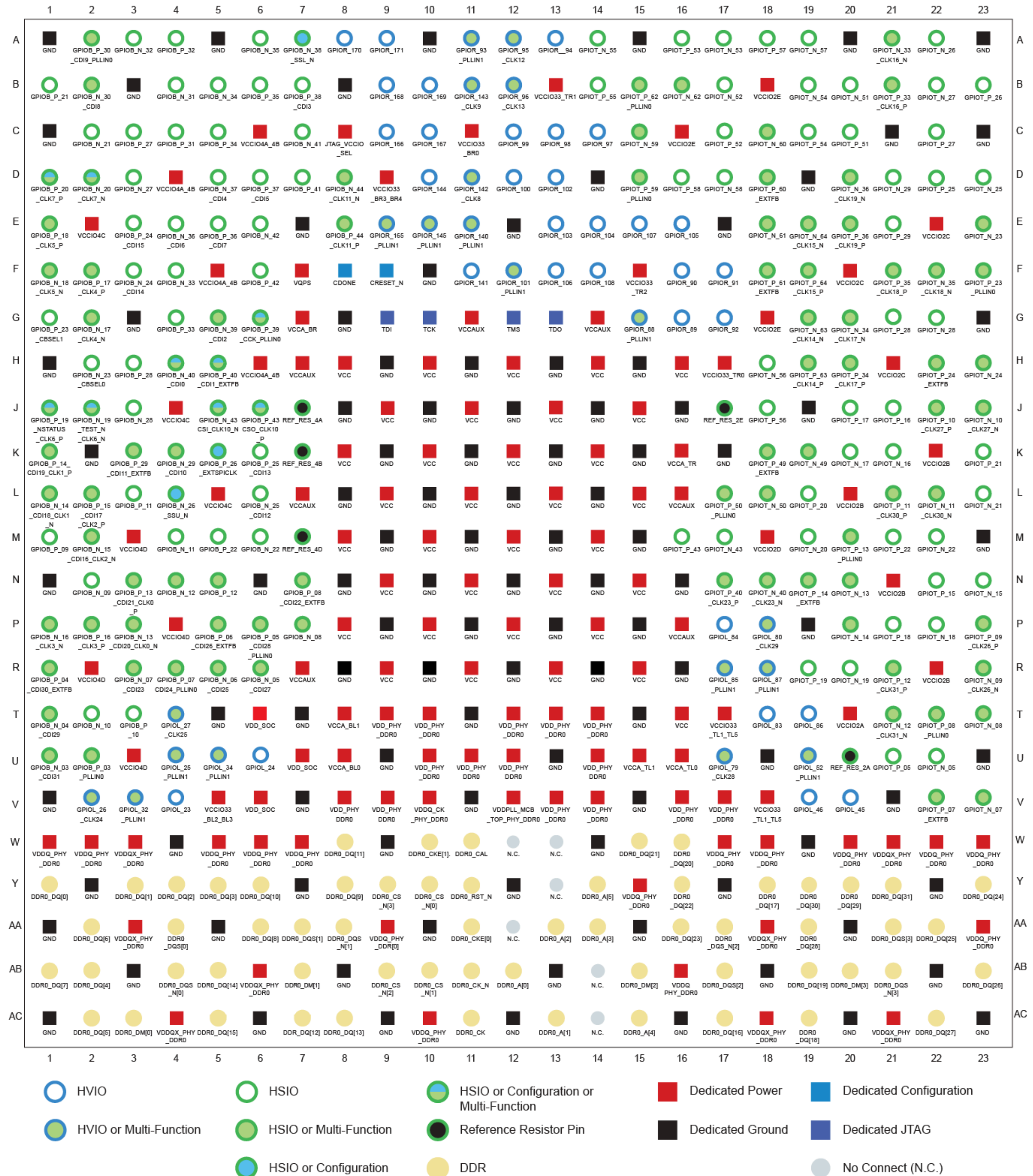


Figure 57: 529-Ball (C) FBGA I/O Bank Diagram

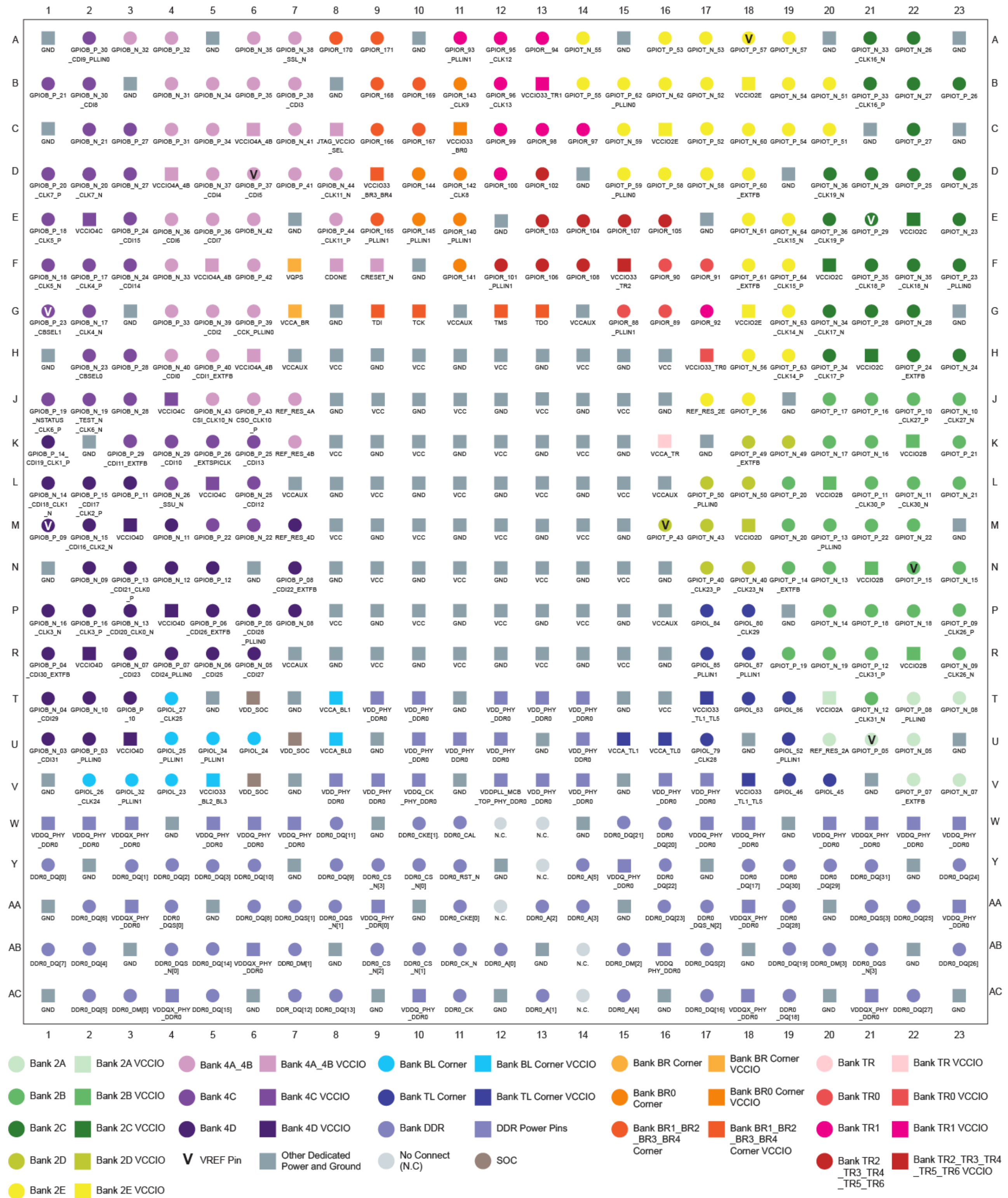


Figure 58: 529-Ball (C) FBGA Emulated MIPI RX Groups

	1	2	3	4	5	6	7	8	9	10	11	12
A	GND	GPIOB_P_30_CDI9_PLLIN0	GPIOB_N_32	GPIOB_P_32	GND	GPIOB_N_35	GPIOB_N_38_SSL_N	GPIOR_170	GPIOR_171	GND	GPIOR_93_PLLIN1	GPIOR_95_CLK12
B	GPIOB_P_21	GPIOB_N_30_CDI8	GND	GPIOB_N_31	GPIOB_N_34	GPIOB_P_35	GPIOB_P_38_CDI3	GND	GPIOR_168	GPIOR_169	GPIOR_143_CLK9	GPIOR_96_CLK13
C	GND	GPIOB_N_21	GPIOB_P_27	GPIOB_P_31	GPIOB_P_34	VCCIO4A_4B	GPIOB_N_41	JTAG_VCCIO_SEL	GPIOR_166	GPIOR_167	VCCIO33_BR0	GPIOR_99
D	GPIOB_P_20_CLK7_P	GPIOB_N_20_CLK7_N	GPIOB_N_27	VCCIO4A_4B	GPIOB_N_37_CDI4	GPIOB_P_37_CDI5	GPIOB_P_41	GPIOB_N_44_CLK11_N	VCCIO33_BR3_BR4	GPIOR_144	GPIOR_142_CLK8	GPIOR_100
E	GPIOB_P_18_CLK5_P	VCCIO4C	GPIOB_P_24_CDI15	GPIOB_N_36_CDI6	GPIOB_P_36_CDI7	GPIOB_N_42	GND	GPIOB_P_44_CLK11_P	GPIOR_165_PLLIN1	GPIOR_145_PLLIN1	GPIOR_140_PLLIN1	GND
F	GPIOB_N_18_CLK5_N	GPIOB_P_17_CLK4_P	GPIOB_N_24_CDI14	GPIOB_N_33	VCCIO4A_4B	GPIOB_P_42	VQPS	CDONE	CRESET_N	GND	GPIOR_141	GPIOR_101_PLLIN1
G	GPIOB_P_23_CBSEL1	GPIOB_N_17_CLK4_N	GND	GPIOB_P_33	GPIOB_N_39_CDI2	GPIOB_P_39_CCK_PLLIN0	VCCA_BR	GND	TDI	TCK	VCCAUX	TMS
H	GND	GPIOB_N_23_CBSEL0	GPIOB_P_28	GPIOB_N_40_CDI0	GPIOB_P_40_CDI1_EXTFB	VCCIO4A_4B	VCCAUX	VCC	GND	VCC	GND	VCC
J	GPIOB_P_19_NSTATUS_CLK6_P	GPIOB_N_19_TEST_N_CLK6_N	GPIOB_N_28	VCCIO4C	GPIOB_N_43 CSI_CLK10_N	GPIOB_P_43 CSO_CLK10_P	REF_RES_4A	GND	VCC	GND	VCC	GND
K	GPIOB_P_14_CDI19_CLK1_P	GND	GPIOB_P_29_CDI11_EXTFB	GPIOB_N_29_CDI10	GPIOB_P_26_EXTSPICLK	GPIOB_P_25_CDI13	REF_RES_4B	VCC	GND	VCC	GND	VCC
L	GPIOB_N_14_CDI18_CLK1_N	GPIOB_P_15_CDI17_CLK2_P	GPIOB_P_11	GPIOB_N_26_SSU_N	VCCIO4C	GPIOB_N_25_CDI12	VCCAUX	GND	VCC	GND	VCC	GND
M	GPIOB_P_09	GPIOB_N_15_CDI16_CLK2_N	VCCIO4D	GPIOB_N_11	GPIOB_P_22	GPIOB_N_22	REF_RES_4D	VCC	GND	VCC	GND	VCC
N	GND	GPIOB_N_09	GPIOB_P_13_CDI21_CLK0_P	GPIOB_N_12	GPIOB_P_12	GND	GPIOB_P_08_CDI22_EXTFB	GND	VCC	GND	VCC	GND
P	GPIOB_N_16_CLK3_N	GPIOB_P_16_CLK3_P	GPIOB_N_13_CDI20_CLK0_N	VCCIO4D	GPIOB_P_06_CDI26_EXTFB	GPIOB_P_05_CDI28_PLLIN0	GPIOB_N_08	VCC	GND	VCC	GND	VCC
R	GPIOB_P_04_CDI30_EXTFB	VCCIO4D	GPIOB_N_07_CDI23	GPIOB_P_07 CDI24_PLLIN0	GPIOB_N_06_CDI25	GPIOB_N_05_CDI27	VCCAUX	GND	VCC	GND	VCC	GND
T	GPIOB_N_04_CDI29	GPIOB_N_10	GPIOB_P_10	GPIOL_27_CLK25	GND	VDD_SOC	GND	VCCA_BL1	VDD_PHY_DDR0	VDD_PHY_DDR0	GND	VDD_PHY_DDR0
U	GPIOB_N_03_CDI31	GPIOB_P_03_PLLIN0	VCCIO4D	GPIOL_25_PLLIN1	GPIOL_34_PLLIN1	GPIOL_24	VDD_SOC	VCCA_BL0	GND	VDD_PHY_DDR0	VDD_PHY DDR0	VDD_PHY DDR0

	13	14	15	16	17	18	19	20	21	22	23
A	GPIOR__94	GPIOT_N_55	GND	GPIOT_P_53	GPIOT_N_53	GPIOT_P_57	GPIOT_N_57	GND	GPIOT_N_33_CLK16_N	GPIOT_N_26	GND
B	VCCIO33_TR1	GPIOT_P_55	GPIOT_P_62_PLLIN0	GPIOT_N_62	GPIOT_N_52	VCCIO2E	GPIOT_N_54	GPIOT_N_51	GPIOT_P_33_CLK16_P	GPIOT_N_27	GPIOT_P_26
C	GPIOR_98	GPIOR_97	GPIOT_N_59	VCCIO2E	GPIOT_P_52	GPIOT_N_60	GPIOT_P_54	GPIOT_P_51	GND	GPIOT_P_27	GND
D	GPIOR_102	GND	GPIOT_P_59_PLLIN0	GPIOT_P_58	GPIOT_N_58	GPIOT_P_60_EXTFB	GND	GPIOT_N_36_CLK19_N	GPIOT_N_29	GPIOT_P_25	GPIOT_N_25
E	GPIOR_103	GPIOR_104	GPIOR_107	GPIOR_105	GND	GPIOT_N_61	GPIOT_N_64_CLK15_N	GPIOT_P_36_CLK19_P	GPIOT_P_29	VCCIO2C	GPIOT_N_23
F	GPIOR_106	GPIOR_108	VCCIO33_TR2	GPIOR_90	GPIOR_91	GPIOT_P_61_EXTFB	GPIOT_P_64_CLK15_P	VCCIO2C	GPIOT_P_35_CLK18_P	GPIOT_N_35_CLK18_N	GPIOT_P_23_PLLIN0
G	TDO	VCCAUX	GPIOR_88_PLLIN1	GPIOR_89	GPIOR_92	VCCIO2E	GPIOT_N_63_CLK14_N	GPIOT_N_34_CLK17_N	GPIOT_P_28	GPIOT_N_28	GND
H	GND	VCC	GND	VCC	VCCIO33_TR0	GPIOT_N_56	GPIOT_P_63_CLK14_P	GPIOT_P_34_CLK17_P	VCCIO2C	GPIOT_P_24_EXTFB	GPIOT_N_24
J	VCC	GND	VCC	GND	REF_RES_2E	GPIOT_P_56	GND	GPIOT_P_17	GPIOT_P_16	GPIOT_P_10_CLK27_P	GPIOT_N_10_CLK27_N
K	GND	VCC	GND	VCCA_TR	GND	GPIOT_P_49_EXTFB	GPIOT_N_49	GPIOT_N_17	GPIOT_N_16	VCCIO2B	GPIOT_P_21
L	VCC	GND	VCC	VCCAUX	GPIOT_P_50_PLLIN0	GPIOT_N_50	GPIOT_P_20	VCCIO2B	GPIOT_P_11_CLK30_P	GPIOT_N_11_CLK30_N	GPIOT_N_21
M	GND	VCC	GND	GPIOT_P_43	GPIOT_N_43	VCCIO2D	GPIOT_N_20	GPIOT_P_13_PLLIN0	GPIOT_P_22	GPIOT_N_22	GND
N	VCC	GND	VCC	GND	GPIOT_P_40_CLK23_P	GPIOT_N_40_CLK23_N	GPIOT_P_14_EXTFB	GPIOT_N_13	VCCIO2B	GPIOT_P_15	GPIOT_N_15
P	GND	VCC	GND	VCCAUX	GPIOL_84	GPIOL_80_CLK29	GND	GPIOT_N_14	GPIOT_P_18	GPIOT_N_18	GPIOT_P_09_CLK26_P
R	VCC	GND	VCC	GND	GPIOL_85_PLLIN1	GPIOL_87_PLLIN1	GPIOT_P_19	GPIOT_N_19	GPIOT_P_12_CLK31_P	VCCIO2B	GPIOT_N_09_CLK26_N
T	VDD_PHY_DDR0	VDD_PHY_DDR0	GND	VCC	VCCIO33_TL1_TL5	GPIOL_83	GPIOL_86	VCCIO2A	GPIOT_N_12_CLK31_N	GPIOT_P_08_PLLIN0	GPIOT_N_08
U	GND	VDD_PHY DDR0	VCCA_TL1	VCCA_TL0	GPIOL_79_CLK28	GND	GPIOL_52_PLLIN1	REF_RES_2A	GPIOT_P_05	GPIOT_N_05	GND

MIPI RX group I1 · MIPI RX group I7 · MIPI RX group I12 · MIPI RX group I15 · Not part of MIPI RX Group

MIPI RX group I2 · MIPI RX group I8 · MIPI RX group I13 · MIPI RX group I16 · C Clock lane

MIPI RX group I3 · MIPI RX group I11 · MIPI RX group I14

Figure 59: 529-Ball (C) FBGA Package Marking

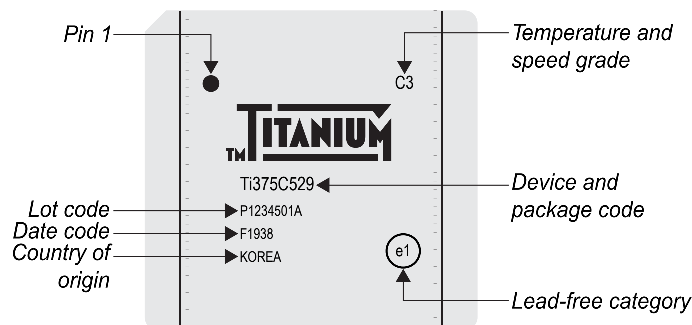
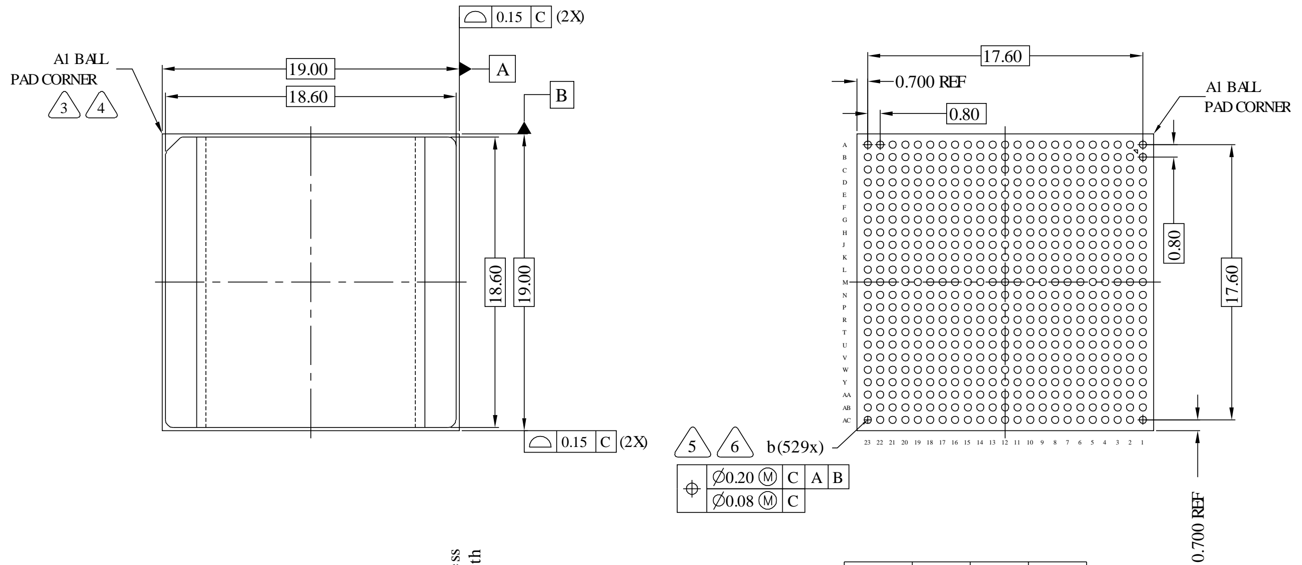


Figure 60: 529-Ball (C) FBGA Package Outline



DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A	2.015	2.168	2.321
A1	0.280	0.380	0.480
A2	1.672	1.788	1.904
b	0.400	0.500	0.600
NUMBER OF BALL 529			

NOTES:

1. All DIMENSIONS AND TOLERANCE CONFORM TO ASME Y14.5M-2018.
2. TERMINAL POSITIONS DESIGNATION PER JESD 95.
3. CORNER DETAILS PER JCET OPTION.
4. PIN 1 IDENTIFIER CAN BE CHAMFER, INK MARK, LASERED MARK, METALLIZED MARK.
5. BALL DIAMETER AFTER REFLOW.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM C.
7. USIN G ∅0.500MM RAW SOLDER BALL SIZE DURING ASSEMBLY.

1156-Ball (N) FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

Figure 61: 1156-Ball (N) FBGA Pinout Diagram (Part 1)

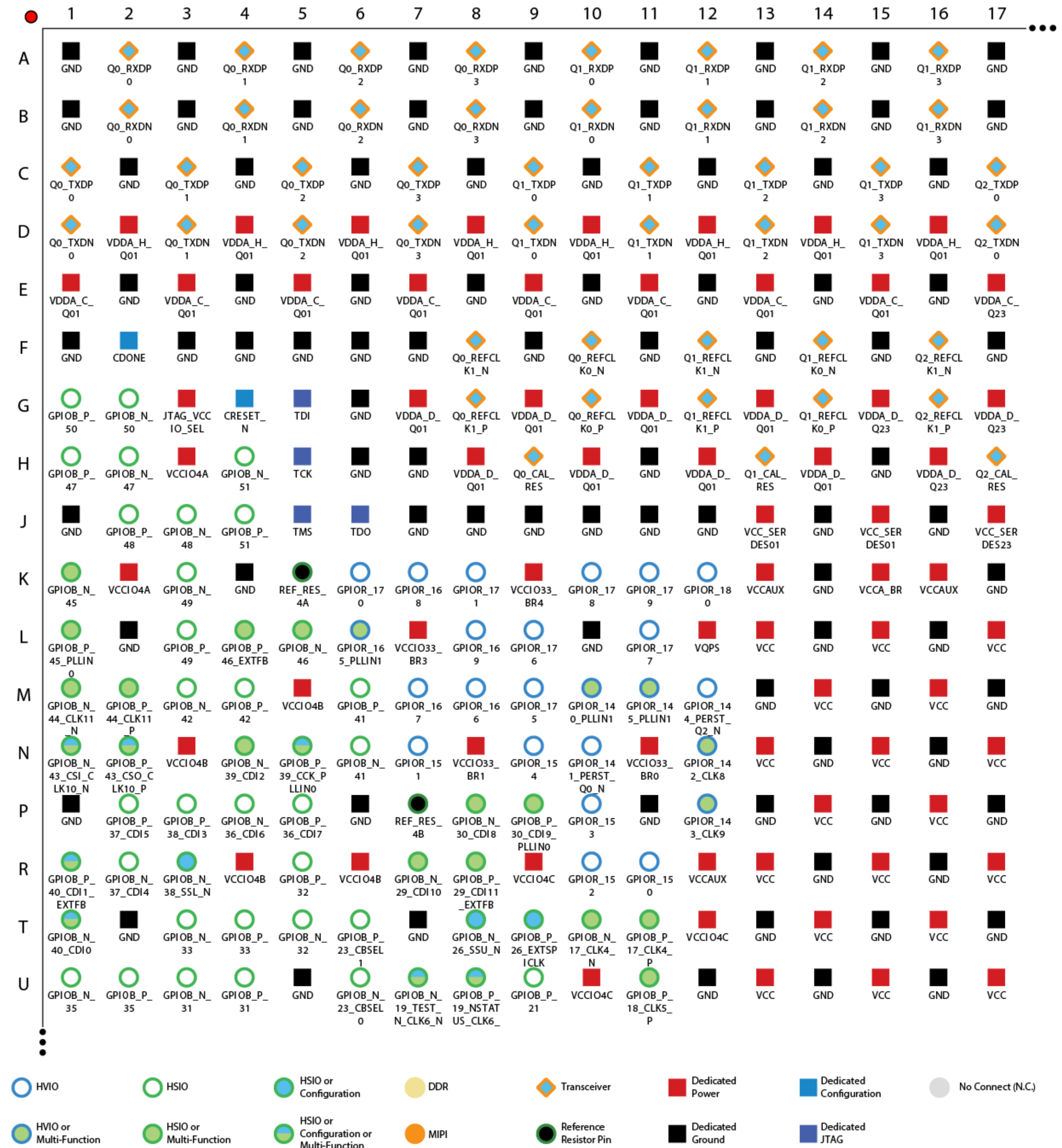


Figure 62: 1156-Ball (N) FBGA Pinout Diagram (Part 2)

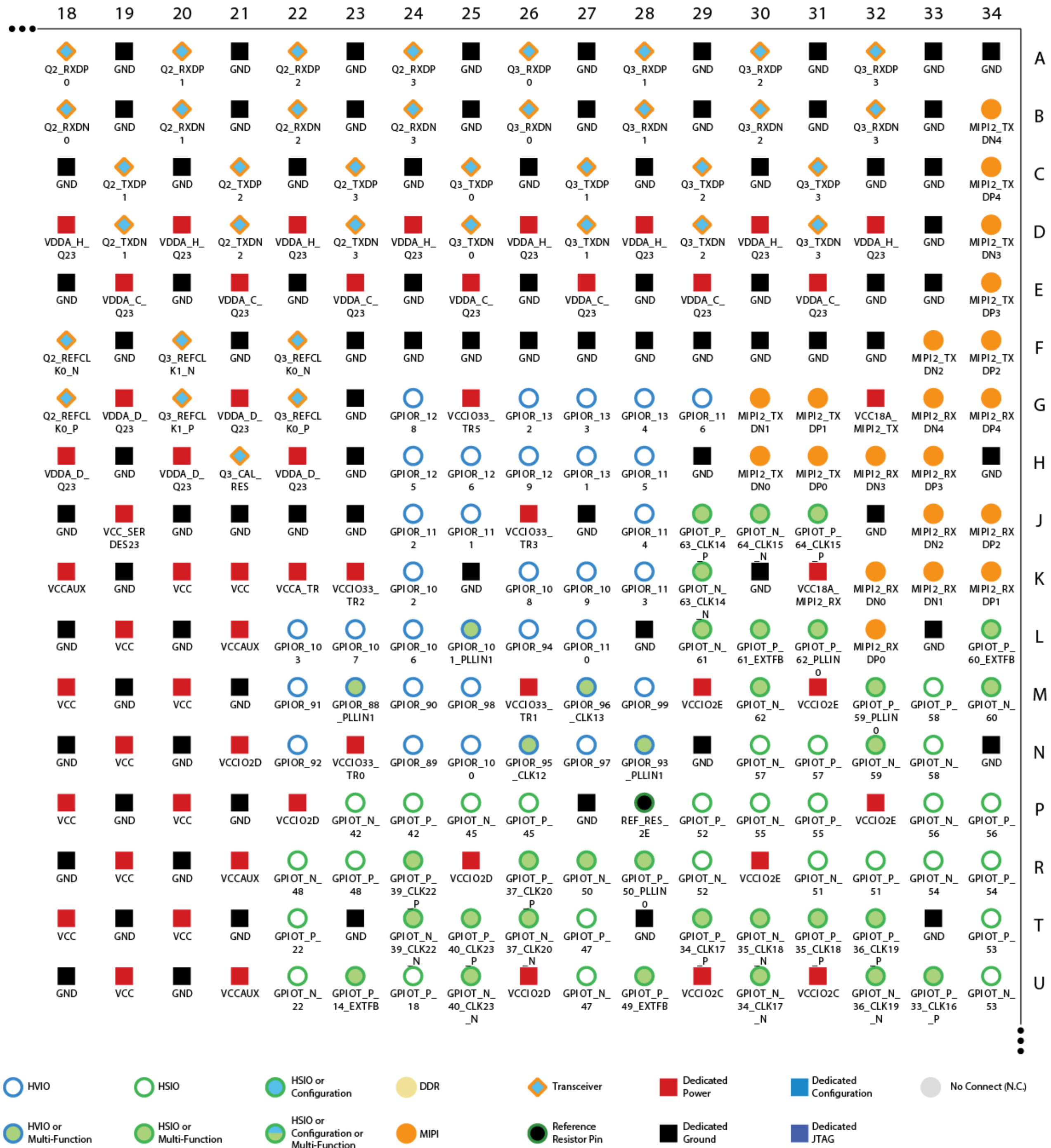


Figure 63: 1156-Ball (N) FBGA Pinout Diagram (Part 3)

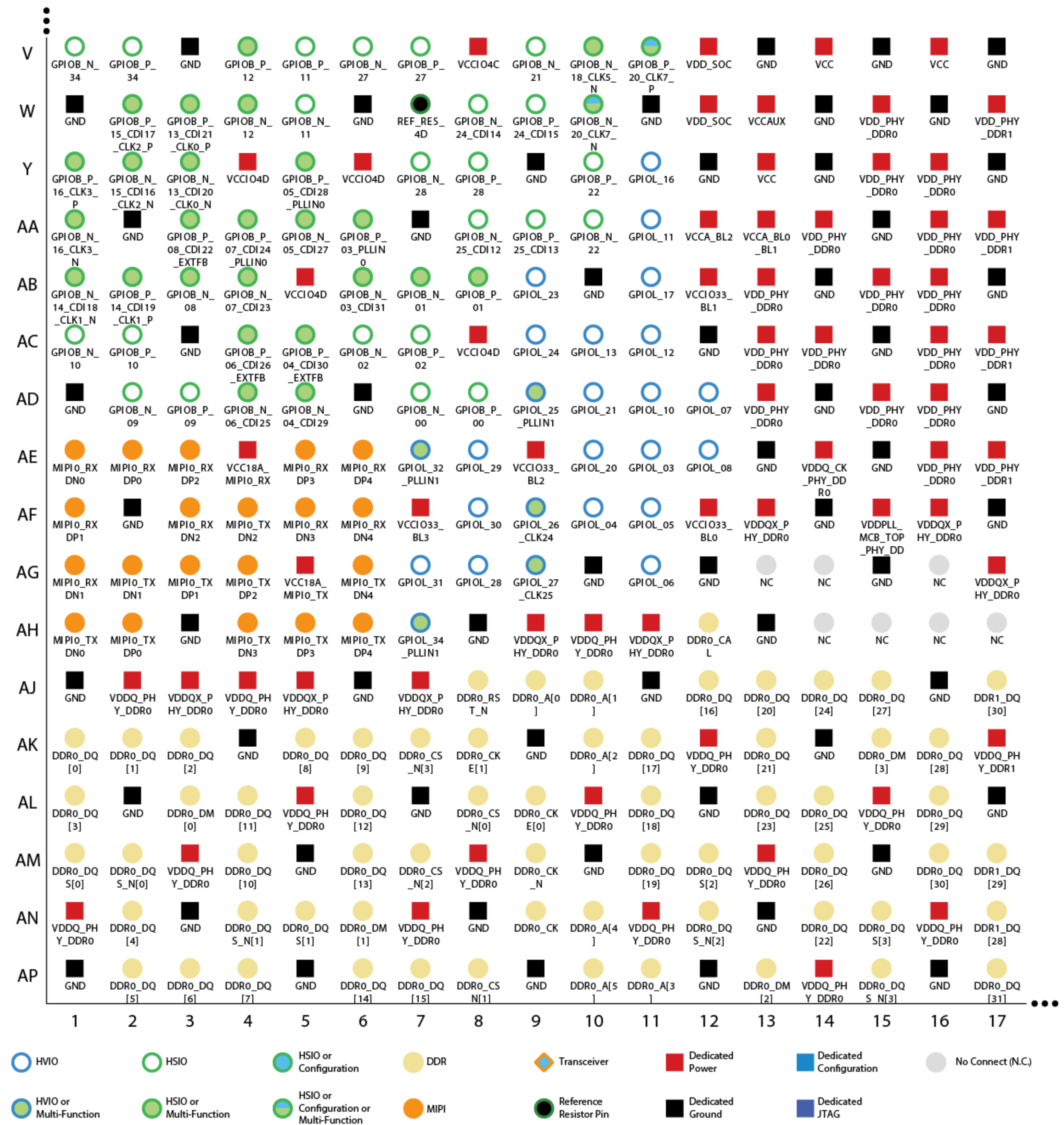


Figure 64: 1156-Ball (N) FBGA Pinout Diagram (Part 4)

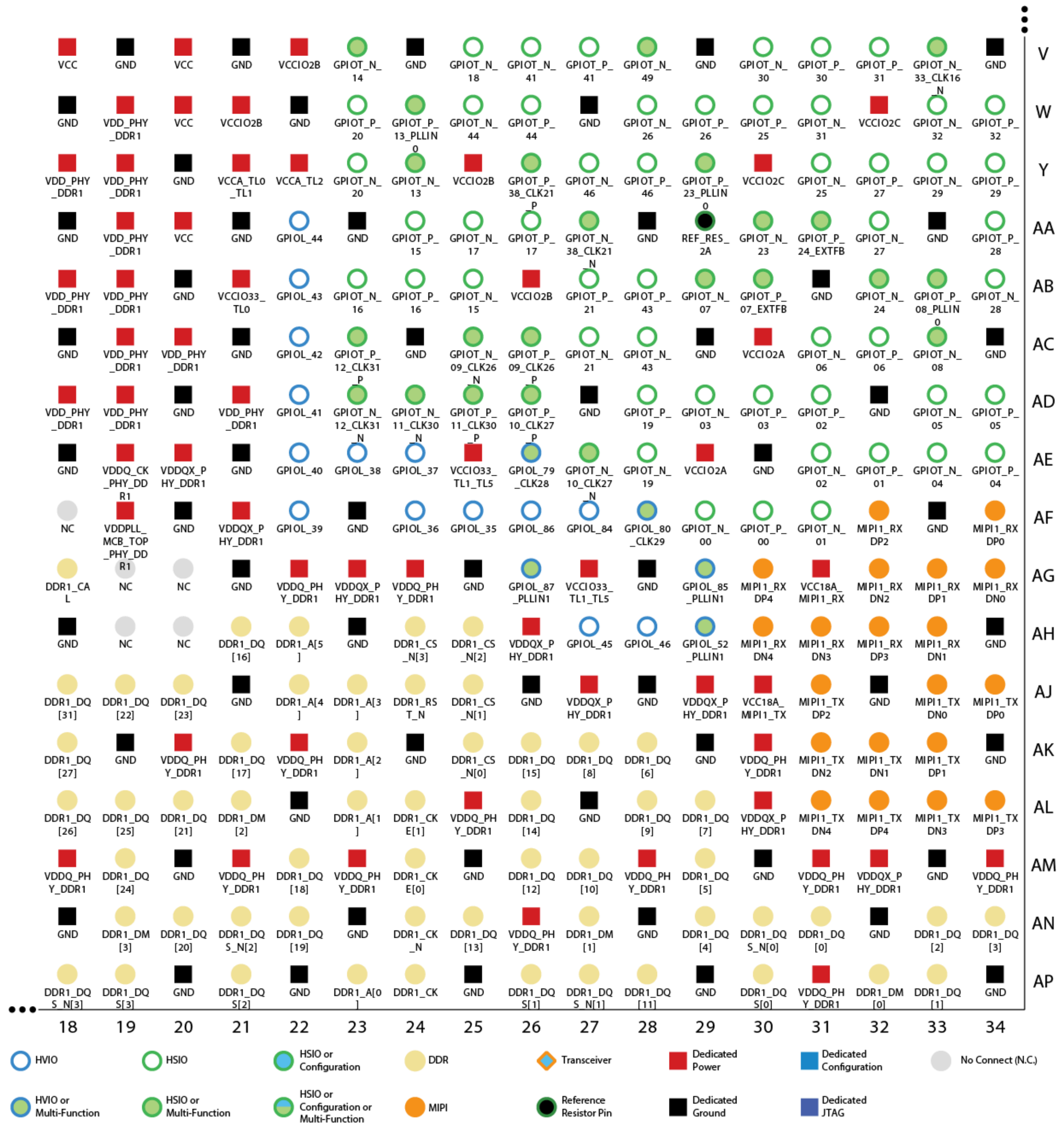


Figure 65: 1156-Ball (N) FBGA I/O Bank Diagram (Part 1)

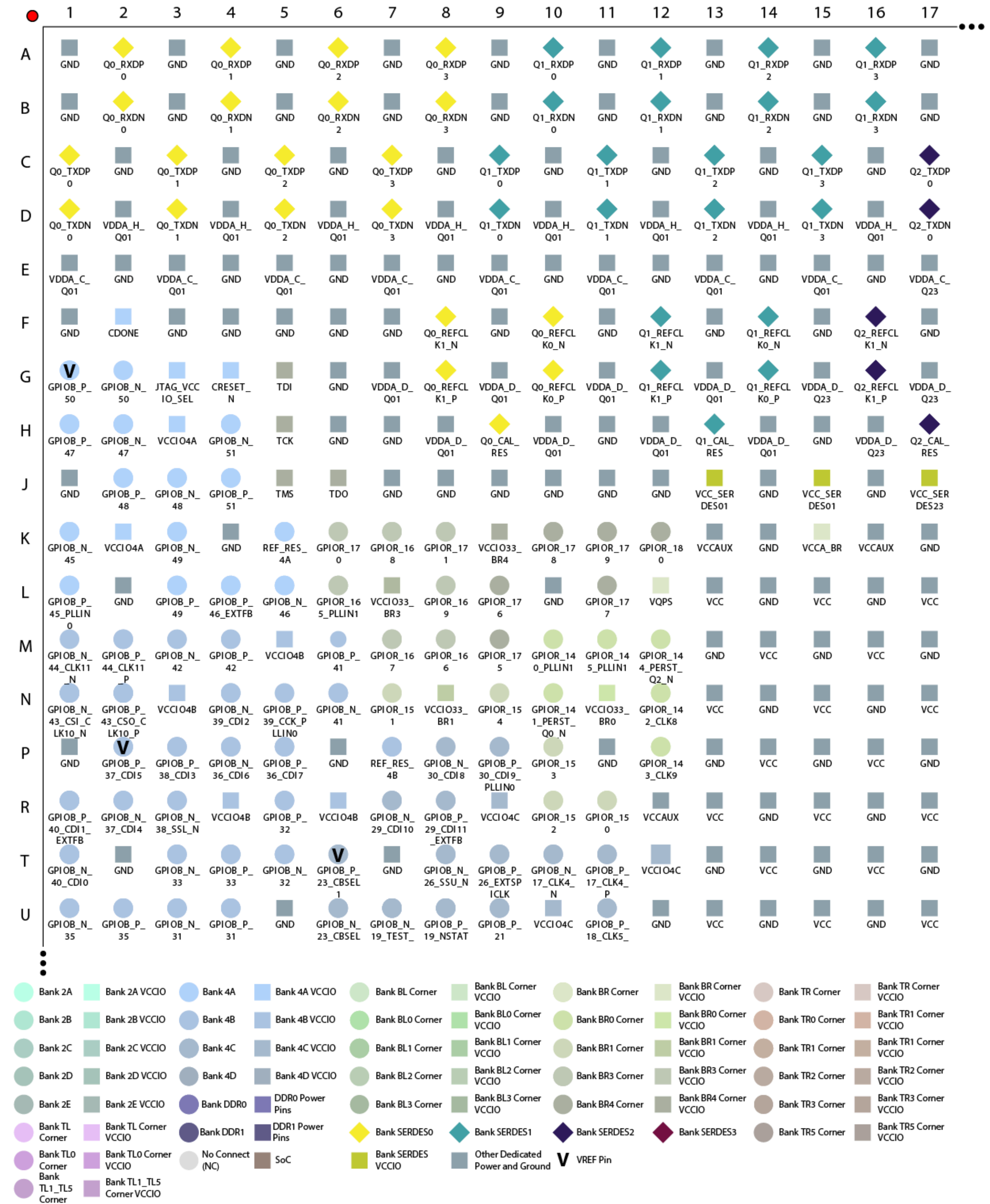


Figure 66: 1156-Ball (N) FBGA I/O Bank Diagram (Part 2)

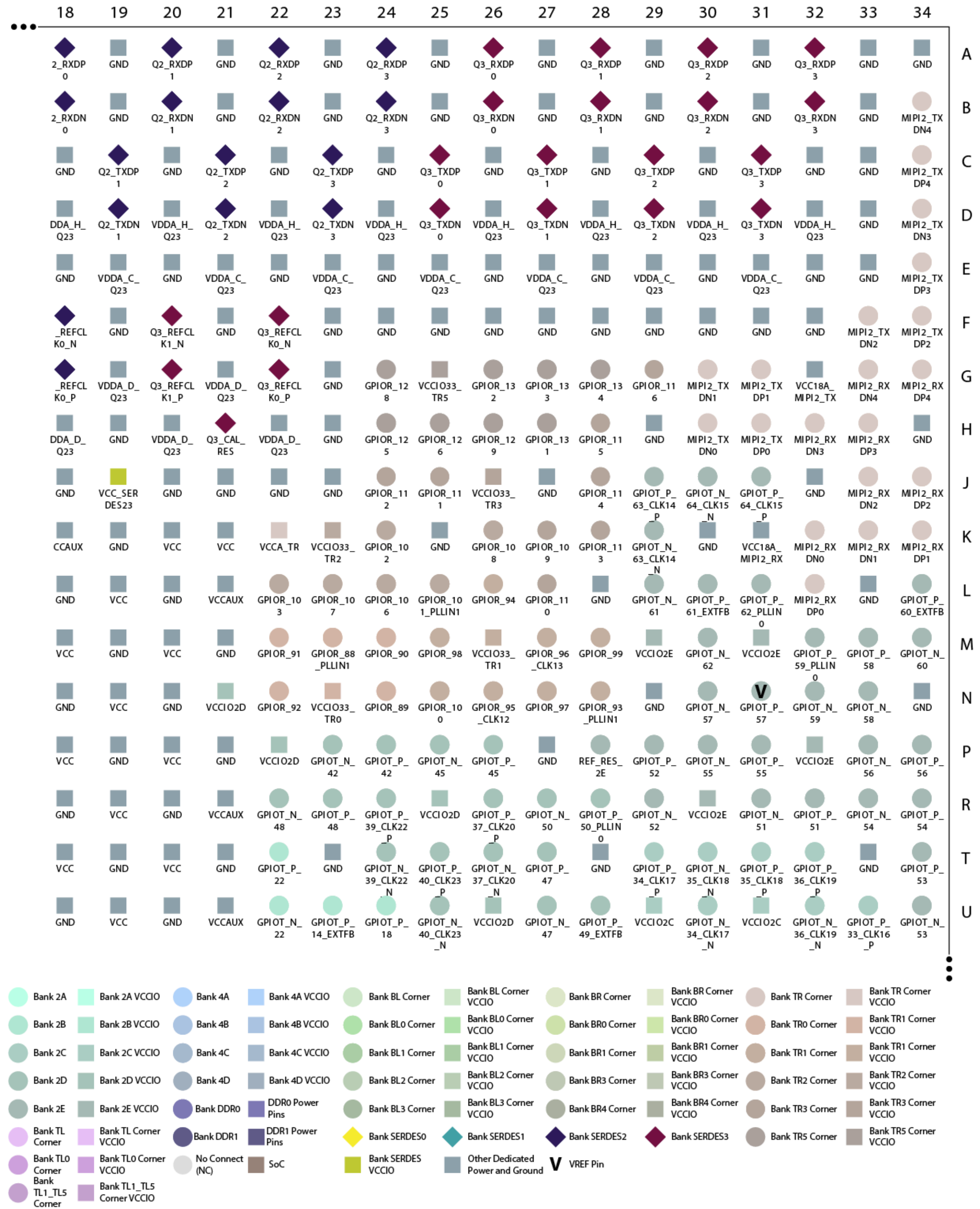


Figure 67: 1156-Ball (N) FBGA I/O Bank Diagram (Part 3)

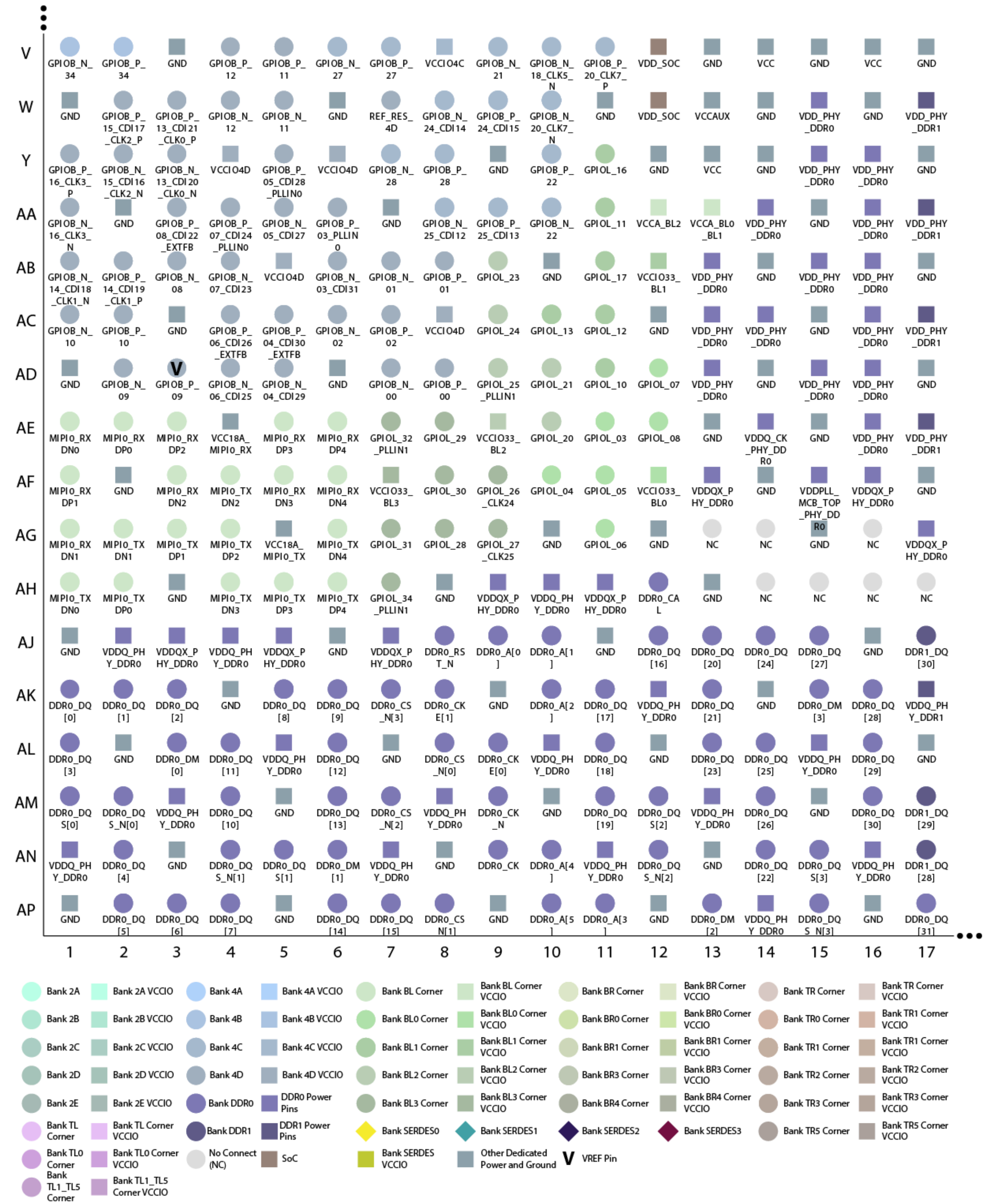


Figure 68: 1156-Ball (N) FBGA I/O Bank Diagram (Part 4)

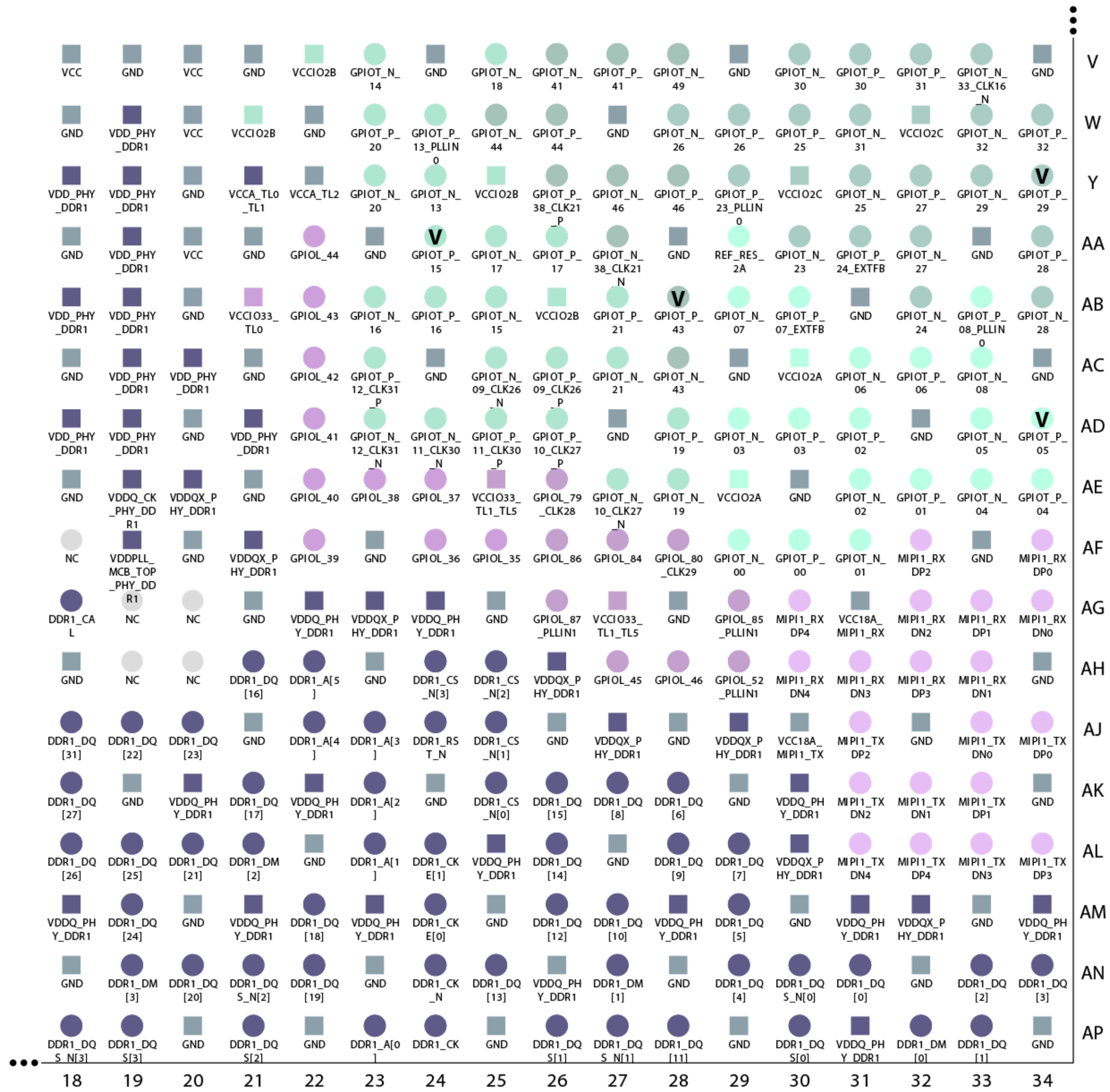


Figure 69: 1156-Ball (N) FBGA Emulated MIPI RX Groups

MIPI RX group I0	MIPI RX group I3	MIPI RX group I6	MIPI RX group I10	MIPI RX group I13	MIPI RX group I16
MIPI RX group I1	MIPI RX group I4	MI PI RX group I7	MIPI RX group I11	MIPI RX group I14	MIPI RX group I17
MIPI RX group I2	MIPI RX group I5	MIPI RX group I8	MIPI RX group I12	MIPI RX group I15	Not part of RX MIPI group

C Clock

Figure 70: 1156-Ball (N) FPGA Package Marking

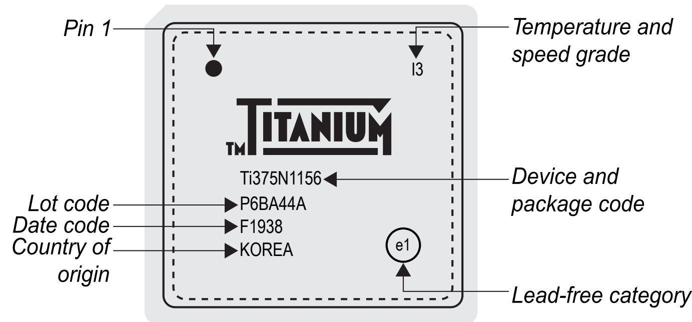
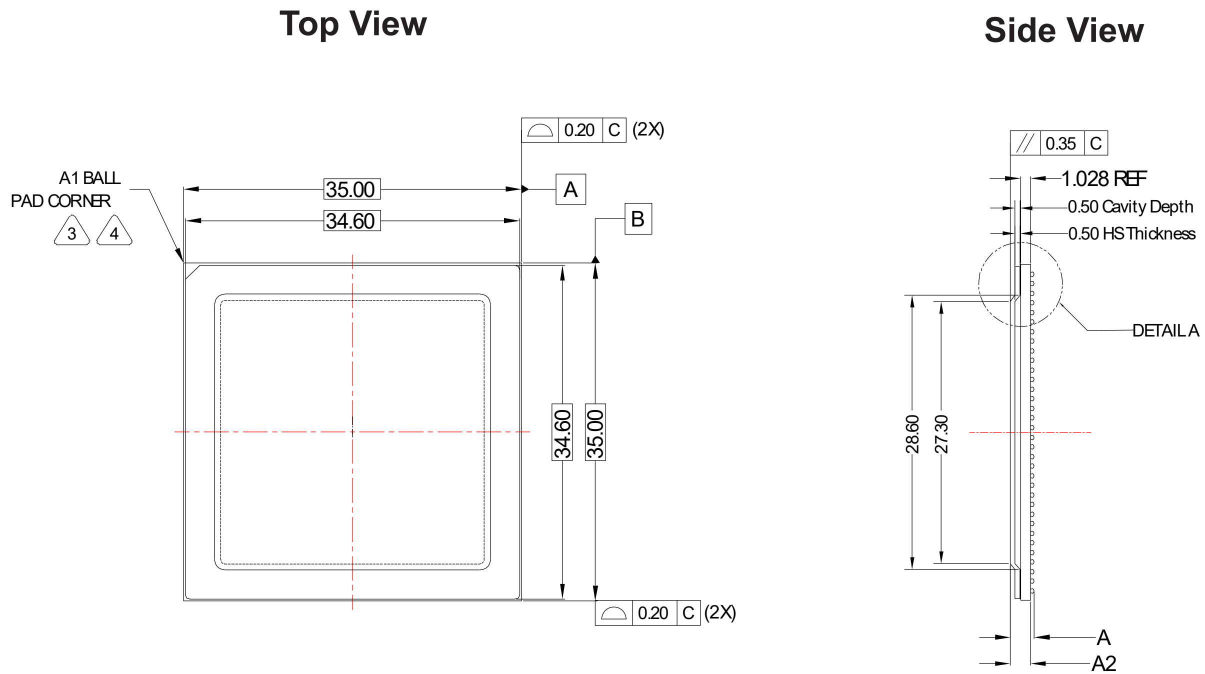


Figure 71: 1156-Ball (N) FBGA Package Outline (Part 1)



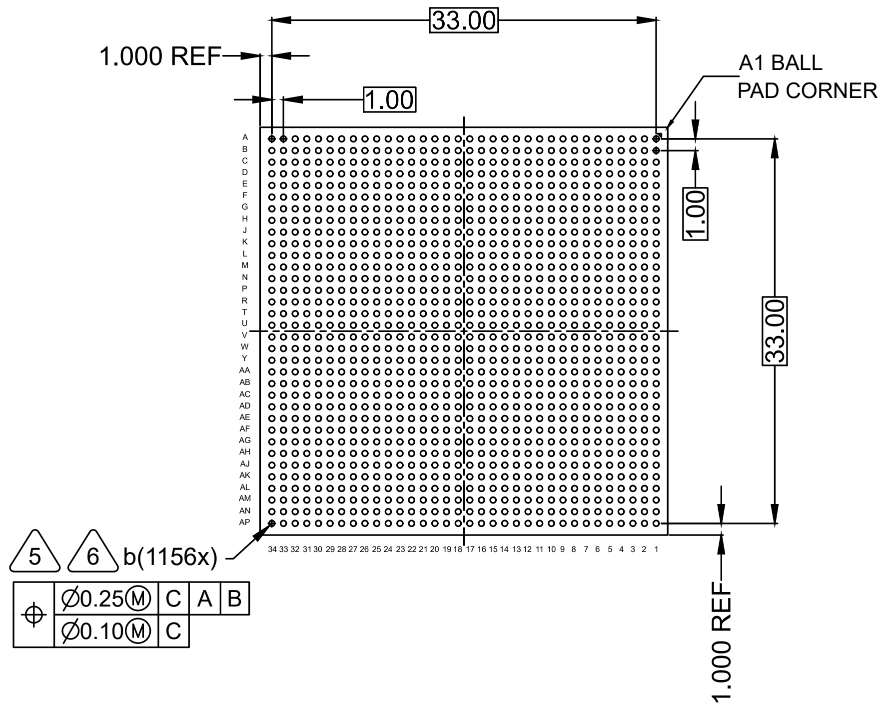
NOTES:

1. All DIMENSIONS AND TOLERANCE CONFORM TO ASME Y14.5M-2018.
2. TERMINAL POSITIONS DESIGNATION PER JESD 95.
3. CORNER DETAILS PER JCET OPTION.
4. PIN 1 IDENTIFIER CAN BE CHAMFER, INK MARK, LASERED MARK, METALLIZED MARK.
5. BALL DIAMETER AFTER REFLOW.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM C.
7. USING ⌀0.500MM RAW SOLDER BALL SIZE DURING ASSEMBLY.

DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A	2.311	2.488	2.665
A1	0.280	0.380	0.480
A2	1.962	2.108	2.254
b	0.400	0.500	0.600
NUMBER OF BALL 1156			

Figure 72: 1156-Ball (N) FBGA Package Outline (Part 2)

Bottom View



NOTES:

1. All DIMENSIONS AND TOLERANCE CONFORM TO ASME Y14.5M-2018.
2. TERMINAL POSITIONS DESIGNATION PER JESD 95.
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5. BALL DIAMETER AFTER REFLOW.
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b	0.400	0.500	0.600
NUMBER OF BALL 1156			

Solder Reflow Guidelines for Surface-Mount Devices

This section provides general guidelines for solder reflow process for Efinix® surface-mount FPGAs. The data used in this document is based on IPC/JEDEC (Association Connecting Electronics Industries/JEDEC Solid State Technology Association) standards. Each printed circuit board (PCB) has its profile, which depends upon the board design and the reflow equipment used. You must characterize each PCB to find a reliable profile.

Reflow

During solder reflow, follow these guidelines:
- Use caution when profiling to ensure that the maximum temperature difference between components is less than 10 °C.
- For best results, perform forced convection reflow with nitrogen.

Inspection

Follow these inspection guidelines:
- **Pre-reflow**—Use visual inspection to verify solder paste dispense location and quantity.
- **Pick and place**—Use machine vision as necessary to ensure proper component placement.
- **Post reflow**—Use electrical testing to verify solder joint formation.

BGA Reballing

Efinix does not recommend BGA reballing. Reballed BGA packages will void the original Efinix® specifications.

Peak Reflow Temperatures

Table 11: Peak Reflow Temperature (T_p) by Package

Package	Moisture Sensitivity Level	Peak Reflow Temperature (+0/-5 °C)
WLCSP	1	260
FBGA	3	260

Note: These packages are "green" and RoHS compliant.

Reflow Profile for SMT Packages

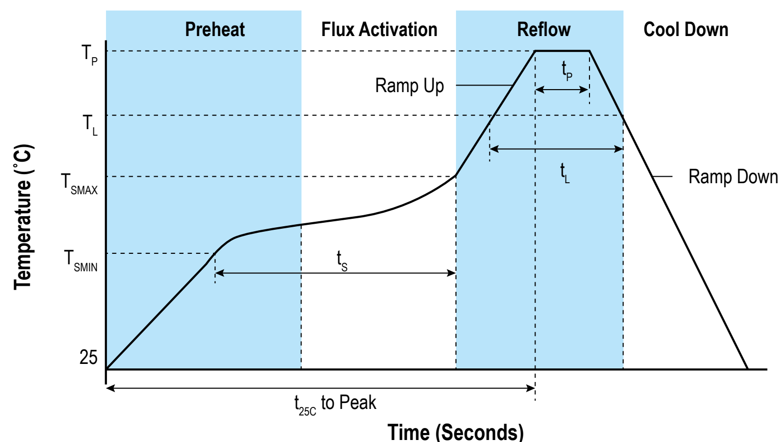
The reflow process usually includes four phases:

1. **Preheat Phase**—The preheat phase brings the assembly from 25 °C to T_S. During this phase, the solvent evaporates from the solder paste. The preheat temperature ramp rate should be less than 2 °C/second to avoid solder balling defects such as solder ball spattering and bridging.
   - **Solder Ball Spattering**—Spattering, the most common solder balling defect, is caused by solvents evaporating explosively. To eliminate spattering, use a slower temperature rise in the preheat phase.
   - **Bridging**—Bridging is usually caused by inaccurate or splashy screen printing, and can often occur with fine pitch components. It can also be caused by solder paste slumping during a rapid temperature rise in the preheat phase.
2. **Flux Activation Phase**—As the temperature rises slowly, it reaches a point at which the flux completely wets the surfaces to be soldered.
3. **Reflow Phase**—The temperature rises to a level sufficient to reflow the solder. The flux wicks surface oxides and contaminants away from the melted solder, resulting in a clean solder joint.
4. **Cool Down Phase**—Ramp down the temperature as fast as possible to control grain size; however, do not exceed 6 °C/second.

Table 12: Peak Reflow Temperature (T_P) Parameters

Parameter	Description	Specification (Lead and Halogen Free Packages)
Ramp up	Average ramp-up rate (T_{SMAX} to T_P)	3 °C/second maximum
T_{SMIN}	Preheat peak minimum temperature	150 °C
T_{SMAX}	Preheat peak maximum temperature	200 °C
t_s	Time between T_{SMIN} and T_{SMAX}	60 - 120 seconds
T_L	Solder melting point	217 °C
t_L	Time maintained above T_L	60 - 150 seconds
t_P	Time within 5 °C of peak temperature	30 seconds
Ramp down	Ramp-down rate	6 °C/second maximum
t_{25C} to T_p	Time from 25 °C to peak temperature	8 minutes maximum

Figure 73: Thermal Reflow Profile



Thermal Resistance

Thermal management is an important consideration when designing your system. Efinix® device data sheets describe the maximum allowable junction temperature so you can assess your system's thermal characteristics. To ensure that the device and package do not exceed the junction temperature requirements, you should always complete a thermal analysis of your specific design.

The data shown in this section is relative and actual values depend on a variety of factors, such as die size, paddle size, airflow, power applied, printed circuit board design, the proximity of other devices, and user applications. Because of this, Efinix FPGAs do not come with preset thermal solutions.

Table 13: Device/Package Thermal Resistance

Measurements taken at 25 °C ambient temperature.

Package	Pitch	Dimensions (mm)	Θ_{JA} (°C/W) Still Air	Θ_{JA} (°C/W) 1 m/s	Θ_{JA} (°C/W) 2 m/s	Θ_{JB} (°C/W)	Θ_{JC} (°C/W)
W64	0.4	3.5 x 3.4	37.24	33.56	32.42	11.95	0.14
F100	0.5	5.5 x 5.5	44.00	39.94	38.57	23.95	18.40
F100S3F2	0.5	5.5 x 5.5	45.62	41.53	40.14	26.13	20.35
F225	0.65	10 x 10	36.89	33.15	32.03	22.32	11.03
F256	0.8	13 x 13	33.89	30.2	29.12	19.19	13.9
J361	0.65	13 x 13	17.50	14.76	13.85	6.07	2.04
G400	0.8	16 x 16	15.42	13.06	12.16	5.34	1.53
J484, L484, M484,	0.8	18 x 18	16.25	13.56	12.70	6.53	3.89
N484	0.8	18 x 18	11.61	9.23	8.28	2.15	0.21
G529	0.8	19 x 19	12.58	10.14	9.20	3.31	1.12
C529	0.8	19 x 19	11.46	8.99	8.06	2.31	0.14
N1156	1.0	35 x 35	8.47	6.26	5.50	1.56	0.28

Where:

- Θ_{JA} is the junction-to-ambient thermal resistance
- Θ_{JB} is the junction-to-board thermal resistance
- Θ_{JC} is the junction-to-case thermal resistance

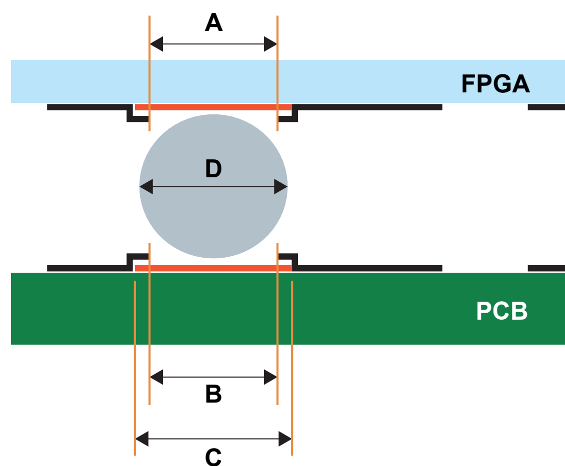
PCB Guidelines for BGA Packages

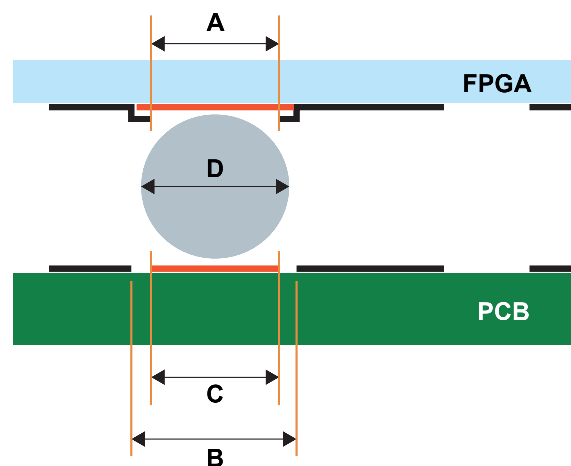
PCB Solder Pad Guidelines

Efinix provides solder mask defined (SMD) and non-solder mask defined (NSMD) diameter information. Use this data when creating your board landing pads.

Non-solder-mask defined (NSMD) pad designs perform better than solder mask defined pads due to lower stresses in the solder near the top of pad. Additionally, they provide a better “grip” area around the pad edge. For best reliability, the Generic Requirements for Surface Mount Design and Land Pattern Standard (IPC-7351A) recommends a NSMD pad with a diameter that is slightly smaller than the solder ball.

Figure 74: SMD and Non-SMD Pad Specification





Legend:

A: BGA package solder mask opening
B: Optimum PCB solder mask opening
C: Optimum PCB pad size
D: Solder ball diameter

Table 14: PCB Solder Pad Recommendations

Package	Pitch (mm)	A BGA Package Solder Mask Opening (mm)	SMD		Non-SMD		D Solder Ball Diameter (mm)
			B Optimum PCB Solder Mask Opening (mm)	C Optimum PCB Pad Size (mm)	B Optimum PCB Solder Mask Opening (mm)	C Optimum PCB Pad Size (mm)	
W64	0.4	N/A	0.2	0.25	0.3	0.2	0.2
F100, F100S3F2	0.5	0.25	0.25	0.3	0.35	0.2	0.25
F225	0.65	0.3	0.3	0.35	0.45	0.3	0.35
F256	0.8	0.4	0.4	0.5	0.6	0.4	0.5
J361	0.65	0.3	0.3	0.35	0.45	0.3	0.35
G400	0.8	0.35	0.35	0.4	0.5	0.35	0.4
J484, L484, M484, N484	0.8	0.35	0.35	0.4	0.5	0.35	0.4
G529	0.8	0.4	0.4	0.5	0.6	0.4	0.5
C529	0.8	0.45	0.45	0.55	0.6	0.4	0.5
N1156	1.0	0.45	0.45	0.55	0.6	0.4	0.5

Routing between Pads on the Top Layer

You can route signal trace between solder pads on the top layer of the PCB while meeting the clearance requirement.

Figure 75: Routing Traces between Pads on the Top Layer

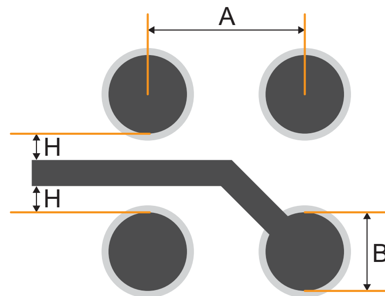


Table 15: Routing Measurements

Measurement	Description	Package									Unit
		W64	F100, F100 S3F2	F225	J361	G400	J484, L484, M484, N484	G529	C529, F256	N1156	
A	Ball pitch.	0.4	0.5	0.65	0.65	0.8	0.8	0.8	0.8	1.0	mm
	Ball ϕ.	0.2	0.25	0.35	0.35	0.4	0.4	0.5	0.5	0.5	mm
B	Width of the solder landing pad ϕ. (SMD)	0.25	0.3	0.35	0.35	0.4	0.4	0.5	0.55	0.55	mm
	Width of the solder landing pad ϕ. (NSMD)	0.2	0.2	0.3	0.3	0.35	0.35	0.4	0.4	0.4	mm
H (min.)	Minimum space between the trace and the landing pad. (SMD)	[3]	0.06	0.08	0.08	0.1	0.1	0.08	0.08	0.1	mm
	Minimum space between the trace and the landing pad. (NSMD)	[3]	0.08	0.08	0.08	0.1	0.1	0.08	0.08	0.1	mm

[3] The via is under the pad, no traces between landing pads.

Guidelines for Vias

You use vias to drop routing down to lower layers. This type of via, called an "offset via," is very robust. The solder mask completely covers the via, which prevents short circuits during paste application, allows for paste overprinting, and prevents etch entrapment.

PCB fabricators use a laser drill for these size vias. Confirm that your fabricator can maintain the tight tolerances required to ensure adequate clearances between vias and pads.

Figure 76: Via Dimensions

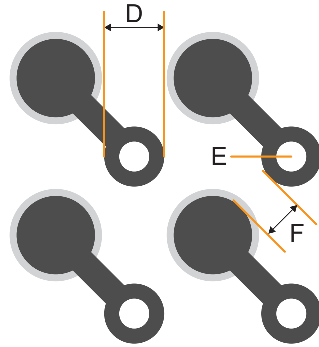


Table 16: Via Measurements

Measurement	Description	Package								Unit
		W64	F100, F100 S3F2	F225	J361	G400	J484, L484, M484, N484	C529, G529, F256	N1156	
D	Via capture pad width.	0.25	0.25	0.3	0.3	0.45	0.45	0.45	0.45	mm
E	Finished via ϕ.	0.127	0.127[4]	0.15	0.15	0.225	0.225	0.225	0.225	mm
F (min.)	Space between the landing pad and via.	[5]	0.072	0.1	0.1	0.1	0.1	0.08	0.1	mm

(4) This is a laser via.
(5) The via is under the pad, no traces between landing pads.

Routing through Different PCB Layers

You can route a trace between two solder pads at the outer two rows of solder pads on the top layer. If you use all of the top-layer routing tracks to route the first and second rows, the inner rows of solder pads must connect to another routing layer with vias for routing outside of the BGA area.

You can use this method to route all of the inner solder pads. Because there is only enough space to route one trace between vias, you need an additional routing layer for every inner row of solder pads after the fourth row.

Figure 77: BGA Trace Routing for Top and Second Layers

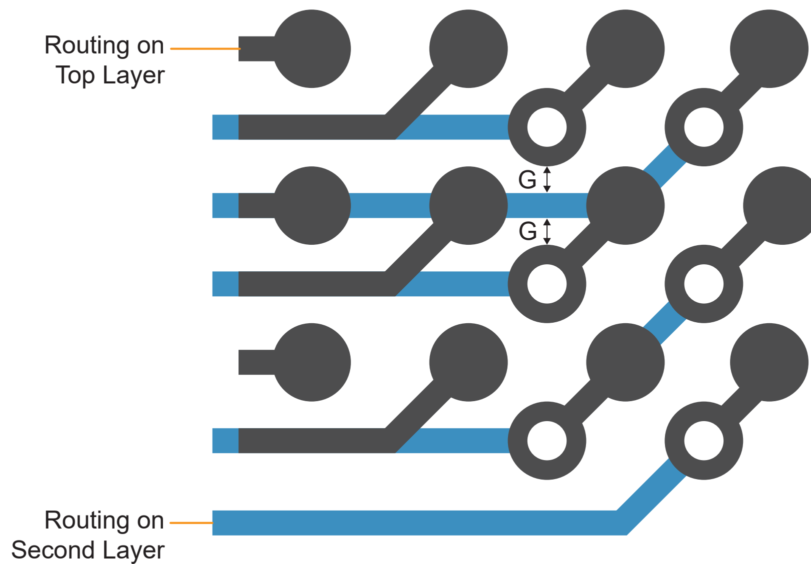


Table 17: Routing Measurements

Measurement	Description	Package								Unit
		W64	F100, F100 S3F2	F225, F256	J361	G400	J484, L484, M484, N484	C529, G529	N1156	
G (min.)	Minimum space required between via and trace.	0.08	0.08	0.08	0.08	0.08	0.08	0.08	0.08	mm

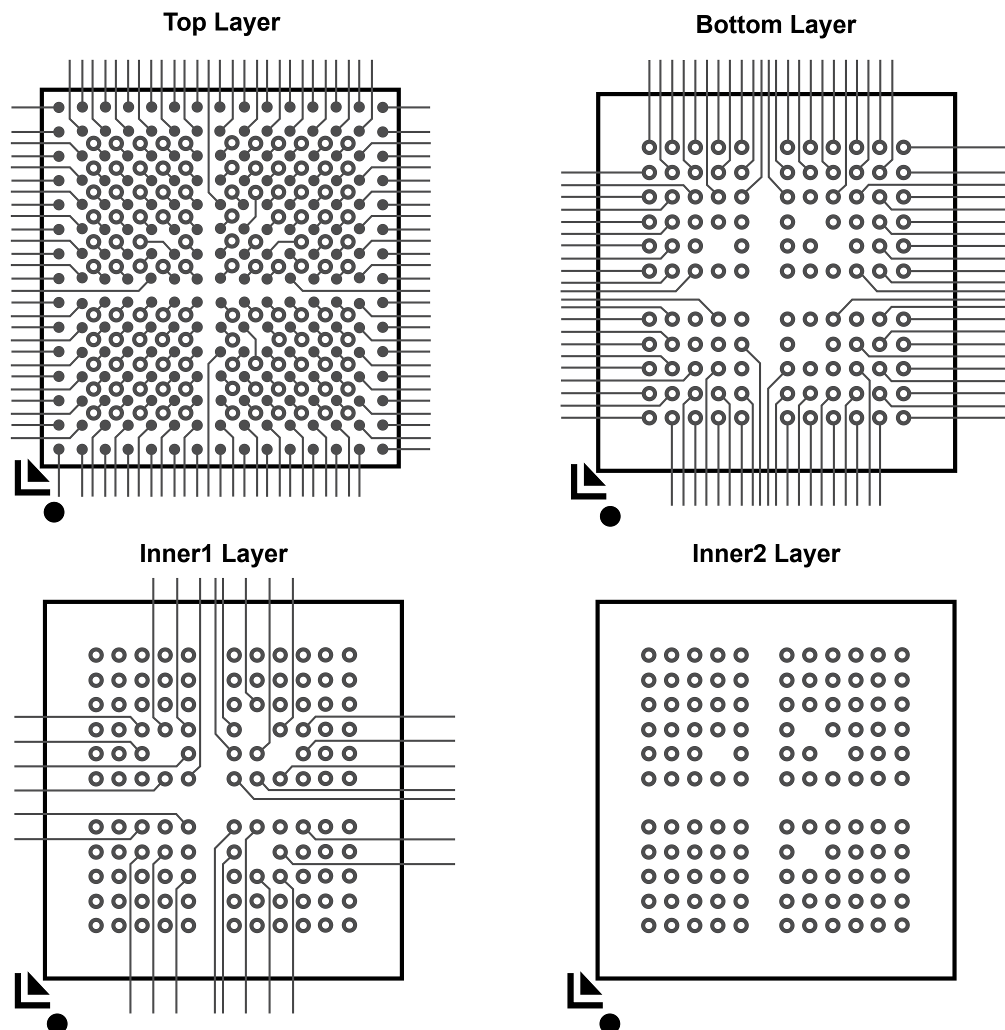
F225 Escape Routing

The following table and figure show how to perform escape routing for the F225 package. These guidelines are one example of acceptable routing using three PCB layers. You can do a different escape routing scheme with a different number of layers. The minimum number of PCB layers is four.

Table 18: Titanium F225 PCB Escape Routing Parameter

Parameter	Specification	Unit
Width of the solder landing pad ϕ	0.35	mm
Width of the solder mask opening ϕ	0.45	mm
Trace width	0.08	mm
Clearance	0.08	mm
Via capture pad width	0.4	mm
Via drill diameter	0.2	mm

Figure 78: 4-Layer Titanium F225 PCB Escape Routing Diagram



Titanium FPGAs Solder Ball

Refer to the table for the recommended type of solder ball used for Titanium FPGAs:

Table 19: Titanium FPGAs Solder Ball

Device	Solder Ball Type
Ti35/Ti60F100S3F2, F100	SAC305
Ti35/Ti60F225	SAC305
Ti35/Ti60F256	SAC305
Ti60W64	SAC405
Ti90/Ti120/Ti180J361	LF35
Ti90/Ti120/Ti180G400	LF35
Ti90/Ti120/Ti180J484, L484, M484	LF35
Ti165/Ti240/Ti375N484	SAC305
Ti90/Ti120/Ti180G529	SAC305
Ti165/Ti240/Ti375C529	SAC305
Ti165/Ti240/Ti375N1156	SAC305

Green Packaging

Efinix FPGAs use packaging solutions that are safer for the environment. These packages are lead (Pb) free and are RoHS compliant. Efinix refers to these products as "green" packaging.

Tape and Reel Packaging

Efinix offers WLCSP devices in tape and reel packaging.

Table 20: Tape and Reel Packaging

Package	Carrier Width (mm)	Cover Width (mm)	Pitch (mm)	Reel Size (in)	Maximum Quantity per Reel
W64	12	9.5	8	13	2,500

Figure 79: Pin 1 Location (W64 Packages)

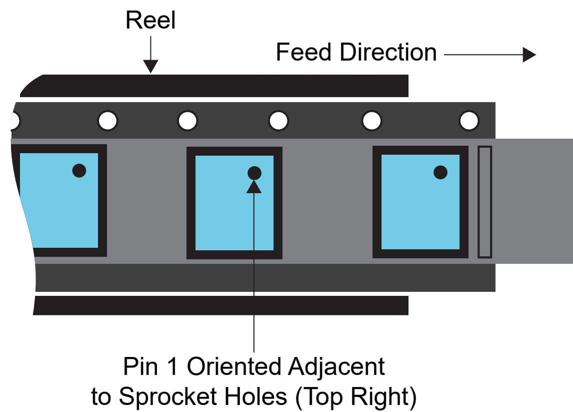
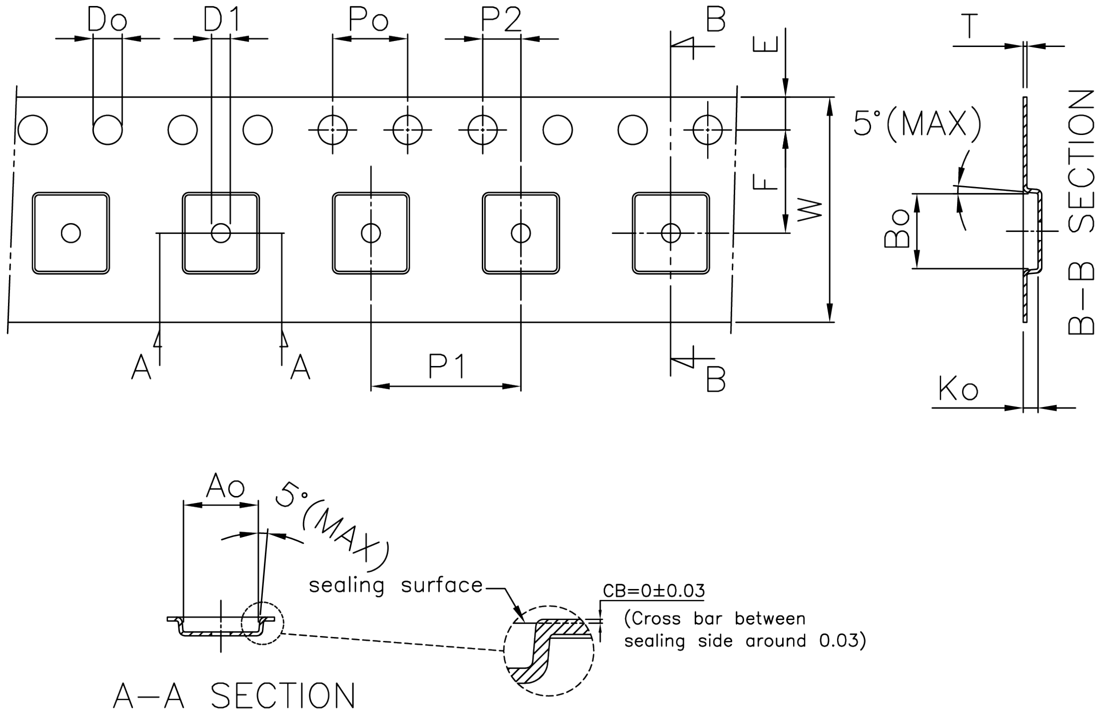


Figure 80: Tape Outline (W64 Packages)



Unit: mm

Symbol	Ao	Bo	Ko	Po	P1	P2	T
Spec	3.59±0.05	3.75±0.05	0.67±0.05	4.00±0.10	8.00±0.10	2.00±0.05	0.25±0.03
Symbol	E	F	Do	D1	W	10Po	
Spec	1.75±0.10	5.50±0.05	$1.50^{+0.10}_{-0}$	1.00±0.05	12.0±0.30	40.0±0.20	

Notice:

1. 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.
2. Carrier camber shall be not more than 1mm per 250mm.
3. Ao & Bo measured on a place in the middle of corner radii.
4. Ko measured from a place on the inside bottom of the pocket to top surface of carrier.
5. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
6. Surface resistivity $\geq 1.0*10^5$ & $\leq 1.0*10^8$ ohm/sq.
7. Tooling type : Male tooling.

Tray Packaging

Efinix offers BGA devices in tray packaging.

Table 21: Tray Packaging

Package	Quantity per Tray	Tray Matrix	Tray Stack	Quantity per Stack
F100, F100S3F2	490	14 x 35	10 + 1	4,900
F225	168	8 x 21	10 + 1	1,680
F256	119	7 x 17	10 + 1	1,190
J361	119	7 x 17	10 + 1	1,190
G400	84	6 x 14	10 + 1	840
J484, L484, M484	84	6 x 14	10 + 1	840
N484	84	6 x 14	5 + 1	840
G529	60	5 x 12	5 + 1	300
C529	84	6 x 14	5 + 1	420
N1156	24	3 x 8	5 + 1	120

Revision History

Table 22: Revision History

Date	Version	Description
October 2024	5.6	Added 484-Ball (N) FBGA Package Specifications on page 52. (DOC-1850) Updated VCCIO33 in pinout for N484, C529, and N1156 packages. (DOC-1960) Corrected clock symbols in M361-Ball FBGA Emulated MIPI RX Groups. (DOC-1997) Updated Table 13: Device/Package Thermal Resistance on page 78 for F100 and F100S3F2 packages. (DOC-2164)
June 2024	5.5	Updated Tray Packaging with F100, F256, and N1156 tray data. Changed 'GND' to 'VQPS_GND' for F100S3F2 - pin A5 and F225 - pin G6 in line with PCN -2405-001. (DOC-1751) Added N1156 package. (DOC-1807) Added F256 package. (DOC-1866) Added 484 package for Ti375 in the Available Package Options.
March 2024	5.4	Removed M361 and F529 packages. (DOC-1769)

Date	Version	Description
February 2024	5.3	Added in new section Titanium FPGAs Solder Ball. (DOC-1709) Added C529 Package. (DOC-1582) Updated pinout descriptions. Updated Titanium Package Options table in Available Package Options section. Updated package marking and outline for F225 and updated package marking for M361, G400, J484, L484, M484, F529, G529, and C529. Updated Tray Packaging for C529 package.
September 2023	5.2	Added package specifications for Ti90, Ti120, and Ti180 G400 package. (DOC-1392) Corrected bank for TDO signal in I/O bank figures for J484, L484, and M484 packages. (DOC-1416) Added in thermal resistance information for G529 and J529 packages. (DOC-1426) Updated the lead-free category for 100-ball and 225-ball FPGA Package Marking. Updated table Peak Reflow Temperature (T_p) by Package.
April 2023	5.1	Update the package specification for Ti60 F225 package due to change of thickness. (DOC-1211)
February 2023	5.0	Added J361, J484 and G529 packages. (DOC-1137) Updated REF_RES_3A pin connection requirement in the Pinout Description topic.
December 2022	4.1	Updated pinout and I/O bank figures for M484 and F529 packages. (DOC-1045) Updated configuration pins external weak pull-up requirements. (DOC-1035)
September 2022	4.0	Added F529 package. Updated PCB guidelines. Updated tray packaging.
July 2022	3.0	Added M361 package. Added L484 package. F484 package renamed as M484.
February 2022	2.0	Added F484 package. Updated available package options table.
December 2021	1.2	Updated PCB Solder Pad Recommendations, Routing Measurements, and added PCB Routing Example. (DOC-649) Updated A7 pin name in 64-Ball WLCSP diagrams.
September 2021	1.1	Updated PCB guidelines. (DOC-504) Updated W64 package outline. (DOC-504) Updated available package options.
June 2021	1.0	Initial release.