Titanium PMA Direct User Guide

UG-TiPMAD-v1.0
October 2024
www.efinixinc.com

Contents

Introduction

Titanium transceivers consist of a physical medium attachment (PMA) and a physical coding sublayer (PCS). The PMA connects the FPGA to the lane, generates the required clocks, and converts the data from parallel to serial or serial to parallel. The PCS contains the digital processing interface between the PMA and the FPGA fabric. The PCS supports SGMII, 10GBase-KR, and PCIe® Gen4 as well as PMA Direct. This user guide provides the specifications for the PMA Direct interface.

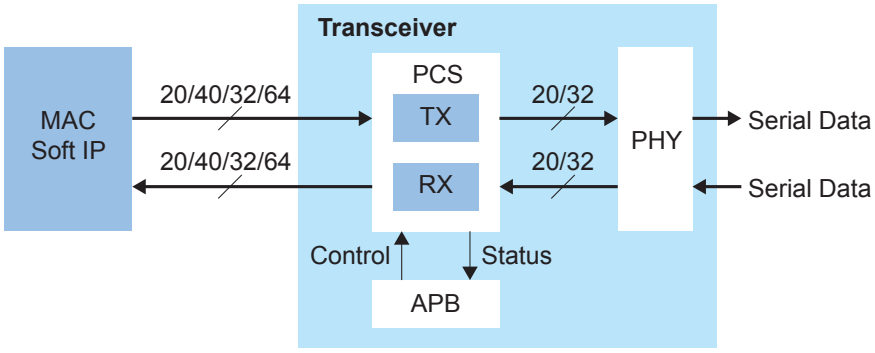
Features

- Per-lane 20-bit and 32-bit PHY interface
- Per-lane 20-, 40-, 32-, and 64-bit core interface
- 1.25G – 12.5G serial link speed
- Single lane and x2, x4 bundle mode
- APB control status register interface

Functional Description

The PMA Direct mode uses the Titanium transceiver lane's PMA only. It supports serial data rates up to 12.5 Gbps. In this configuration, the serializer and deserializer interface connect directly to the FPGA fabric. The transceiver supports 20-, 40-, 32-, and 64-bit configurations. This mode gives you the flexibility to implement other transceiver protocols in the FPGA fabric.

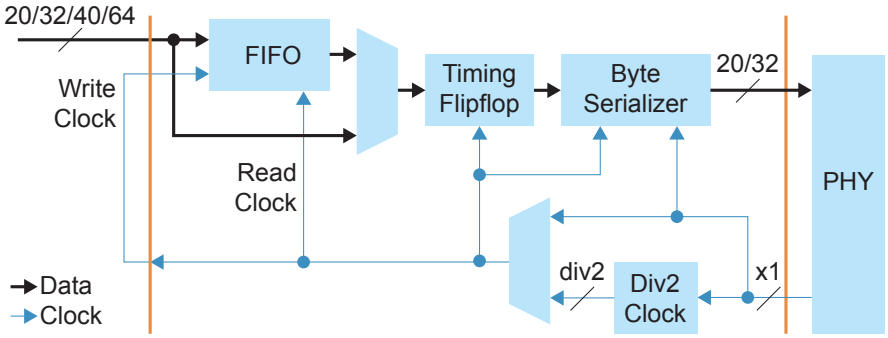
Figure 1: Funtional Block Diagram



Transmitter (TX)

The transmitter comprises a FIFO, timing flipflop, and byte serializer.

Figure 2: TX Block Diagram



The TX FIFO compensates for clock phase differences between the transceiver (read clock) and soft logic (write clock). The PHY provides the clock source to the soft logic, which routes the clock back to the transceiver as its clock source.

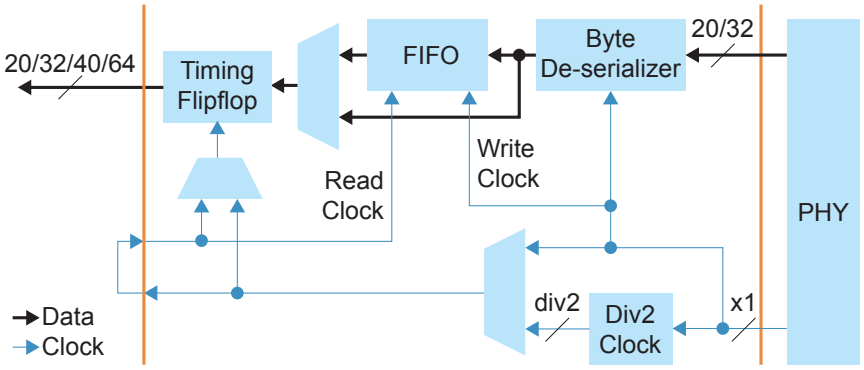
The timing flipflop improves timing closure before the data is propagated to the byte serializer. TX register mode, bypassing the FIFO, is not supported currently.

The byte serializer converts the soft logic data width from 40 bits to 20 bits or 64 bits to 32 bits before feeding the 20/32-bit data to the PHY. If you do not use the byte serializer, the data width from the soft logic must be 20 or 32 bits to match the PHY data width.

Receiver (RX)

The receiver comprises a timing flipflop, FIFO, and byte de-serializer.

Figure 3: RX Block Diagram



The RX FIFO has the same function as the TX FIFO, it compensates for the clock phase differences between the transceiver (read clock) and soft logic (write clock).

The timing flipflop has two paths:

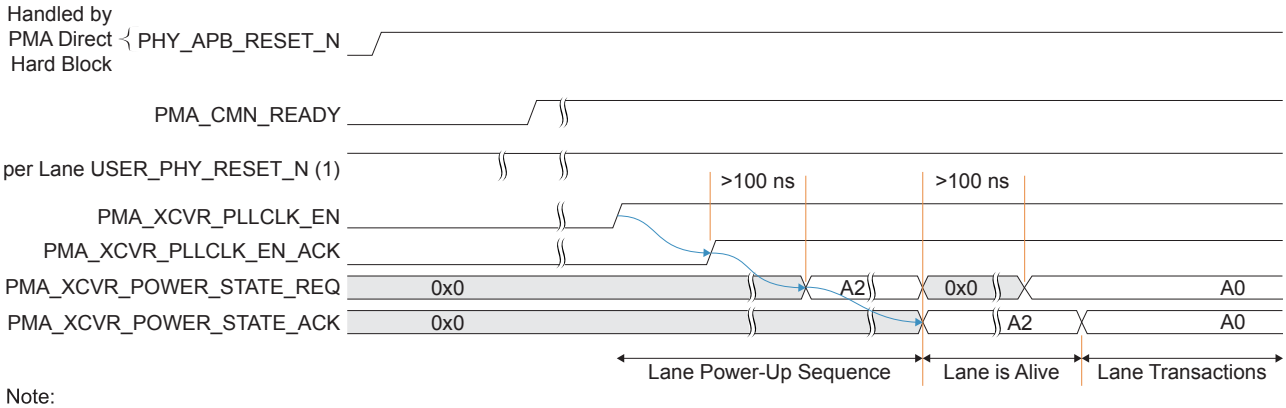
- A FIFO path for better timing at the cost of extra latency.
- A register path that has lower latency at the cost of more difficult timing closure. Refer to **RX Register Mode** on page 9 for design guidelines.

The byte de-serializer converts the PHY data width from 20 or 32 bits to 40 or 64 bits and halves the clock frequency. If you do not use the byte de-serializer, the data width to the soft logic is 20 or 32 bits to match the PHY data width at the same clock frequency as the PHY.

Power-Up Sequence

Initially, the PMA Direct reset controller controls the APB_PRESET_N and PHY_RESET_N signals. The PHY reset signals are handed over to the client after PMA_CMN_READY is asserted and the soft logic enters user mode. The client needs to drive the per lane PHY reset signals high in the initial state so that the power up sequence is not impacted.

Figure 4: Power-Up Sequence



Note:
1. The user application must drive each lane's USER_PHY_RESET_N signal high.

When PMA_CMN_READY is asserted:

- Set PMA_XCVR_POWER_STATE_REQ to 0x0
- Assert PMA_XCVR_PLLCLK_EN

When PMA_XCVR_PLLCLK_EN_ACK is asserted, set PMA_XCVR_POWER_STATE_REQ to A2.

There is a 100 ns (minimum) delay between the assertion of PMA_XCVR_PLLCLK_EN_ACK and when you can set PMA_XCVR_POWER_STATE_REQ to A2.

Valid Recovered Data Capture Window

The client should monitor the assertion of the PHY's `RX_SIGNAL_DETECT` and wait for $t_{rx\_cr\_ceinit}$ or $t_{rx\_cr\_noinit}$ before deciding to use the true recovered data from PHY CDR block.

Figure 5: CDR Recovered Data Window

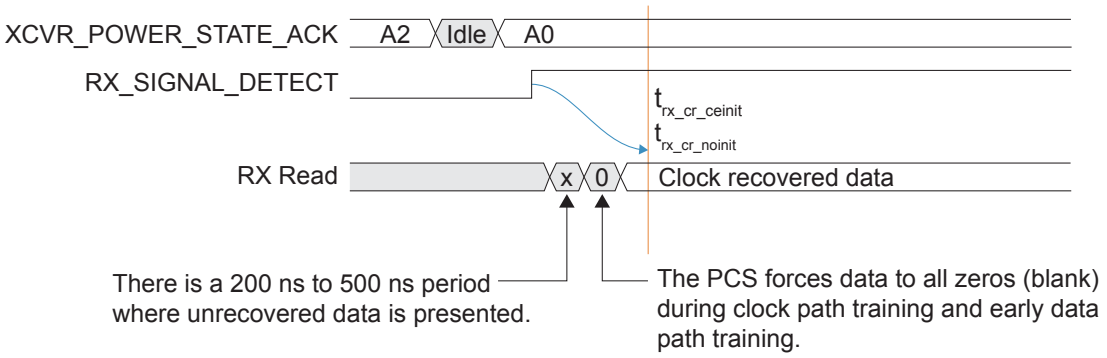


Table 1: Recovered Data Valid Window Timing Parameters

All values are preliminary.

Timing Parameters	<5G (Open Eye)		≥5G (Closed Eye)		Description
	Minimum	Maximum	Minimum	Maximum	
$t_{rx\_cr\_ceinit}$	2,001.613 µs	3,201.806 µs	22.3 µs	117.4 µs	Initial time required to lock clock recovery once valid data is received.
$t_{rx\_cr\_noinit}$	1.389 µs	1.622 µs	658 ns	838 ns	Time required to lock clock recovery once valid data is received, assuming initial adaptation has been previously completed.

RX Equalization

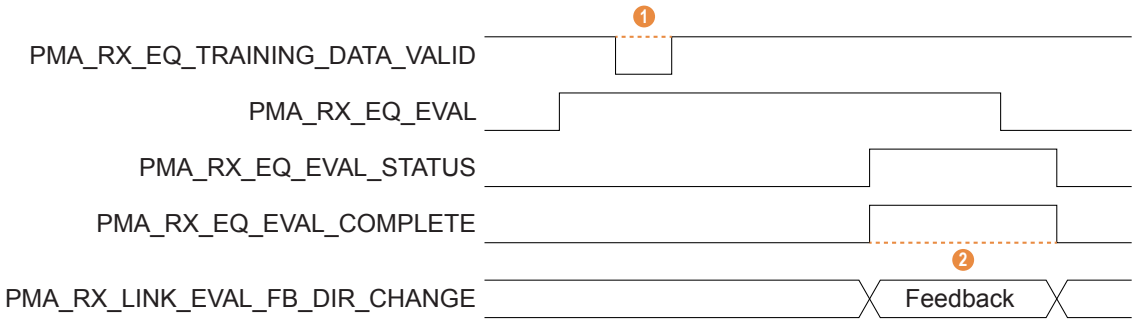
You use the RX equalization evaluation interface to update the far-end transmitter's de-emphasis settings.

The `PMA_RX_EQ_EVAL` input starts the evaluation. When evaluation completes, the `PMA_RX_EQ_EVAL_COMPLETE` and `PMA_RX_LINK_EVAL_FB_DIR_CHANGE` output signals are valid upon assertion of `PMA_RX_EQ_EVAL_STATUS`. The `PMA_RX_LINK_EVAL_FB_DIR_CHANGE` signal provides the evaluation result.

During evaluation, you can de-assert `PMA_RX_EQ_TRAINING_DATA_VALID` if you do not want the incoming RX serial data to be used for the evaluation. For system power up, inialitize `PMA_RX_EQ_TRAINING_DATA_VALID` to `1'b1`.

Do not assert `PMA_RX_EQ_EVAL` while `RX_EQ_EVAL_STATUS` is asserted. After asserting `PMA_RX_EQ_EVAL`, do not de-asserted it until `RX_EQ_EVAL_STATUS` has been asserted.

Figure 6: Evaluate RX Equalization



1. Mask off window. When low, RX serial data is not used for RX equalization evaluation.
2. Signal stays low if evaluation is not completed.

TX De-Emphasis

The PMA Direct interface has a bus, `pma_tx_deemphasis[17:0]`, that provides the pre-emphasis, main cursor, and post-emphasis settings as follows:

- *Bits [17:12]*—C+1 - post-emphasis setting
- *Bits [11:6]*—C0 - main cursor setting
- *Bits [5:0]*—C-1 - pre-emphasis setting

The following boundary conditions must be maintained:

- C0+ | C+1 | + | C-1 | ≤ FS
- C0- | C+1 | - | C-1 | ≥ 0.1875 * FS
- C0 ≥ 0.5625 * FS
- | C+1 | ≤ 0.375 * FS
- | C-1 | ≤ 0.1875 * FS

Note: Refer to "pma_tx_deemphasis" in Table 10: pipe_config/config_reg_11, pipe_config/config_reg_12, pipe_config/config_reg_13, pipe_config/config_reg_14 on page 16 for the pre-emphasis, main cursor, and post-emphasis setting.

The FS values are stored in the PHY_PMA_ISO_TX_FSLF[15:0] PHY register. The user application must read PHY register bit[13:8] to determine the C+1, C0, and C-1 values. The PHY_PMA_ISO_TX_FSLF address is:

- *Lane 0*—24'h:20f008
- *Lane 1*—24'h:20f108
- *Lane 2*—24'h:20f208
- *Lane 3*—24'h:20f308

RX Register Mode

When the RX is configured in register mode, the phase compensation FIFO is bypassed. This bypass introduces clock skew between the transceiver's RXD signal and the core logic clocked by the transceiver recovered clock RAW_SERDES_RX_CLK. To address this clock skew you must insert a bus of negative edge registers on the RXD path to address hold violations.

Bonding Mode

The PMA Direct interface supports a bonding mode in which you use multiple lanes together.

Table 2: TX Bonding Modes

Decription	x1	x2	x4
Supported modes	✓	✓	✓
Bonded lanes	-	L0 - L1 L2 - L3	L0 - L3
Clock source to fabric	-	L1, L3	L1

The PMA Direct interface does not support x8 mode because of the potential for unpredictable data skew.

Note: For TX x2 and x4 modes there is a frequency-dependent data skew between lanes. The user application should implement RX deskew FIFO logic to address this skew.

Table 3: RX Bonding Modes

Description	x1	x2	x4	x8
Supported modes	✓	✓	✓	✓
Bonded lanes	-	L0 - L1 L2 - L3	L0 - L3	Q0 - Q1 Q2 - Q3 Q1 - Q2
Clock source to fabric	-	L1, L3	L1	Q0 L1, Q1 L1, Q2 L1

In RX x8 mode, the TX channel is disabled. The TX is held in reset and all TX ports are tied off.

Read Initial and Preset TX Coefficients

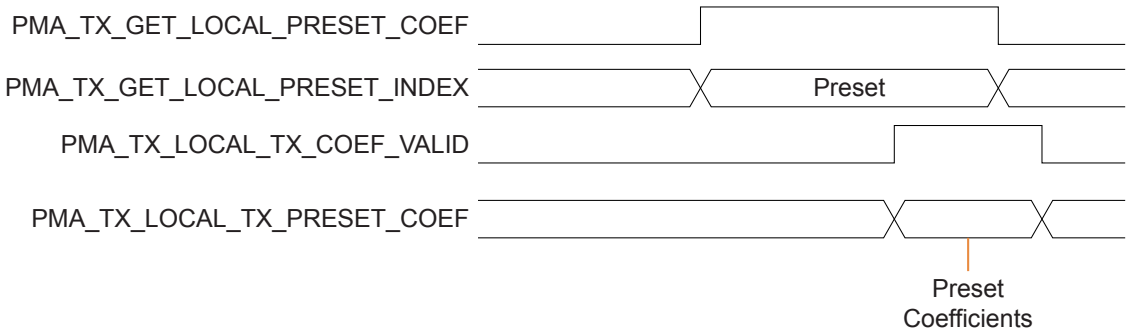
The PMA Direct interface can read the PHY's initial and preset transmitter coefficients through the APB registers. The user application should program the registers to control the start operation, and use the APB registers to read the coefficient values.

Refer to Table 10: pipe_config/config_reg_11, pipe_config/config_reg_12, pipe_config/config_reg_13, pipe_config/config_reg_14 on page 16 for the control bits and Table 11: pipe_config/config_reg_18, pipe_config/config_reg_19, pipe_config/config_reg_20, pipe_config/config_reg_21 on page 17 for the output.

- Do not assert `PMA_TX_GET_LOCAL_INIT_COEF` or `PMA_TX_GET_LOCAL_PRESET_COEF` while `PMA_TX_LOCAL_TX_COEF_VALID` is asserted.
- After asserting `PMA_TX_GET_LOCAL_INIT_COEF` or `PMA_TX_GET_LOCAL_PRESET_COEF`, do not de-assert the signal until PMA_TX_LOCAL_TX_COEF_VALID is asserted.
- During the coefficient read operation, `PMA_TX_LOCAL_PRESET_INDEX` is valid while `PMA_TX_GET_LOCAL_PRESET_COEF` is asserted.

Figure 7: Read Initial TX Coefficients

Figure 8: Read Preset TX Coefficients



Signals

In the Efinity® Interface Designer, these signal names have a user-defined prefix, e.g., <*user prefix*>_<*signal name*>. Efinix recommends that you use the following prefixes for easy quad and lane identification and traceability:

- *Lane signal prefix*—`Qm_Ln` (e.g., `Q0_L1`)
- *Quad signal prefix*—`Qm` (e.g., `Q0`)

Table 4: Signals per Lane

Signal	Direction	Clock Domain	Description
TXD[63:0]	Input	PCS_CLK_TX	Transmit data. [19:0] and [51:32] for 20-bit and 40-bit operation. [31:0] and [63:32] for 32-bit and 64-bit operation. Tie unused data signals to 0.
RXD[63:0]	Output	PCS_CLK_RX	Receive data. [19:0] and [51:32] for 20-bit and 40-bit operation. [31:0] and [63:32] for 32-bit and 64-bit operation. Tie unused data signals to 0.
Clock and Reset			
PCS_CLK_TX	Input	N/A	Interface transmitter clock. Must be the same clock source as RAW_SERDES_TX_CLK. The Efinity software connects this clock for you.
PCS_CLK_RX	Input	N/A	Interface receiver clock. Must be the same clock source as RAW_SERDES_RX_CLK. The Efinity software connects this clock for you.
PCS_RST_N_TX	Input	Asynchronous	PCS TX reset.
PCS_RST_N_RX	Input	Asynchronous	PCS RX reset.
PMA_DIRECT_TX_CLK	Output	N/A	TX clock source from PHY.
PMA_DIRECT_RX_CLK	Output	N/A	Recovered clock from PHY.
USER_PHY_RESET_N	Input	Asynchronous	PHY per lane reset. The user application should initialize to 1.
Control			
PMA_TX_ELEC_IDLE	Input	Asynchronous	PMA TX electrical idle. 1'b1: TX lines placed into electrical idle state. 1'b0: Transmit data.
Power Up			
PMA_XCVR_PLLCLK_EN	Input	Asynchronous	Link PLL clock enable. This signal is used to gate the PMA_PLLCK_DATART and PMA_PLLCLK_FULLRT clocks for the associated link.

Signal	Direction	Clock Domain	Description
PMA_XCVR_PLLCLK_EN_ACK	Output	Asynchronous	Link PLL clock enable acknowledgment. This signal indicates whether the PMA_PLLCLK_DATART and PMA_PLLCLK_FULLRT for the associated link is running or not.
PMA_XCVR_POWER_STATE_ REQ[3:0]	Input	Asynchronous	Link power state request. This signal is used to change the link's power state. When the link has completed the transition to the requested power state, the requested state is reflected on PMA_XCVR_POWER_ STATE_ACK. 4'b0000: Idle. 4'b0001: A0 - TX/RX active. 4'b0010: A1 - Powerdown1 (low power state with minimum exit latency). 4'b0100: A2 - Powerdown2 (lower power state with longer exit latency as compared to A1). 4'b1000: A3 - Powerdown3 (lower power state and longer exit latency as compared to A2). This is a one hot encoded signal. A subsequent change request is not signaled until the current request has been acknowledged and PMA_XCVR_POWER_STATE_REQ has returned to 0. Upon reset release, the first power state must A2.
PMA_XCVR_POWER_STATE_ ACK[3:0]	Output	Asynchronous	Link power state acknowledgment. This signal provides indication that a power state change request has completed. 4'b000000: Value after reset, prior to first power state request 4'b0001: A0 4'b0010: A1 4'b0100: A2 4'b1000: A3 Once a power state is acknowledged, the value remains unchanged until a new power state is requested and the link has completed the transition to the new power state.
PMA_RX_SIGNAL_DETECT	Output	Asynchronous	PMA receiver signal detect. Asserted high upon detection of a high-speed signal on the RX differential inputs.
RX Equalization Evaluation			
PMA_RX_EQ_EVAL	Input	Asynchronous	PMA receiver equalization evaluation enable.
PMA_RX_EQ_TRAINING_ DATA_VALID	Input	Asynchronous	PMA receiver equalization training data valid. The user application should initialize to 1.
PMA_RX_EQ_EVAL_COMPLETE	Output	Asynchronous	PMA receiver equalization complete.
PMA_RX_EQ_EVAL_STATUS	Output	Asynchronous	PMA receiver equalization status.

Table 5: Signals per Quad

Signal	Direction	Clock Domain	Description
USER_APB_CLK	Input	N/A	APB clock source, maximum 200 Mhz.

Signal	Direction	Clock Domain	Description
USER_APB_PADDR[23:0]	Input	APB_CLK	APB address.
USER_APB_PSEL	Input		APB select.
USER_APB_PENABLE	Input		APB enable.
USER_APB_PWRITE	Input		APB write.
USER_APB_PWDATA[31:0]	Input		APB write data.
USER_APB_PRDATA[31:0]	Output		APB read data.
USER_APB_PREADY	Output		APB ready.
PMA_CMN_READY	Output	Asynchronous	PHY ready status signal.

Register Map

The following tables show the PMA Direct registers.

Table 6: Register Map

Register Name	Type	Reset Value	Address[23:0]	Lane/Common
std_pcs/config_reg_0	RW	0x00000000	0xC00500	Lane0
std_pcs/config_reg_1	RW	0x00000000	0xC00504	
std_pcs/config_reg_2	RW	0x00000000	0xC00540	Lane1
std_pcs/config_reg_3	RW	0x00000000	0xC00544	
std_pcs/config_reg_4	RW	0x00000000	0xC00580	Lane2
std_pcs/config_reg_5	RW	0x00000000	0xC00584	
std_pcs/config_reg_6	RW	0x00000000	0xC005C0	Lane3
std_pcs/config_reg_4	RW	0x00000000	0xC005C4	
pipe_config/config_reg_3	RW	0x00000000	0x60000C	Lane0
pipe_config/config_reg_5	RW	0x00000000	0x600014	Lane1
pipe_config/config_reg_7	RW	0x00000000	0x60001C	Lane2
pipe_config/config_reg_9	RW	0x00000000	0x600024	Lane3
pipe_config/config_reg_11	RW	0x00000000	0x60002C	Lane0
pipe_config/config_reg_12	RW	0x00000000	0x600030	Lane1
pipe_config/config_reg_13	RW	0x00000000	0x600034	Lane2
pipe_config/config_reg_14	RW	0x00000000	0x600038	Lane3
pipe_config/config_reg_18	RW	0x00000000	0x600048	Lane0
pipe_config/config_reg_19	RW	0x00000000	0x60004C	Lane1
pipe_config/config_reg_20	RW	0x00000000	0x600050	Lane2
pipe_config/config_reg_21	RW	0x00000000	0x600054	Lane3
pipe_config_cmn/config_reg_22	RW	0x00000000	0x600058	Common

Table 7: std_pcs/config_reg_0, std_pcs/config_reg_2, std_pcs/config_reg_4, std_pcs/config_reg6

Bits	Name	Description	Type	Reset
18	cfg_ser_en	To enable TX byte serializer: 1'b1: TX Core data width is two times the PHY data width 1'b0: TX Core data width is the same as the PHY data width	RW	0
19	cfg_deser_en	To enable RX byte de-serializer: 1'b1: RX Core data width is two times the PHY data width 1'b0: RX Core data width is the same as the PHY data width	RW	0

Table 8: std_pcs/config_reg_1, std_pcs/config_reg_3, std_pcs/config_reg_5, std_pcs/config_reg_7

Bits	Name	Description	Type	Reset
24	cfg_timing_flop_en_rx	Enable RX timing flipflop for better timing closure: 1'b1: Enable 1'b0: Disable	RW	0
13	cfg_bypass_pcfifo_rx	Enable RX phase FIFO: 1'b1: Enable 1'b0: Disable	RW	0
11	cfg_timing_flop_en_tx	Enable RX timing flipflop for better timing closure: 1'b1: Enable 1'b0: Disable	RW	0
0	cfg_bypass_pcfifo_tx	Enable TX phase FIFO: 1'b1: Enable 1'b0: Disable	RW	0

Table 9: pipe_config/config_reg_3, pipe_config/config_reg_5, pipe_config/config_reg_7, pipe_config/config_reg_9

Bits	Name	Description	Type	Reset
25:23	pma_xcvr_data_width	PHY TX and RX parallel data width: 3'b101: 20 bits 3'b010: 32 bits	RW	0

Table 10: pipe_config/config_reg_11, pipe_config/config_reg_12, pipe_config/config_reg_13, pipe_config/config_reg_14

Bits	Name	Description	Type	Reset
29:26	pma_tx_local_preset_index	Transmitter local preset index: Act as the PIPE4 LocalPresetIndex[3:0] signal. This signal must be valid while PMA_TX_GET_LOCAL_PRESET_COEF is asserted because it provides the requested index to report coefficients on PMA_TX_LOCAL_TX_PRESET_COEF[17:0]. Note: Currently only values 0 to 10 are supported.		
25	pma_tx_get_local_preset_coef	Transmitter local preset coefficient request. Act as the PIPE GetLocalPresetCoefficients signal. Once asserted, this signal must remain asserted until the PMA_TX_LOCAL_TX_COEF_VALID signal asserts. The result is presented on PMA_TX_LOCAL_TX_PRESET_COEF[17:0].		
24	pma_tx_get_local_init_coef	Transmitter local initial coefficient request. Once asserted, this signal must remain asserted until PMA_TX_LOCAL_TX_COEF_VALID asserts. The result is presented on PMA_TX_LOCAL_TX_PRESET_COEF[17:0].		
23	rx_polarity	RX data invert polarity. 1'b0 Polarity inversion disabled 1'b1: Polarity inversion enabled		

Bits	Name	Description	Type	Reset
22	pma_rx_termination	Receiver termination. 1'b0: Receiver high impedance. 1'b1: Receiver terminated. Note: Assert pma_rx_termination before PMA_XCVR_PLLCLK_EN_ACK goes high in response to PMA_XCVR_PLLCLK_EN being asserted for initial startup.		
21	pma_tx_low_power_swing_en	Transmitter low power voltage swing enable. Act as the PIPE TXSwing function. The following values are peakto-peak (differential) values: 1'b0: 1000 $V_{p-p(diff)}$ 1'b1: 400 $mV_{p-p(diff)}$	RW	0
20:18	pma_tx_vmargin	Transmitter voltage margin control. Act as the PIPE TXMargin[2:0] function. 3'b000: Maximum driver output swing 3'b110: Minimum driver output swing 3'b111: Reserved		
17:0	pma_tx_deemphasis	Transmitter de-emphasis level control. For the closed eye standard, the bus provides the pre, post, and main cursor settings as follows: [5:0] C-1 [11:6] C0 [17:12] C+1 For the opened eye standard, only bits [1:0] are used: 2'b00: 6 dB de-emphasis 2'b01: 3.5 dB de-emphasis 2'b10: No de-emphasis 2'b11: Reserved	RW	0

Table 11: pipe_config/config_reg_18, pipe_config/config_reg_19, pipe_config/config_reg_20, pipe_config/config_reg_21

Bits	Name	Description	Type	Reset
0	pma_tx_local_tx_coef_valid	Transmitter local coefficient valid. Act as the PIPE LocalTXCoefficientsValid signal. This signal indicates when the coefficients on PMA_TX_LOCAL_PRESET_COEF[17:0] are valid based on either a PMA_TX_GET_LOCAL_PRESET_COEF or a PMA_TX_GET_LOCAL_INIT_COEF request. This signal remains asserted until a request signal is triggered: either PMA_TX_GET_LOCAL_PRESET_COEF or PMA_TX_GET_LOCAL_INIT_COEF deassert. Note: For the result to be valid, the PHY must be in A2, A1, or A0 power states and resistor calibration must have completed as indicated by the assertion of PMA_CMN_READY.	RW	0

Bits	Name	Description	Type	Reset
18:1	pma_tx_local_tx_preset_coef	Transmitter local preset and initialization coefficients. Act as the PIPE LocalTXPresetCoefficients[17:0] signal. Coefficients from a PMA_TX_GET_LOCAL_PRESET_COEF or PMA_TX_GET_LOCAL_INIT_COEF request are presented here and remain valid while PMA_TX_LOCAL_TX_COEF_VALID is asserted. Note: For the result to be valid, the PHY must be in A2, A1, or A0 power states and resistor calibration must have completed as indicated by the assertion of PMA_CMN_READY.	RW	0

Table 12: pipe_config_cmn/config_reg_22

Bits	Name	Description	Type	Reset
7:6	cfg_bonding_mode_tx3	Determines the TX bonding mode for lane 3. 00: x1 01: x2 10: x4	RW	0
5:4	cfg_bonding_mode_tx2	Determines the TX bonding mode for lane 2. 00: x1 01: x2 10: x4	RW	0
3:2	cfg_bonding_mode_tx1	Determines the TX bonding mode for lane 1. 00: x1 01: x2 10: x4	RW	0
1:0	cfg_bonding_mode_tx0	Determines the TX bonding mode for lane 0. 00: x1 01: x2 10: x4	RW	0

Revision History

Table 13: Document Revision History

Date	Version	Description
October 2024	1.0	Initial release.