AN 021: Performing Boundary-Scan Testing on Trion® FPGAs

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Contents

Introduction

The Efinix® Trion® FPGAs support the Joint Test Action Group (JTAG) IEEE Std. 1149.1 Boundary-Scan Testing (BST). BST allows you to test pin connections without physically probing the specific pin, which is beneficial when there is a need to perform a pin connection test quickly and efficiently.

Trion FPGAs include the following required IEEE Std. 1149.1 circuitry components:

- *JTAG pins*—BST interface
- *TAP Controller*—Controls the BST operation based on the Test Access Port (TAP) Controller State Machine
- *Instruction Register*—Registers for reading and decoding BST instructions
- *Data Registers*—Device ID, bypass, and boundary-scan registers

Figure 1: IEEE Std. 1149.1 Circuitry in Trion FPGAs

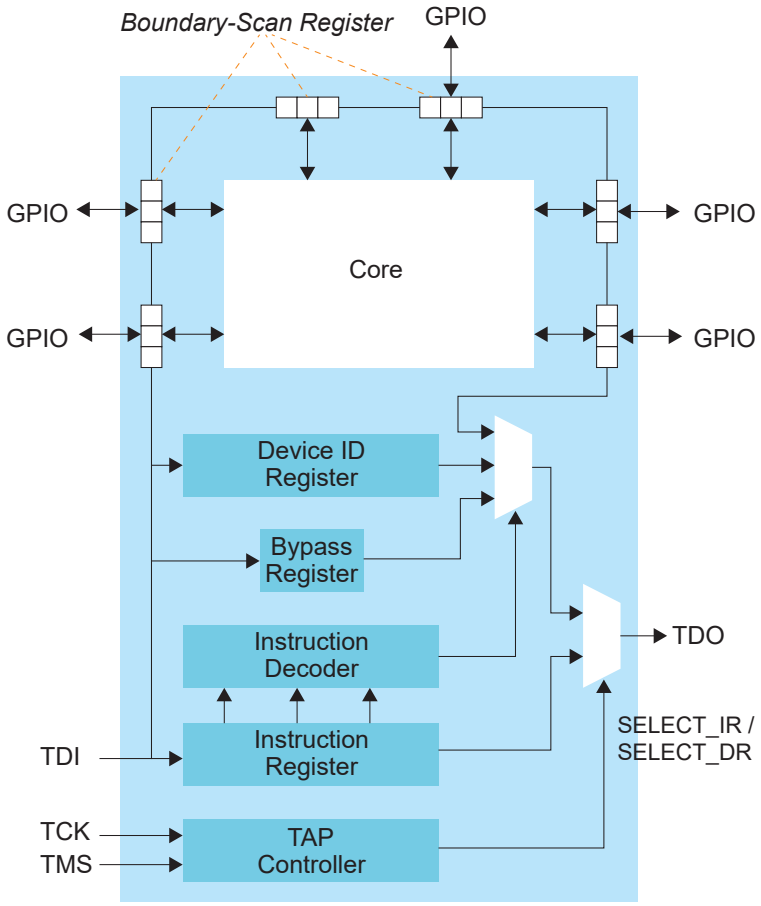


Table 1: Boundary -Scan Testing Support for Trion FPGAs

FPGA	Package	Supported
T4	BGA49	–
	BGA81	✓
T8	BGA49	–
	BGA81, QFP144	✓
T13	All	✓
T20	All	✓
T35	All	✓
T55	All	✓
T85	All	✓
T120	All	✓

JTAG Pins

The following table lists the pins required when performing BST on Trion FPGAs. These pins provide access to the TAP controller.

Table 2: JTAG Pins

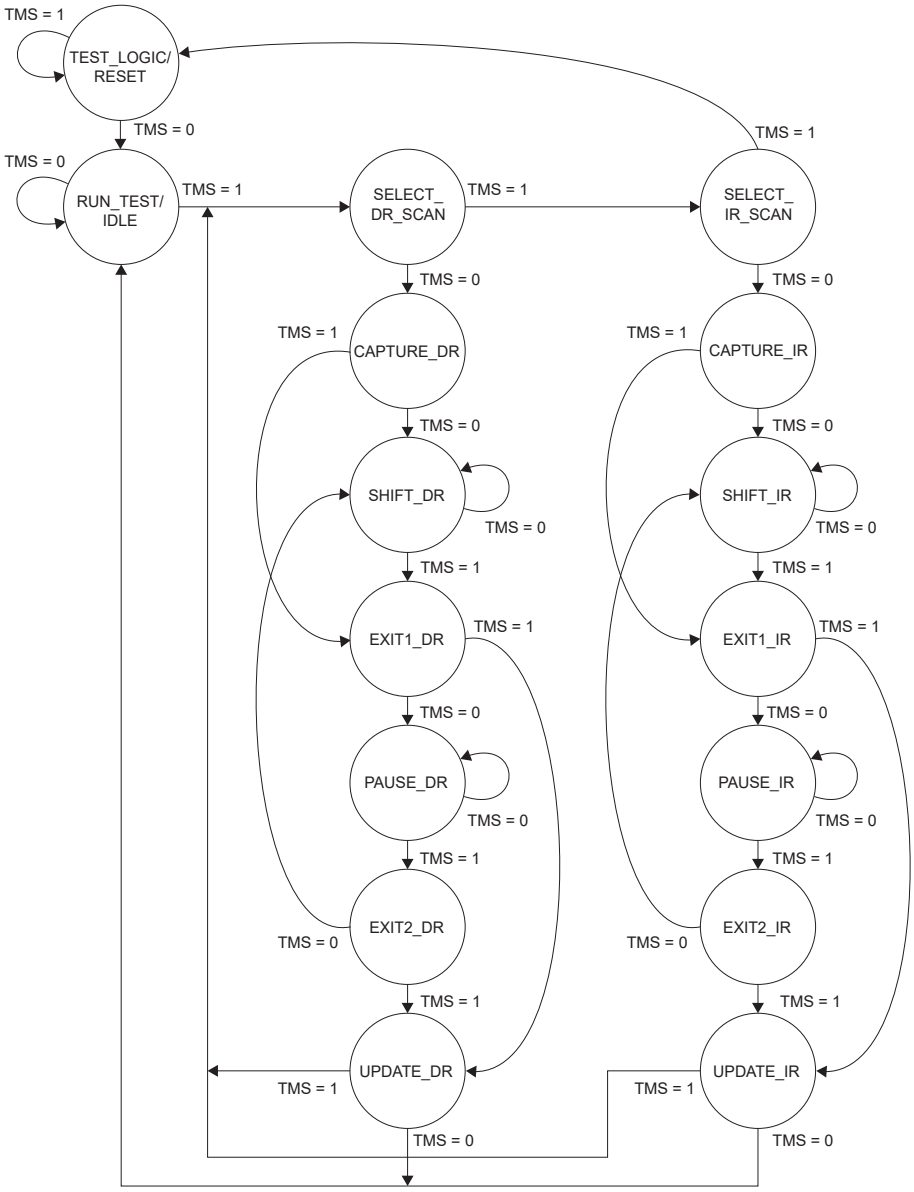
Pin Name	Direction	Description
TCK	Input	JTAG test clock input. The rising edge loads signals applied at the TAP input pins (TMS and TDI). The falling edge clocks out signals through the TAP TDO pin.
TMS	Input	JTAG test mode select. Mode select pin for the TAP controller. The value of TMS on the rising edge of TCK determines the next state in the TAP controller state machine. TMS is typically a weak pull-up; when external source does not drive it, the test logic perceives a logic 1.
TDI	Input	JTAG test data input. Data applied at this serial input goes to the instruction register or a test data register, depending on the state in the TAP controller. Typically, the signal applied at TDI changes states following the TCK's falling edge while the registers shift in the value received on the rising edge. TDI is typically a weak pull-up; when external source does not drive it, the test logic perceives a logic 1.
TDO	Output	JTAG test data output. The serial output from the instruction register or the test data register, depending on the state in the TAP controller. During shifting, data applied at TDI appears at TDO after several cycles of TCK determined by the length of the instruction register or test data register included in the serial path. The signal driven through TDO changes state following the falling edge of TCK. When no data is shifted through the device, TDO is set to an inactive drive state (e.g., high-impedance).

Note: The JTAG pins (`TCK`, `TDI`, `TDO`, `TMS`) are not testable as these pins are not connected to the boundary-scan cells.

TAP Controller

The TAP Controller is controlled by the TMS pin and TCK pin, which controls the BST operation based on the TAP Controller State Machine. The status of the TMS pin on every rising edge of TCK brings the TAP Controller to a specific state.

Figure 2: IEEE Std. 1149.1 TAP Controller State Machine



RESET State

The TAP Controller reaches this state when TMS is held high for five TCK pulses. This state is useful when the test logic needs to be disabled to perform Trion FPGAs' regular operation. The TRST pin is not available in Trion FPGAs. Pulse the TMS high for at least five times to disable the test logic or reset the TAP Controller.

RUN_TEST / IDLE State

TAP Controller state move from RESET state to this state when `TMS` is low. In Trion FPGAs, you cannot use any instruction when the TAP controller is in this state.

SELECT_IR_SCAN to UPDATE_IR States

The instruction register is connected between the `TDI` pin and `TDO` pin to allow opcode instruction to be shifted into the instruction register from the `TDI` pin. Next, the opcode instruction is updated to enable TAP Controller to perform the corresponding actions.

SELECT_DR_SCAN to UPDATE_DR States

The data registers are connected between the `TDI` pin and `TDO` pin based on the opcode instruction updated in the instruction register.

Instruction Register

Trion FPGAs support the following instruction registers.

Table 3: Trion FPGA IEEE Std. 1149.1 Circuitry Instruction Register

Register	Length (bits)	Description
Instruction	4	You can provide opcodes to the instruction register to determine the actions and select the data registers (device ID, bypass, or boundary-scan).

Table 4: Trion FPGA IEEE Std. 1149.1 BST Instructions

Instruction	Opcode [4:0]	Description
IDCODE	0011	Selects the device ID register and returns the device ID of the Trion FPGA through TDO.
BYPASS	1111	Selects the bypass register, thus allowing the TDI pin to be connected to the TDO by a 1-bit register. When the Trion FPGA is connected to a daisy chain on the board to other JTAG devices, you can use this instruction if BST is not required on the Trion FPGA.
EXTEST	0000	Selects the boundary-scan register. EXTEST allows off-chip circuitry testing by allowing the boundary-scan register to drive out the pin and monitor the data coming from the pin.
SAMPLE/PRELOAD	0010	PRELOAD allows the boundary-scan register to be preloaded with known data by shifting in the known data through the TDI pin before the EXTEST instruction is used. SAMPLE allows the boundary-scan register to sample the states of the pin and to be shifted out through TDO for analysis.

JTAG Device IDs

The following table lists the Trion JTAG device IDs.

Table 5: Trion JTAG Device IDs

FPGA	Package	JTAG Device ID
T4, T8	BGA81	0x0
T8	QFP144	0x00210A79
T13	All	0x00210A79
T20	WLCSP80, QFP100F3, QFP144, BGA169, BGA256	0x00210A79
T20	BGA324, BGA400	0x00240A79
T35	All	0x00240A79
T55, T85, T120	All	0x00220A79

Data Registers

The following table lists the available circuitry data registers.

Table 6: Trion FPGA IEEE Std. 1149.1 Circuitry Data Registers

Register	Length (bits)	Description
Device ID	32	Device ID register. Selected when the IDCODE instruction is provided to the instruction register.
Bypass	1	Bypass register. Selected when the BYPASS instruction is provided to the instruction register.
Boundary-scan	*n*	Boundary-scan register. Selected when the EXTEST or SAMPLE/PRELOAD instruction is provided to the instruction register. Refer to the BSDL file of the respective Trion FPGA package to obtain its boundary-scan register length, *n*.

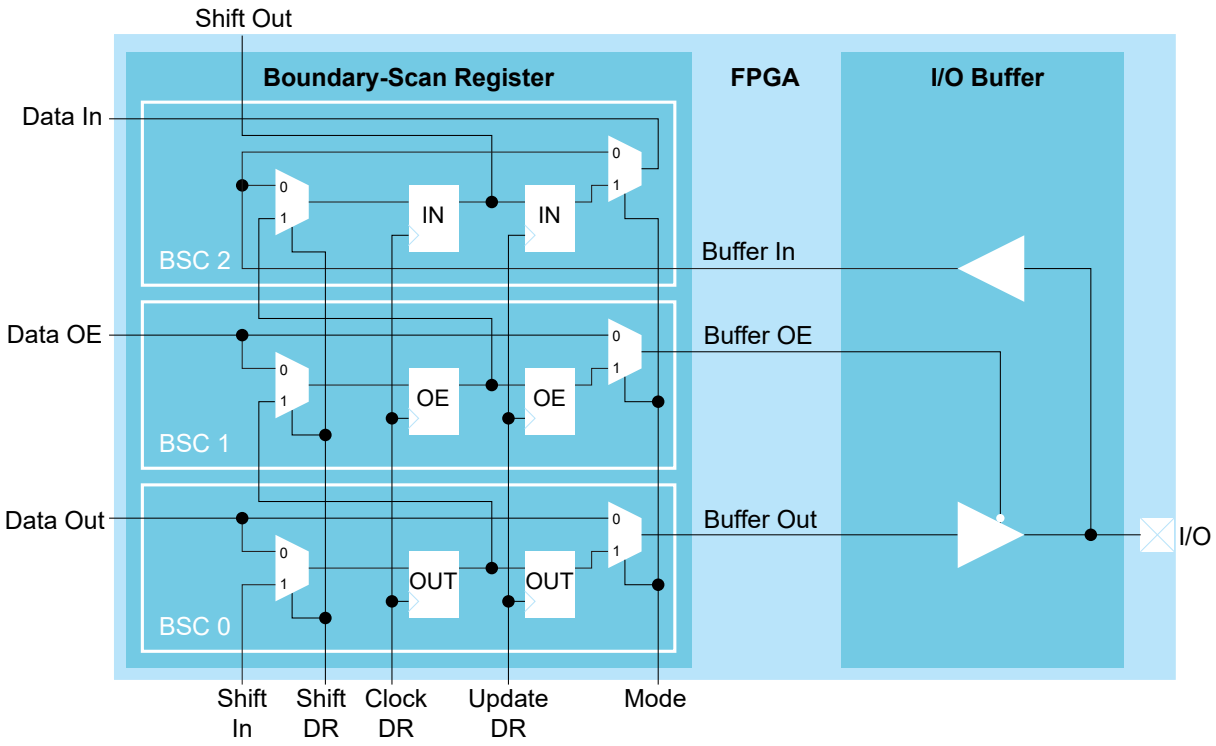
Boundary-Scan Register

The boundary-scan register has data in, data OE, and data out signals connected to the FPGA core while buffer in, buffer OE, and buffer out signals are connected to the pad through the buffers. The `Shift DR`, `Clock DR`, and `Update DR` signals are the control signals generated by the TAP controller. The `Clock DR` signal supplies the clock to the capture register (flip-flops on the left). The `Shift DR` signal which controls the input multiplexers allows the register to capture the pin's states when low and shift the data when high. The `Update DR` signal supplies the clock to the update register (flip-flops on the right), which causes the data used to control the pin stored in the register. The `Mode` signal is generated by the instruction register to control the output multiplexers. The `Mode` signal is low during `SAMPLE/PRELOAD` instruction and high during `EXTEST` instruction.

GPIO Pins

The following figure shows the boundary-scan register on GPIO pins.

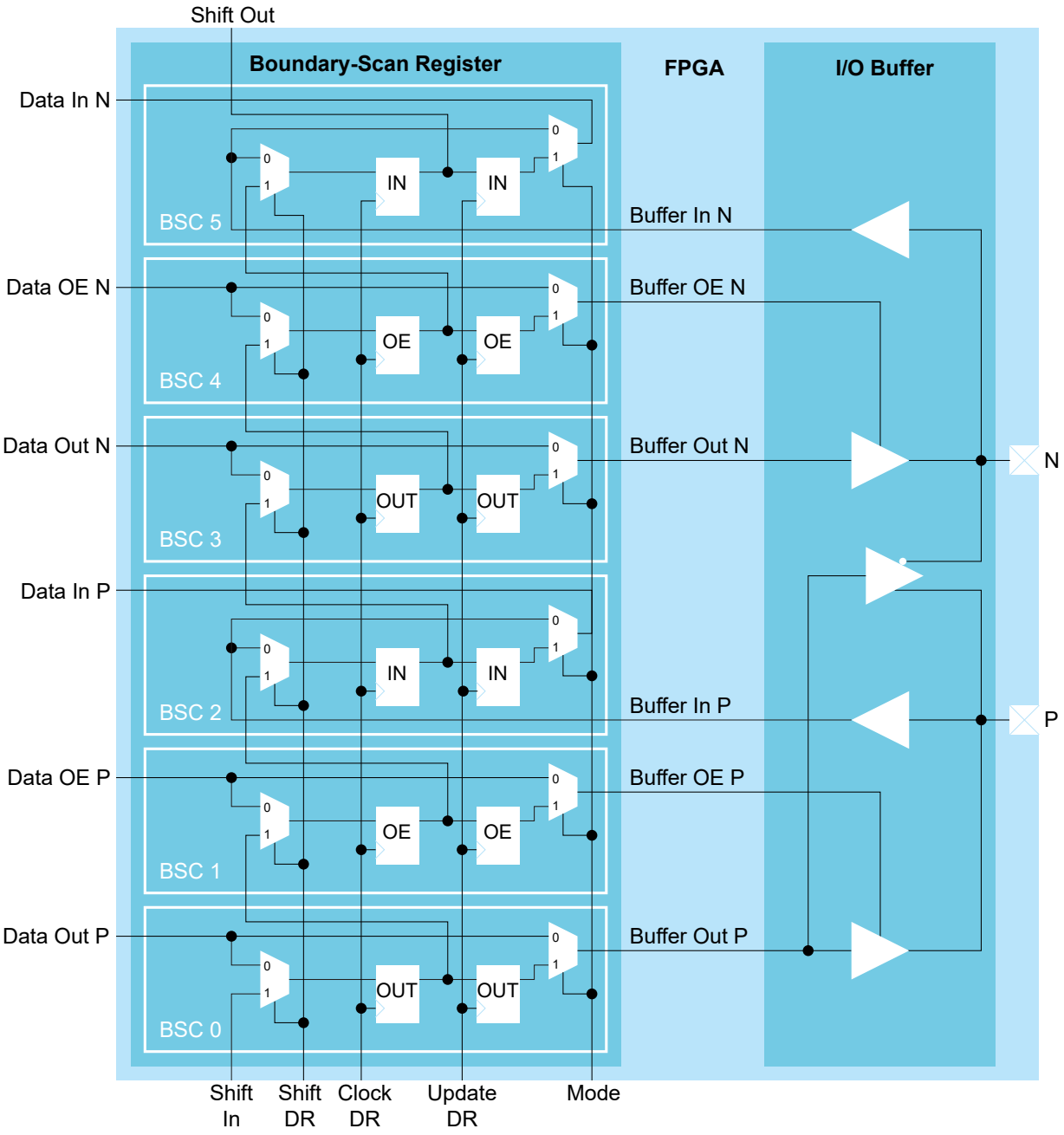
Figure 3: Trion FPGA IEEE Std. 1149.1 Boundary-Scan Register on GPIO Pins



LVDS Pins

The following figure shows the boundary-scan register on LVDS pins.

Figure 4: Trion FPGA IEEE Std. 1149.1 Boundary-Scan Register on LVDS TX Pins



Note: The differential buffer is only enabled on the configured device.

The signal path that passes from the LVDS TX pad through to the I/O buffer changes depending on the I/O standard you are using. The following figures show the paths for the supported standards. The blue color line indicates the signal path. The black lines are unused paths.

Figure 5: I/O Buffer Path for LVCMOS and LVTTL

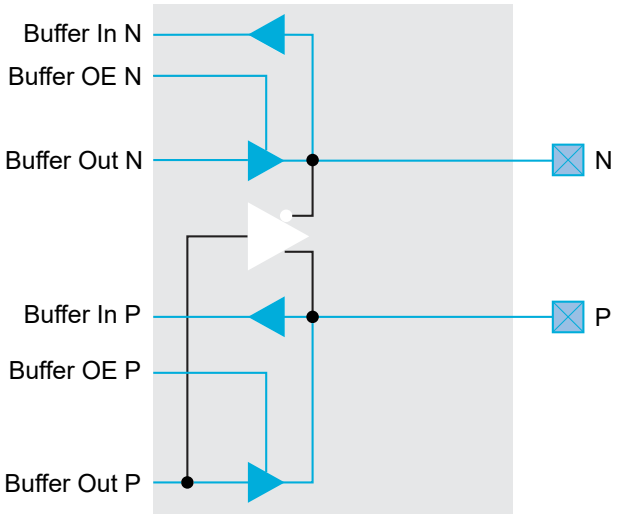
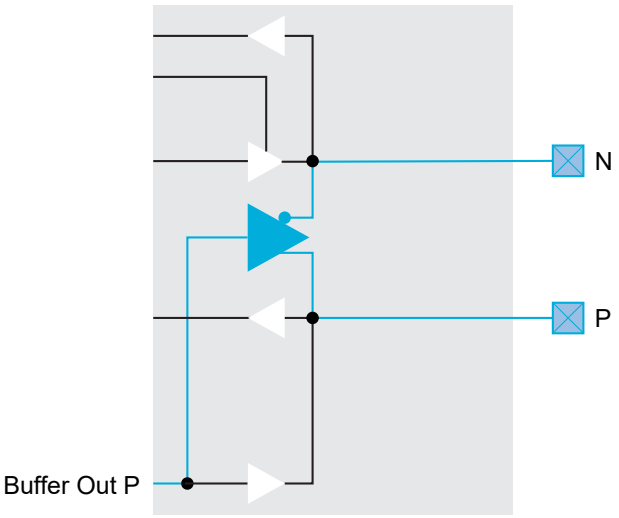
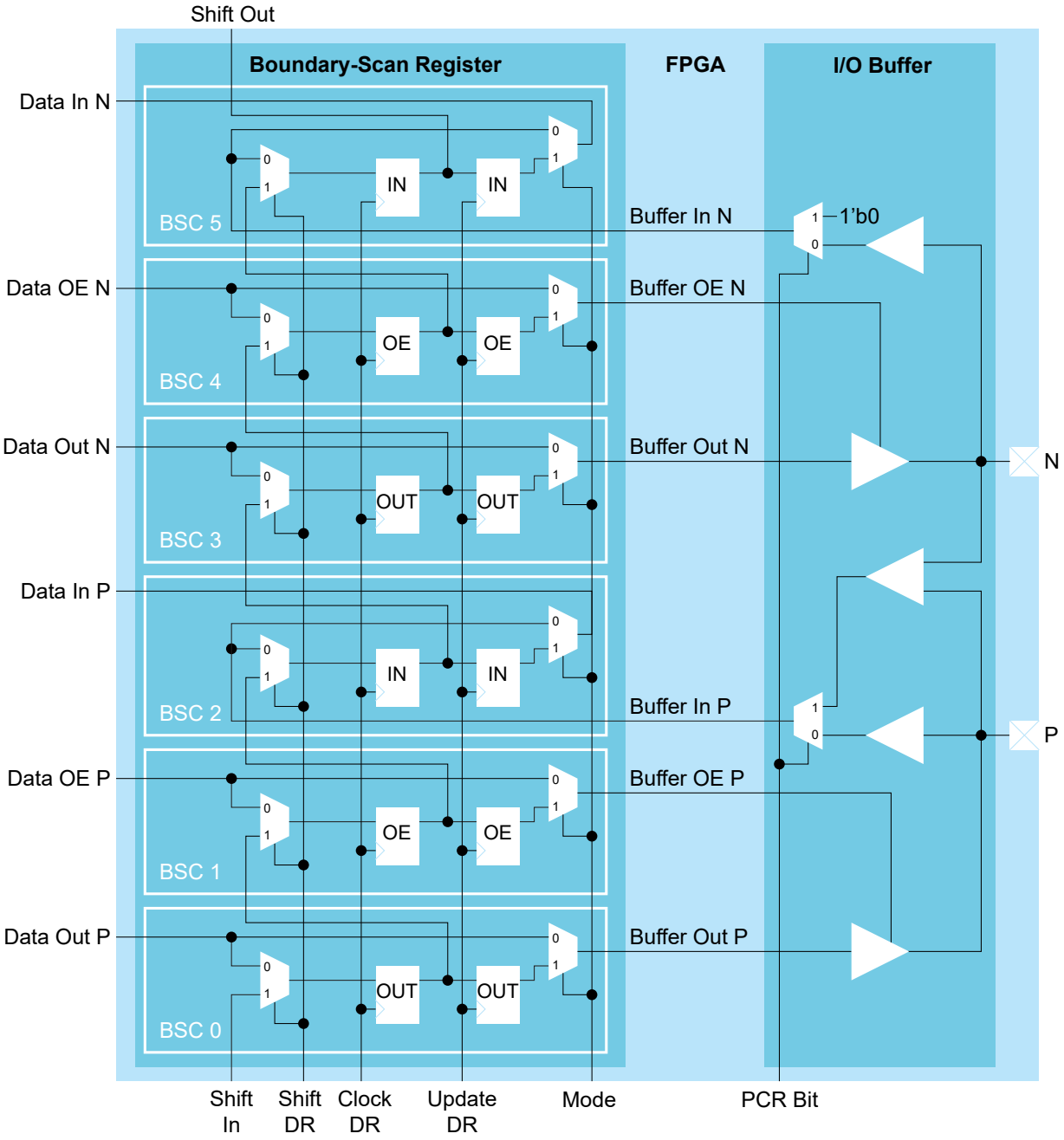


Figure 6: I/O Buffer Path for LVDS TX



The following figure shows the boundary-scan register on LVDS RX pins.

Figure 7: Trion FPGA IEEE Std. 1149.1 Boundary-Scan Register on LVDS RX Pins



The signal path that passes from the LVDS RX pad through to the I/O buffer changes depending on the I/O standard you are using. The following figures show the paths for the supported standards. The blue color line indicates the signal path. The black lines are unused paths.

Figure 8: I/O Buffer Path for LVCMOS and LVTTL

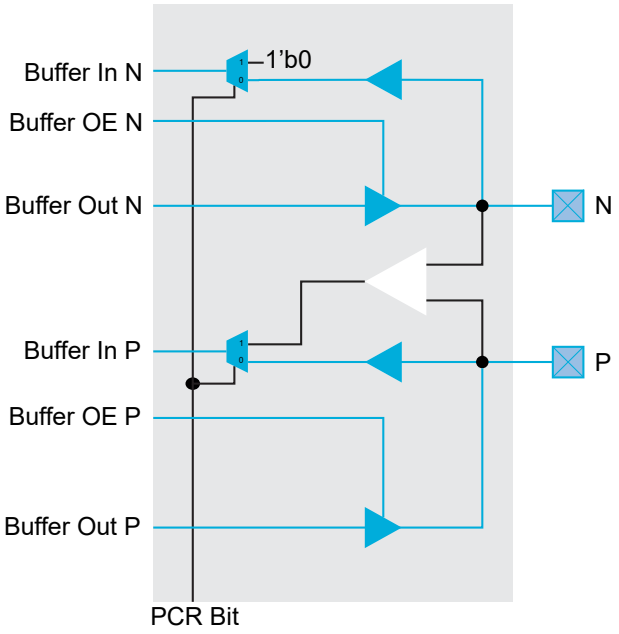
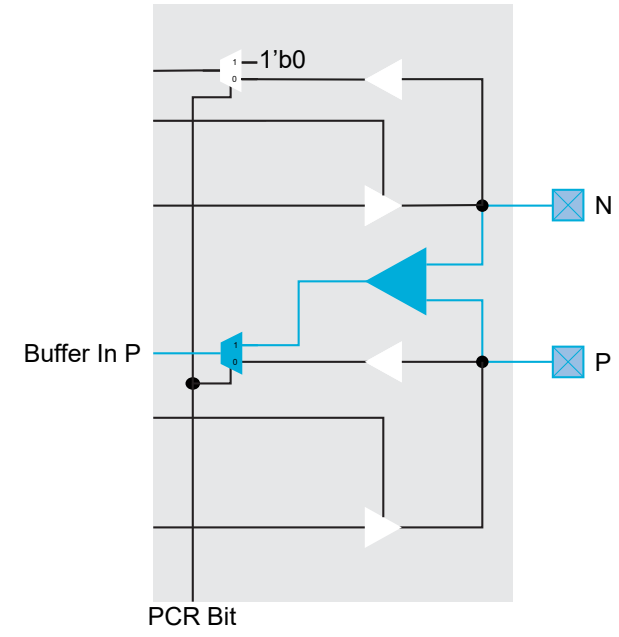


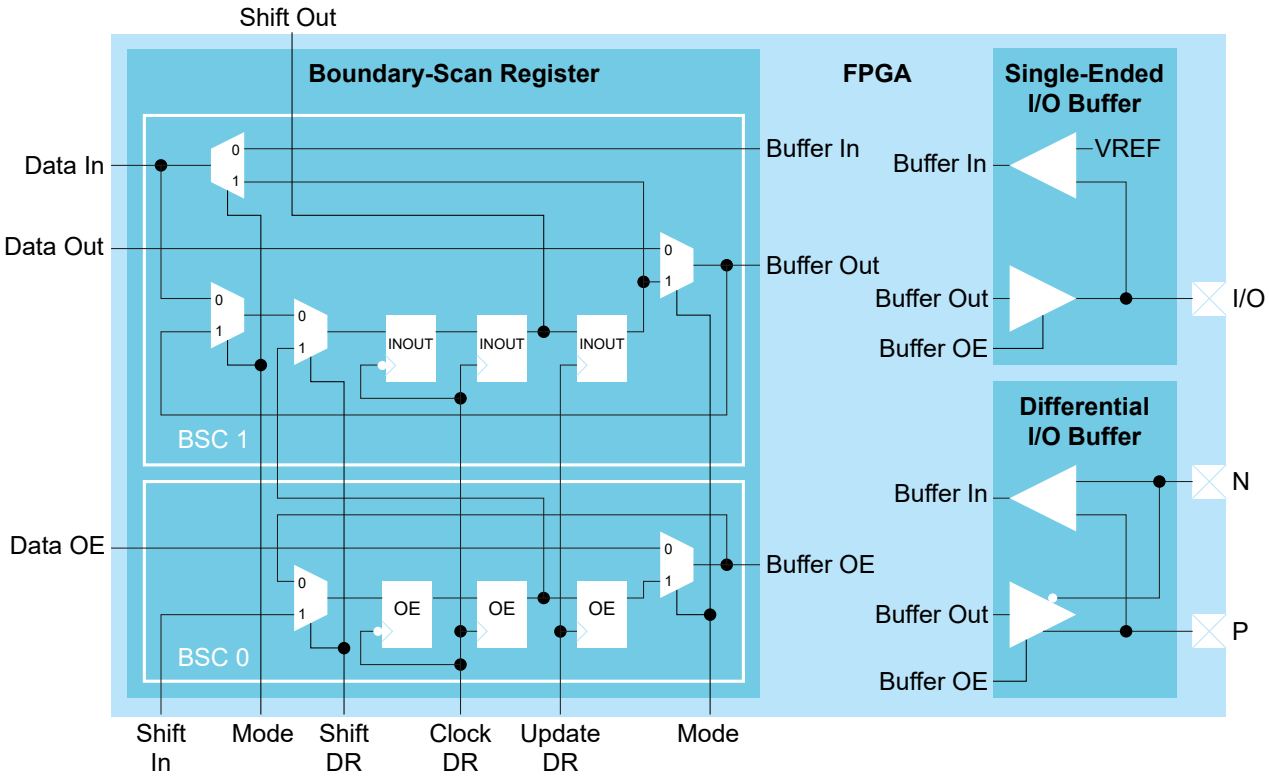
Figure 9: I/O Buffer Path for LVDS RX



Dedicated DDR Pins

The following figure shows the boundary-scan register on single-ended and dedicated differential DDR pins.

Figure 10: Trion FPGA IEEE Std. 1149.1 Boundary-Scan Register on DDR Pins



Note: Only `DQ`, `DM`, and `DQS` pins have buffer in connection. Each differential DDR pin pair has one set of boundary-scan cells.

Boundary-Scan Testing

GPIO Pins

Each GPIO pins consist of 3 boundary-scan cells which are used for input, output, and output enable.

During the boundary-scan testing on the unconfigured device, the boundary-scan register can control and monitor the input, output, and output enable states. The GPIO pins are in **weak pullup** mode.

During the boundary-scan testing on the configured device, the boundary-scan register can control and monitor the input, output, and output enable states for any GPIO modes (**input**, **output**, **inout**, **clkout**, and **none**). Unused GPIO pins are tri-stated and are configured in **weak pullup** mode. You can change the default mode to **weak pulldown** in the Interface Designer.

LVDS Pins

Each LVDS pin consists of 3 boundary-scan cells which are used for input, output, and output enable. In total, there are 6 boundary-scan cells for each pair of LVDS pins.

During the boundary-scan testing on the unconfigured device, all the differential buffer paths are disabled. However, the boundary-scan register can control and monitor the input, output, and output enable states in the single-ended buffer paths. Exceptions are T8 (Q144 package), T13 (all packages), and T20 (Q100, Q144, F169, and F256 packages) which are only able to control and monitor the output and output enable states. The LVDS pins are not in either a **weak pullup** or a **weak pulldown** mode.

During the boundary-scan testing on the configured device, the boundary-scan register can control and monitor the states of the enabled I/O buffer paths. The I/O buffer paths are determined by the GPIO modes and the I/O standards in the Interface Designer. For the LVDS pins pair which is configured as differential I/O, you need to use the P pin to drive or monitor the differential signal since the differential buffer path is connected to the boundary-scan cell of that pin.

Note: The boundary-scan has no access to enable or disable the differential buffer.

Dedicated Configuration Pins

The JTAG pins (`TCK`, `TDI`, `TDO`, and `TMS`) are not testable as these pins are not connected to the boundary-scan cells. The `CONDONE` and `CRESET_N` pins consist of observe-only cells which are able to monitor the signal states but are not able to drive the pins.

Dedicated MIPI Pins

The dedicated MIPI pins are not testable as these pins do not have boundary-scan cells.

Dedicated DDR Pins

Each dedicated DDR pin consists of 2 boundary-scan cells which are used for bidirectional, and output enable.

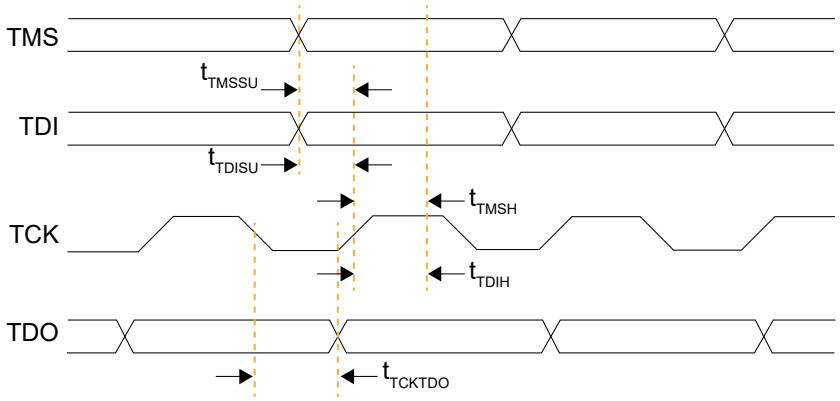
The **SAMPLE/PRELOAD** instruction only allows the boundary-scan register to monitor the input and output enable states. In addition, the **EXTEST** instruction allows the boundary-scan register to control the output and output enable states. However, it is not able to monitor the input state.

Boundary-Scan Description Language

Efinix provides Boundary-Scan Description Language (BSDL) files to describe the IEEE Std. 1149.1 features of each Trion FPGA. You can use the BSDL files to perform test program generation, boundary-scan testing, and failure analysis. Each Trion FPGA has its dedicated BSDL file. You can obtain the BSDL files from the Support Center and the post-configuration BSDL file in your project's outflow. The Interface Designer creates the post-configuration BSDL file when you generate constraints.

Timing Parameters

Figure 11: Boundary-Scan Timing Waveform



Learn more: Timing requirements are important to ensure a successful boundary-scan operation. Refer to the respective Trion data sheet for timing specifications.

Revision History

Table 7: Revision History

Date	Version	Description
June 2023	1.2	Updated BST support and added QFP100F3 package support. (DOC-1346)
November 2022	1.1	Added JTAG device IDs for T20BGA324 and T20BGA400. Added Boundary-Scan Register topic. (DOC-953) Added Boundary-Scan Testing topic. (DOC-953) Added explanation for post-configuration BSDL file. (DOC-953)
June 2020	1.0	Initial release.