AN 030: Using the Titanium Power Estimator

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Contents

Introduction

Designing low-power systems has become increasingly important. Battery-powered, handheld, IoT, and mobile applications are obvious power-sensitive systems. However, even in power-hungry systems just a few percent of power savings can translate into significant operating cost reductions.

Each Titanium FPGA has its own unique power profile. Therefore, Efinix provides a power estimator for each family member. These tools are Excel spreadsheets with macros. You select the specifications of the FPGA you want to use, add information about your design, and the estimator calculates the projected power consumption.

Note: The power estimators are just that - an estimate. They are intended to help guide your decision making process as you pick an FPGA and plan your design. You should verify the actual power consumption in system.

Total Tab

The Total tab is where you provide high-level information about your target FPGA and your system's thermal profile. It also displays power estimation summaries. Spreadsheet cells with a blue background are either static or calculated. White cells are for user input.

Device Settings

Enter data about the FPGA you want to use in the Device Settings table. Different FPGAs consume different amounts of power for the same design. For example, a larger FPGA consumes more power than a smaller one.

Table 1: Device Settings

Option	Choices	Notes
Package	Dependent on the FPGA	The package size affects the thermal resistance. The number of tabs in the spreadsheet changes based on the package you choose.
Grade	Commercial, Industrial	Commercial is 0 to 85 °C. Industrial is -40 to 100 °C.
Condition	Typical, Maximum	Choose the static leakage power to mimic. Typical is the average expected leakage. Maximum is the worst case leakage.

Thermal Profile

The estimator performs thermal analysis based on the FPGA you choose, the ambient temperature, and the airflow. The FPGA itself is a heat source, so the ambient temperature while it is operating, and the amount of cooling, if any, affects the overall power consumption.

The estimator calculates the effective Θ_{JA} and junction temperature based on your selections.

Table 2: Thermal Profile

Option	Choices	Notes
Ambient Temperature (°C)	User defined.	Enter the ambient temperature under which you expect your system to operate. Efinix recommends that you do not operate the FPGA at temperatures higher than the shown maximum ambient temperature.
Airflow	0.0 m/s	Default value is 0.0 m/s which is still air.
Board Thermal Profile	JEDEC (2s2p)	This the profile that Efinix has modeled.
Effective Theta-JA (°C/W)	Default	Only default value is available.

The **Notes** field shows warning messages if the junction temperature exceeds the user selected operating temperature range or if there is a thermal runaway causing the leakage power to never converge.

Power Supply Summary

The Power Supply Summary table shows the estimated current consumption in mA for each voltage domain for the resource utilization you specify. This summary includes static and dynamic power consumption. These values help you to determine the specifications for the power regulator to use on your board.

Block Power Summary

The Block Power Summary table shows the DC and dynamic power consumption totals from the other tabs in the worksheet.

The static power shows the leakage power and power from `VCCAUX`, which is a combination of the thermal profile parameters and the selected FPGA.

The total power shows the DC power + dynamic power.

MIPI Estimate Core Power

The MIPI Estimate Core Power shows the estimation of the power consumption of MIPI implementation in your design in mW. The MIPI Estimate Core Power value is calculated from values inserted in the HSIO Configured as MIPI Lanes table of the GPIO tab.

- If you already have a design using HSIO as MIPI lanes, you get resources from the synthesis report and enter it in the HSIO Configured as MIPI Lanes table of the GPIO tab. In this scenario, the estimator includes the MIPI Estimate Core Power value in the Total Power value.
- If you have not created a design yet and are just exploring power options, include the planned HSIO as MIPI lane usage in the HSIO Configured as MIPI Lanes table of the GPIO tab. In this scenario, the estimator does not include the MIPI Estimate Core Power value in the Total Power value. To get the actual total power including MIPI, add MIPI Estimate Core Power to the Total Power.

Logic, Memory, and DSP Tabs

Your design will have at least one, and probably more, modules. To get a better power estimation, list the modules, their clock frequency, number of look-up tables (LUTs), number of memory blocks, and number of DSP on these tabs.

If you already have an Efinity design, you can obtain this data from the Module Resource Usage Distribution Estimates section in the placement report file.

Tip: Click on the column heading to view pop-up help.

About the Toggle Percentage

The AF column represents the average percentage of logic that toggles on each clock cycle. The default, 12.5%, is an industry accepted average. You can adjust the toggle rate higher, or lower, based on the operation you expect for the module.

Clock Tab

Power consumption is strongly correlated to the clock usage. On this tab you enter the clocks, their frequency, and the flip-flops.

If you already have an Efinity design, you can obtain this data from the synthesis report file.

GPIO Tab

Titanium I/O pins support several I/O standards. You use this tab to summarize how many input, output, and inout (bidirectional) pins your design uses.

The estimator only needs you to enter the number of input pins for 1.8 V LVDS. The input pin power consumption for the other standards is negligible.

For the 1.8 V LVDS standard, you can select the output differential and output pre-emphasis.

You can specify the data rate: single data rate (SDR) or double data rate I/O (DDR). In Efinity® report files, pins that use double data rate I/O are indicated as `DDIO`.

For outputs and inout pins, enter the pin loading (in pF) in the Load (pf) cell or use the default, which is 1.2. This value is the total load, including the die capacitance + package capacitance + board (off chip) capacitance. For general estimation, the die + package capacitance is about 1 - 2 pF; can use 2 to be more conservative. So if your off-chip capacitance is 10 pF, you would enter 12 pF (2 + 10) in the Load cell.

The Output Enable column represents that average percentage of time that the output pins are enabled and inout pins are outputs and enabled. The default is 100%.

You can also adjust the AF percentage. See **About the Toggle Percentage** on page 5

HSIO Configured as MIPI Lanes

Titanium HSIO can be configured as MIPI TX or RX lanes. You use this tab to summarize how many input and output lanes your design uses. The estimator estimates the I/O power, core power and total power for each lane.

Each row represents one MIPI channel. Enter the modules, number of MIPI lanes, their mode, data rate, active factor, percentage of time the lane is in high-speed (HS) mode.

See **About the Toggle Percentage** on page 5 for information about the active factor.

PLL Tab

The PLL tab captures data about the PLLs your design uses. Enter the output frequency and VCO frequency for each PLL.

Table 3: Frequency Settings

Setting	Description
Output Clock Frequency (MHz)	In this column, insert the highest value of the output clock frequency. For example, if you have three PLL output clocks, 10 MHz, 20 MHz, and 50 MHz, use the **50**. Valid values are 0.1342 to 1000, where 0 represents no clock output.
VCO Frequency (MHz)	Insert a number between 2200 and 5500.

HyperRAM Tab

This tab is visible only if you choose F100 package in the Total page. The HyperRAM tab contains data about the static and dynamic power consumption for on-chip HyperRAM block that is available in F100 packages. Enter the clock frequency, read active factor, write active factor, and active factor.

See **About the Toggle Percentage** on page 5 for information about the active factor.

Revision History

Table 4: Revision History

Date	Version	Description
October 2021	1.0	Initial release.