Data Pipeline Core User Guide

UG-CORE-DATA-PIPELINE-v1.2
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Contents

Introduction

The Data Pipeline core allows the highest data throughput that is both high-speed and high performance (bubble/void free). This transfer is achieved through robust pipeline design inside the core.

Use the IP Manager to select IP, customize it, and generate files. The Data Pipeline core has an interactive wizard to help you set parameters. The wizard also has options to create a testbench and/or example design targeting an Efinix® development board.

Features

The Data Pipeline core includes the following features:

- Allow the selection of:
  - Normal pipeline with *ready* back pressure.
    - Maximum area saving.
  - High-bandwidth and high-performance pipeline with registered *ready* back pressure.
    - The *ready* signal is registered to ease the timing closure during high-speed data transfer.
      - `downstream_ready_i` to `upstream_ready_o` path is cut off by a register.
    - No bandwidth performance degradation.
- Multiplexer implementation location is configurable based on user's preference and critical path location.

Device Support

Table 1: Data Pipeline Core Device Support

FPGA Family	Supported Device
Trion	All
Titanium	All
Topaz	All

Resource Utilization and Performance

Note: The resources and performance values provided are based on some of the supported FPGAs. These values are just guidance and can change depending on the device resource utilization, design congestion, and user design.

Table 2: Titanium Resource Utilization and Performance

FPGA	Location of Multiplexer Logic	Data Width	Logic Elements (Logic, Adders, Flipflops, etc.)	Memory Block	DSP Block	f_{MAX} (MHz)[1]	Efinity Version[2]
Ti180 M484 C4	High-Bandwidth and High-Performance Pipeline						
	Input	16	37/172,800 (0.02%)	0/1,280 (0%)	0/640 (0%)	910	2023.2
		64	133/172,800 (0.08%)	0/1,280 (0%)	0/640 (0%)	840	
		256	517/172,800 (0.30%)	0/1,280 (0%)	0/640 (0%)	650	
	Output	16	52/172,800 (0.03%)	0/1,280 (0%)	0/640 (0%)	1050	
		64	196/172,800 (0.11%)	0/1,280 (0%)	0/640 (0%)	1050	
		256	772/172,800 (0.45%)	0/1,280 (0%)	0/640 (0%)	820	
	Normal Pipeline						
	Input	16	19/172,800 (0.01%)	0/1,280 (0%)	0/640 (0%)	940	2023.2
		64	67/172,800 (0.04%)	0/1,280 (0%)	0/640 (0%)	870	
		256	259/172,800 (0.15%)	0/1,280 (0%)	0/640 (0%)	820	
	Output	16	19/172,800 (0.01%)	0/1,280 (0%)	0/640 (0%)	940	
		64	67/172,800 (0.04%)	0/1,280 (0%)	0/640 (0%)	870	
		256	259/172,800 (0.15%)	0/1,280 (0%)	0/640 (0%)	820	

(1) Using default parameter settings.
(2) Using Verilog HDL.

Table 3: Trion Resource Utilization and Performance

FPGA	Location of Multiplexer Logic	Data Width	Logic Elements (Logic, Adders, Flipflops, etc.)	Memory Block	DSP Block	f_{MAX} (MHz)(1)	Efinity Version(2)
T120 F576 C4	High-Bandwidth and High-Performance Pipeline						
	Input	16	37/112,128 (0.03%)	0/1,056 (0%)	0/320 (0%)	320	2023.2
		64	133/112,128 (0.12%)	0/1,056 (0%)	0/320 (0%)	290	
		256	517/112,128 (0.46%)	0/1,056 (0%)	0/320 (0%)	270	
	Output	16	52/112,128 (0.05%)	0/1,056 (0%)	0/320 (0%)	410	
		64	196/112,128 (0.17%)	0/1,056 (0%)	0/320 (0%)	360	
		256	772/112,128 (0.69%)	0/1,056 (0%)	0/320 (0%)	320	
	Normal Pipeline						
	Input	16	19/112,128 (0.02%)	0/1,056 (0%)	0/320 (0%)	300	2023.2
		64	67/112,128 (0.06%)	0/1,056 (0%)	0/320 (0%)	295	
		256	259/112,128 (0.23%)	0/1,056 (0%)	0/320 (0%)	280	
	Output	16	19/112,128 (0.02%)	0/1,056 (0%)	0/320 (0%)	300	
		64	67/112,128 (0.06%)	0/1,056 (0%)	0/320 (0%)	295	
		256	259/112,128 (0.23%)	0/1,056 (0%)	0/320 (0%)	280	

Release Notes

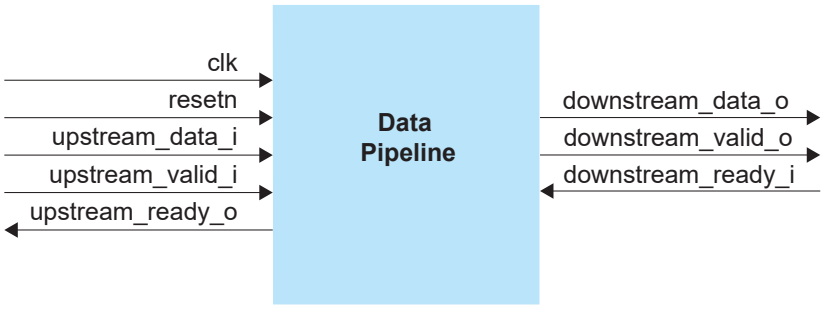
You can refer to the IP Core Release Notes for more information about the IP core changes. The IP Core Release Notes are available on the Efinity Downloads page under each Efinity software release version.

Note: You must be logged in to the Support Center to view the IP Core Release Notes.

Functional Description

The Data Pipeline core is a hand-shaking mechanism where each end of a link can signal data to be sent as *valid* or data to be received as *ready*. When both ends agree (valid and ready), a data transfer occurs on that clock cycle. This mechanism is very useful when pipelining the path between a sender and a receiver for concurrency and/or timing of the data transferred.

Figure 1: Data Pipeline Core Block Diagram



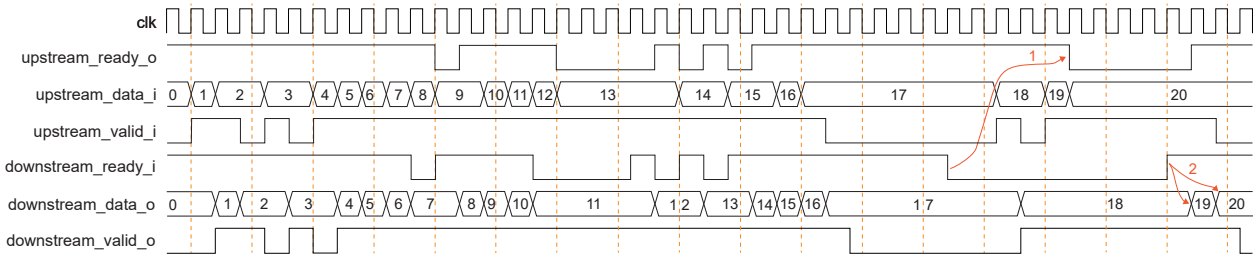
The Data Pipeline core operates as follows:

- The design is using 1 clock and 1 `resetn`.
- The ready signal is registered to cut the path between input and output to ease the timing closure (for `HBP = 1`).
- The `downstream_data_o` and `downstream_valid_o` are in the hold stage when `downstream_ready_i` is de-asserted.
- The multiplexer introduces additional cell delay to the data path. To mitigate the timing closure, you can choose to move the multiplexer to input or output side, depending on the critical path location.
- The **Param** settings are as follows:
  - `HBP == 0`: Normal pipeline implementation with ready back pressure.
  - `HBP == 1`, `MUX_IN == 1`: pipeline ready back pressure with multiplexer logic at input side.
  - `HBP == 1`, `MUX_IN == 0`: pipeline ready back pressure with multiplexer logic at output side.
  - `D_WIDTH`: data width as per design.

For **Param** settings with high-performance turned on, the Data Pipeline core waveform is as follows:

Figure 2: Data Pipeline Core Waveform

With high bandwidth and *ready* signal.



The design has the highest bandwidth performance:

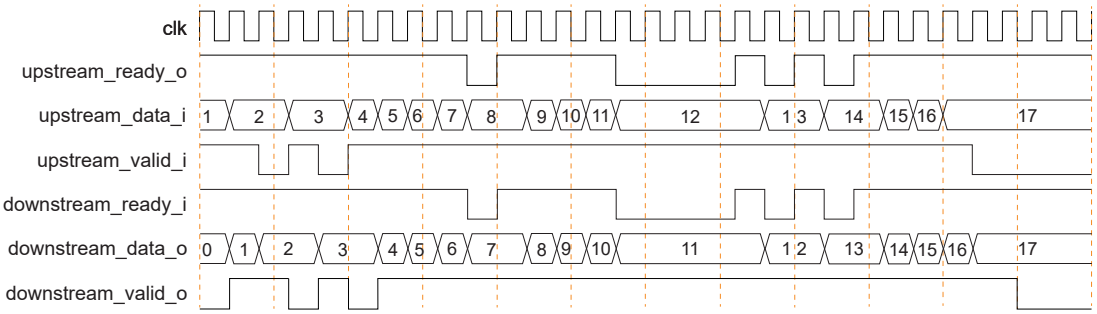
- Pointer 1—Able to take in 2 more data after the `downstream_ready_i` is de-asserted.
- Pointer 2—The data in the buffer can be immediately transffered at the first positive edge when the `downstream_ready_i` wakes up as there is no bubble or void cycle.

Note: The timing diagram for operation of the core is similar regardless of multiplexer placement on the input or output side.

For **Param** settings with high-performance turned off, the Data Pipeline core waveform is as follows:

Figure 3: Data Pipeline Core Waveform

Without *ready* signal.



The design falls back to normal implementation where the ready signal is not in the pipeline. Maximum area saving still applies for as long as no timing closure problem emerges.

Ports

Table 4: Clock and Reset Interface

Port	Direction	Description
clk	Input	All signals are synchronous to this clock.
resetn	Input	Synchronous reset signal that initializes all internal pointers and output flags.

Table 5: Upstream Interface

Port	Direction	Description
upstream_valid_i	Input	Indicates channel is signalling valid data.
upstream_data_i	Input	Content of data.
upstream_ready_o	Output	Logic high indicates downstream port is ready to receive the next transfer.

Table 6: Downstream Interface

Port	Direction	Description
downstream_valid_o	Input	Indicates the valid data is available.
downstream_data_o	Output	Data to be transferred.
downstream_ready_i	Input	Indicates the downstream port can accept data.

IP Manager

The Efinity® IP Manager is an interactive wizard that helps you customize and generate Efinix® IP cores. The IP Manager performs validation checks on the parameters you set to ensure that your selections are valid. When you generate the IP core, you can optionally generate an example design targeting an Efinix development board and/or a testbench. This wizard is helpful in situations in which you use several IP cores, multiple instances of an IP core with different parameters, or the same IP core for different projects.

Note: Not all Efinix IP cores include an example design or a testbench.

Generating the Data Pipeline Core with the IP Manager

The following steps explain how to customize an IP core with the IP Configuration wizard.

1. Open the IP Catalog.
2. Choose **Bridge and Adaptors > Data Pipeline** core and click **Next**. The **IP Configuration** wizard opens.
3. Enter the module name in the **Module Name** box.

   Note: You cannot generate the core without a module name.

4. Customize the IP core using the options shown in the wizard. For detailed information on the options, refer to the *Customizing the Data Pipeline* section.
5. (Optional) In the **Deliverables** tab, specify whether to generate an IP core example design targeting an Efinix® development board and/or testbench. These options are turned on by default.
6. (Optional) In the **Summary** tab, review your selections.
7. Click **Generate** to generate the IP core and other selected deliverables.
8. In the **Review configuration generation** dialog box, click **Generate**. The Console in the **Summary** tab shows the generation status.

   Note: You can disable the **Review configuration generation** dialog box by turning off the **Show Confirmation Box** option in the wizard.

9. When generation finishes, the wizard displays the **Generation Success** dialog box. Click **OK** to close the wizard.

The wizard adds the IP to your project and displays it under **IP** in the Project pane.

Generated Files

The IP Manager generates these files and directories:

- **<module name>_define.vh**—Contains the customized parameters.
- **<module name>_tmpl.v**—Verilog HDL instantiation template.
- **<module name>_tmpl.vhd**—VHDL instantiation template.
- **<module name>.sv**—IP source code.
- **settings.json**—Configuration file.
- **Testbench**—Contains generated RTL and testbench files.

Customizing the Data Pipeline

The core has parameters so you can customize its function. You set the parameters in the **General** tab of the core's IP Configuration window.

Table 7: Data Pipeline Core Parameters (General Tab)

Parameter	Options	Description
Enable High-Bandwidth and High-Performance Pipeline (HBP)	Yes, No	Yes: High-bandwidth and high-performance pipeline with registered *ready* back pressure. No: Design falls back to normal implementation without the *ready* signal in the pipeline. Maximum area saving still applies for as long as no timing closure problem emerges.
Data_Width	User defined	Data width.
Location of Multiplexer Logic (MUX_IN)	Input, Output	The multiplexer introduces additional cell delay to the data path. Users can choose to move the multiplexer to the input or output side, depending on the critical path location.

Data Pipeline Testbench

You can choose to generate the testbench when generating the core in the IP Manager Configuration window. To generate testbench, the **Optional Signals** option must be enabled.

Note: You must include all **.v** files generated in the **/testbench** directory in your simulation.

Important: Efinix tested the testbench generated with the default parameter options only.

Efinix provides a simulation script for you to run the testbench quickly using the Modelsim software. To run the Modelsim testbench script, run `vsim -do modelsim.do` or `sh run_modelsim.sh` in a terminal application. You must have Modelsim installed on your computer to use these scripts.

The testbench is designed with 256-bit data width and supports the following :

- Enable/disable high-bandwidth and high-performance pipeline.
- Multiplexer logic at input/output.

The testbench outputs only if there is a passing or failing of the simulation.

Revision History

Table 8: Revision History

Date	Document Version	IP Version	Description
November 2024	1.2	6.4	Added Topaz in Device Support. (DOC-2176) Added IP Version in Revision History. (DOC-2185)
April 2024	1.1	–	Updated Resource and Performance Utilization. (DOC-1800) Updated Testbench. Changed all slave_* and master_* to downstream_* and upstream_* respectively. Added important note in Example Design and Testbench regarding using default parameters options only. (DOC-1781)
January 2024	1.0	–	Initial release. (DOC-1627)