Titanium DDR DRAM Block User Guide

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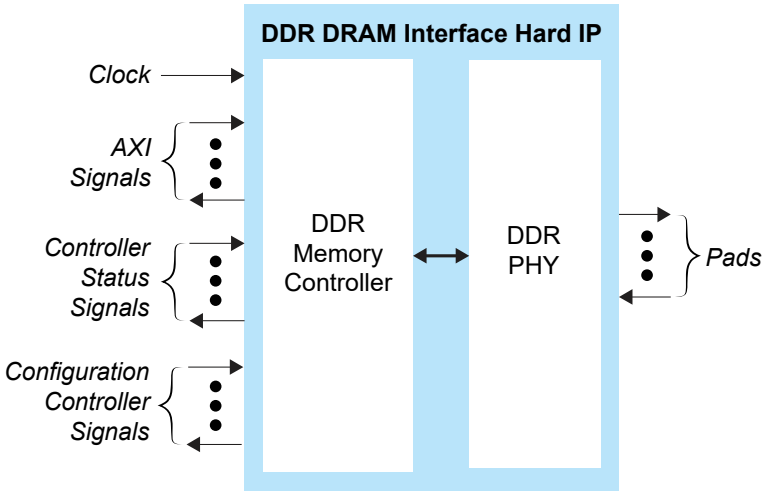
Introduction

The Titanium DDR DRAM hardened memory controller and PHY provides a robust and complete solution to implement an external memory interface to a LPDDR4/LPDDR4x DRAM device. When the block is hardened, it provides a power and area-efficient solution.

Figure 1: DDR DRAM Interface Hard IP Block Diagram



Features

- Supports LPDDR4 and LPDDR4x protocol
- DDR PHY supports data rates up to 3,300 Mbps
- Programmable termination with calibration to compensate for variations across power, voltage, and temperature (PVT)
- Supports various hardware calibrations for optimal performance
- User configurable data width support: x16 or x32 depending on the FPGA and package
- User configurable timing parameters
- Supports up to 2 AXI interfaces with multiple accesses:
  - Data width up to 512 bits to allow a flexible system interconnect to the FPGA core
  - Includes a built-in arbiter to manage memory read and write requests from multiple sources

DDR Comparison

Efinix® strongly recommends you to design with LPDDR4x with better performance and lower power consumption.

Table 1: Titanium DDR Features

Feature	LPDDR4	LPDDR4x
VDD (mV)	850	850
VDDQ (mV)	1100	620
V_{REF} DQ (mV)	0.167 x VDDQ(1)	0.167 x VDDQ(1)
Maximum frequency (DDR controller)	1.65 GHz(2)	1.65 GHz(2)
Burst lengths	8/16	8/16
Configuration	x16, x32	x16, x32
Address commands signals	6 Pins	6 Pins
CA bus data rate	Single	Single
DQ bus data rate	Double	Double
Output drive strength (Ω)	Programmable(1)	Programmable(1)
CA training	✓	✓
DQ Read Training	✓	✓
DQ Write Training	✓	✓
V_{REF} DQ Training	✓	✓
DQS Interval Oscillator	✓	✓
ZQ Calibration	✓	✓
Write leveling	✓	✓
Read leveling	✓	✓
Pre-bank refresh	✓	✓
Interface	LVSTL	LVSTL
On-Die Termination (ODT)	✓(1)	✓(1)
Package option	Discrete	Discrete

(1) Refer to your DRAM data sheet.
(2) Refer to **Table 3: LPDDR4/4x and MIPI D-PHY Interface Performance** on page 5 for the maximum data rate supported by package.

Titanium FPGAs with LPDDR4/LPDDR4x DRAM Support

Table 2: DDR DRAM Widths Supported for Titanium FPGAs

FPGA	Package	LPDDR4/4x PHY with Memory Controller	DQ Widths
Ti90, Ti120 and Ti180	J361, M361, M484, F529	1 block	x16
Ti90, Ti120 and Ti180	J484, G529	1 block	x16 or x32
Ti135, Ti200, and Ti375	C529	1 block	x16 or x32

Supported Frequencies and Configurations

The following table shows the maximum DDR interface data rate. You need to validate the actual data rate supported by your system.

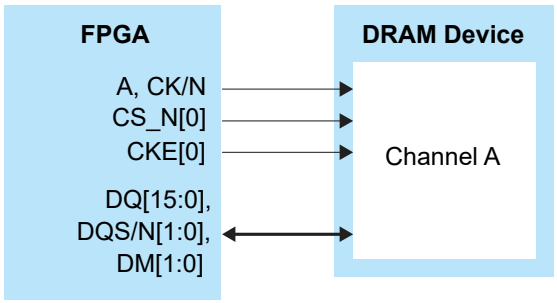
Table 3: LPDDR4/4x and MIPI D-PHY Interface Performance

Description	FPGA Speed Grade		Units
	C4, I4, C4L, I4L	C3, I3, C3L, I3L	
LPDDR4/4x DRAM interface maximum data rate.	3.3	2.8	Gbps
MIPI D-PHY block maximum data rate.	2.5	2.0	Gbps

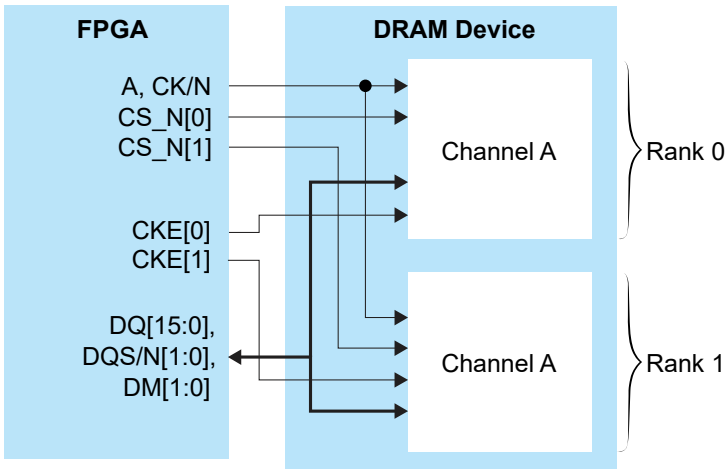
Note: Efinix® recommends LPDDR4x for lower power and better performance.

The following LPDDR4 and LPDDR4x configurations are supported. The figures show the connections between the FPGA and the DRAM device.

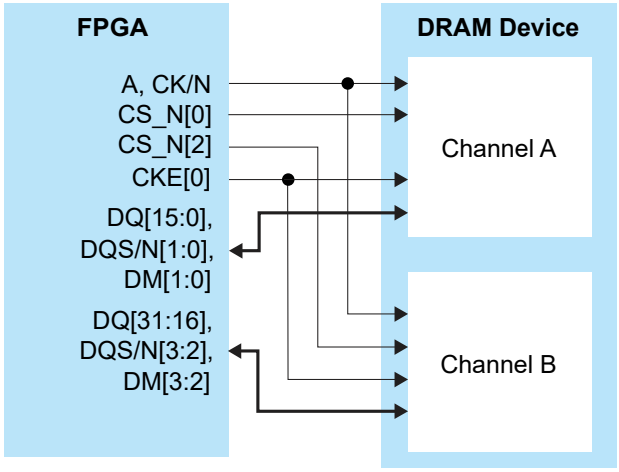
Single-Rank, x16 Interface



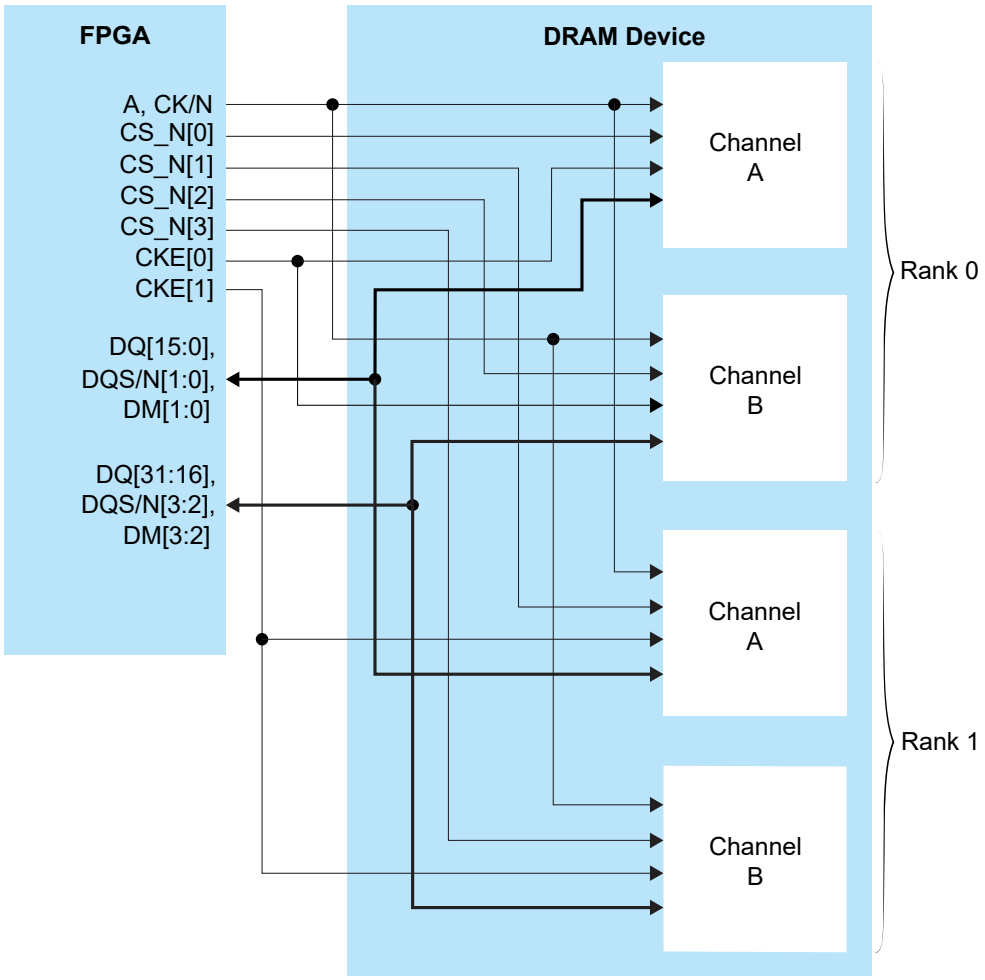
Dual-Rank, x16 Interface



Single-Rank, x32 Interface



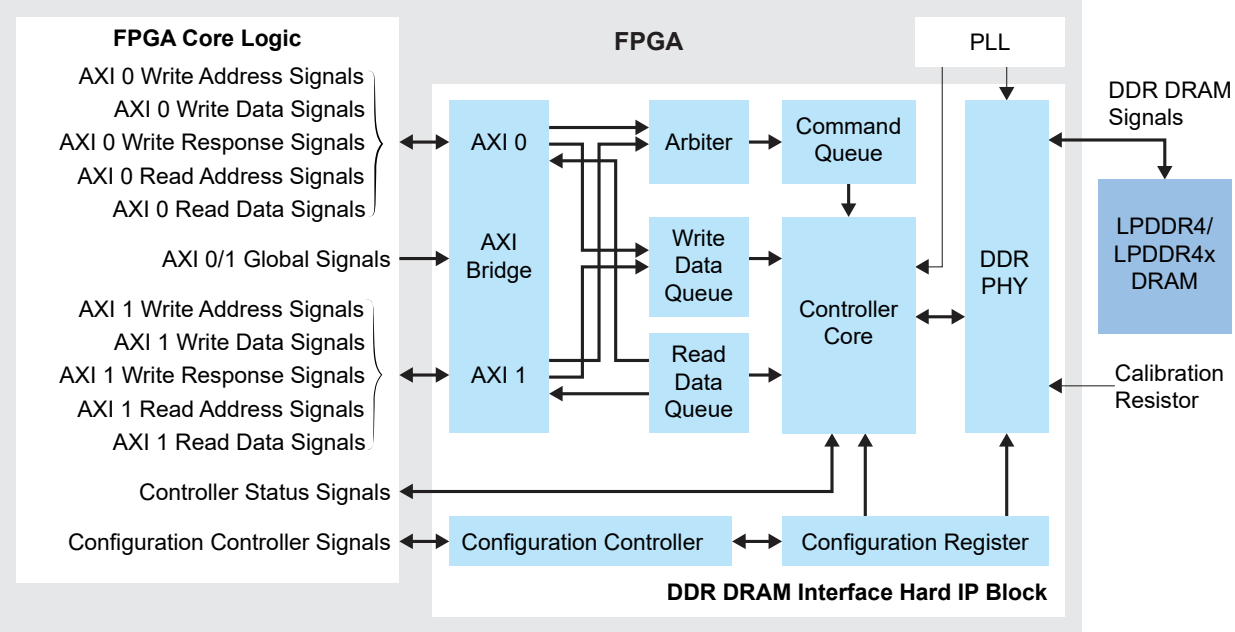
Dual-Rank, x32 Interface



Functional Description

The following figure shows the DDR DRAM block diagram.

Figure 2: DDR DRAM Interface Hard IP Block Diagram



DDR PHY

The DDR PHY is a physical layer that interfaces with the external DRAM device. It is fully compliant with the LPDDR4 and LPDDR4x electrical specifications. DDR PHY has a built-in data training circuit to enable in-system calibration, which helps optimize the system timing for high performance.

The PHY connects to the DRAM device using the signals in the following table.

Table 4: DDR DRAM Pads

Signal	Direction	Description
DDR_A[5:0]	Output	Address signals to the DRAM.
DDR_CS_N[3:0]	Output	Chip select to the DRAM.
DDR_CKE[1:0]	Output	Active-high clock enable signals to the DRAM.
DDR_RST_N	Output	Active-low reset signal to the DRAM.
DDR_CK	Output	Differential clock signals to the DRAM.
DDR_CK_N	Output	
DDR_DQ[*n*:0]	Bidirectional	Data bus to/from the memories. For writes, the FPGA drives these signals. For reads, the memory drives these signals. These signals are connected to the DQ pins on the memories. *n* is 15 or 31 depending on the Data Width setting.
DDR_DQS_N[*m*:0]	Bidirectional	Differential data strobes to/from the memories. For writes, the FPGA drives these signals. For reads, the memory drives these signals. These signals are connected to the DQS pins on the memories. *m* is 1or 3 depending on the DQ width.
DDR_DQS[*m*:0]	Bidirectional	
DDR_DM[*m*:0]	Bidirectional	Signals used as active-high data-mask and data bus inversion indicator. *m* is 1 or 3 depending on the DQ width. If data bus inversion is enabled for a write operation, the DDR controller will drive the signal high if the write data byte is inverted. Similarly, if data bus inversion is enabled for a read operation, the memory device will drive the signal high if the read data byte is inverted.

DDR Controller

The DDR controller block handles all of the protocols and hand-shaking between the DRAM device and the DDR PHY. It reduces latency of the DRAM device interface and minimizes core logic consumption.

AXI Interface

The DDR DRAM interface hard IP block has two AXI interfaces (target 0 and target 1) that provide an easy, efficient way to access the DRAM device. All AXI signals and operations comply with the AMBA AXI4 specification.

The AXI interfaces support:

- A clock frequency that is asynchronous to the controller clock frequency; a FIFO handles the synchronization between the AXI clock domain and the DDR controller clock domain
- Burst sizes of 1 – 64 bytes
- Burst lengths of 1 – 256 for data transfer
- Read and write strobes (data masking)
- Incrementing and wrapping burst types
- Narrow bus transfers

The following figures are examples of the read-and-write operations.

Figure 3: Read Operation Example

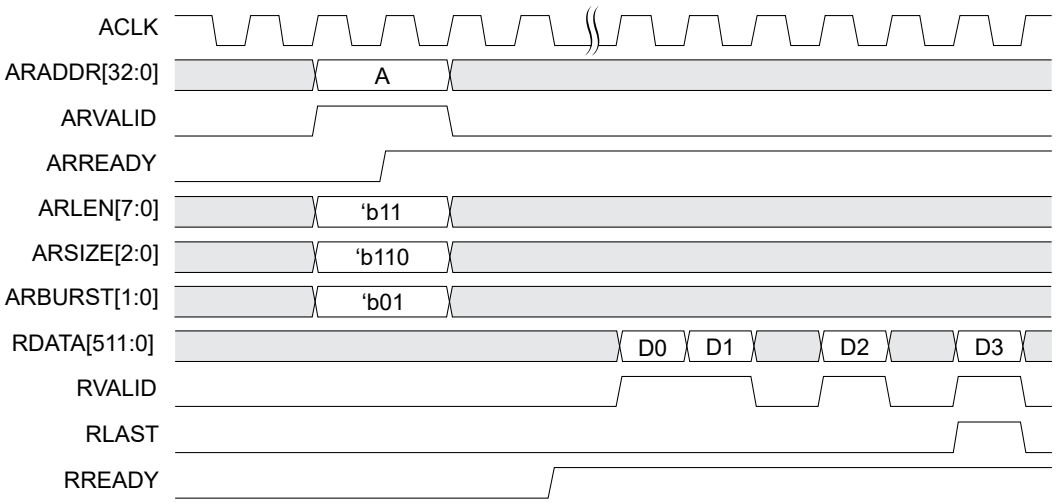
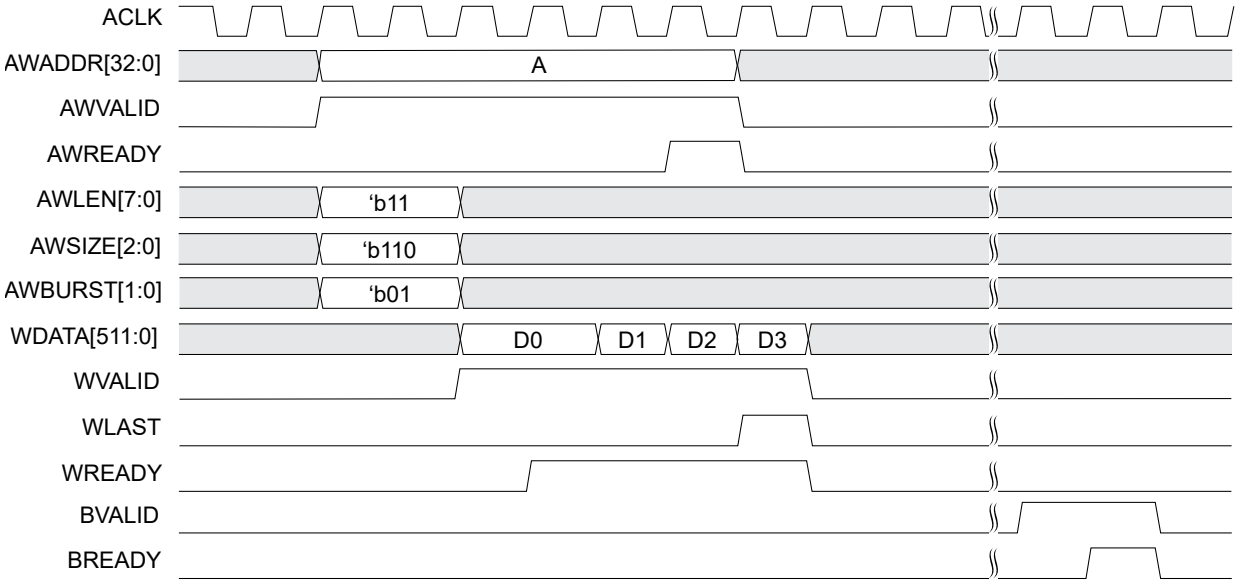


Figure 4: Write Operation Example



Note: `AWREADY` is asserted after both `AWVALID` and `WVALID` are asserted.

Interface Mappings

The AXI data width, AXI burst size, DRAM DQ width, and burst length determine the AXI-to-DQ data mapping. The following example shows the mapping based on these settings:

- AXI data width: 512
- AXI burst size (ASIZE) (number of bytes): 64
- DQ width: 32
- DRAM Burst Length: 16

Table 5: AXI Data to DRAM Device DQ Mapping Example

AXI Data	[511:504]	[503:496]	[495:488]	[487:480]	...	[31:24]	[23:16]	[15:8]	[7:0]
AXI Beat	64	63	62	61	...	4	3	2	1
DQ	[31:24]	[23:16]	[15:8]	[7:0]	...	[31:24]	[23:16]	[15:8]	[7:0]
DRAM Burst	16				...	1			

Table 6: Maximum Burst Length

AWSIZE/ARSIZE	AWLEN/ARLEN
6	≤ 63
5	≤ 127
4	≤ 255

Note: A burst must not cross a 4KB address boundary.

AXI Signals

The following tables describe the read and write AXI interfaces signals.

Table 7: AXI4 Global Signals (Interface to FPGA Core Logic)

Signal	Direction	Clock Domain	Description
ACLK_*x*	Input	N/A	AXI4 clock inputs.
ARSTN_*x*	Input	ACLK_x	Active-low reset signal to the AXI interface.

Table 8: AXI4 Write Address Signals (Interface to FPGA Core Logic)

Signal x is 0 or 1	Direction	Clock Domain	Description
AWADDR_*x*[32:0]	Input	ACLK_x	Write address. It gives the address of the first transfer in a burst transaction.
AWBURST_*x*[1:0]	Input	ACLK_x	Burst type. The burst type and the size determine how the address for each transfer within the burst is calculated.
AWID_*x*[5:0]	Input	ACLK_x	Address ID. This signal identifies the group of address signals.
AWLEN_*x*[7:0]	Input	ACLK_x	Burst length. This signal indicates the number of transfers in a burst.
AWREADY_*x*	Output	ACLK_x	Address ready. This signal indicates that the slave is ready to accept an address and associated control signals.
AWSIZE_*x*[2:0]	Input	ACLK_x	Burst size. This signal indicates the size of each transfer in the burst.
AWVALID_*x*	Input	ACLK_x	Address valid. This signal indicates that the channel is signaling valid address and control information.
AWLOCK_*x*	Input	ACLK_x	Lock type. This signal provides additional information about the atomic characteristics of the transfer.
AWAPCMD_*x*	Input	ACLK_x	Write auto-precharge.
AWQOS_*x*	Input	ACLK_x	QoS identifier for write transaction.
AWCACHE_*x*[3:0]	Input	ACLK_x	Memory type. This signal indicates how transactions are required to progress through a system.
AWALLSTRB_*x*	Input	ACLK_x	Write all strobes asserted. The DDR controller only supports a maximum of 16 AXI beats for write commands using this signal.
AWCOBUF_*x*	Input	ACLK_x	Write coherent bufferable selection.

Table 9: AXI4 Write Data Channel Signals (Interface to FPGA Core Logic)

Signal x is 0 or 1	Direction	Clock Domain	Description
WDATA_*x*[511:0]	Input	ACLK_x	Write data.
WLAST_*x*	Input	ACLK_x	Write last. This signal indicates the last transfer in a write burst.
WREADY_*x*	Output	ACLK_x	Write ready. This signal indicates that the slave can accept the write data.
WSTRB_*x*[63:0]	Input	ACLK_x	Write strobes. This signal indicates which byte lanes hold valid data. There is one write strobe bit for each eight bits of the write data bus.
WVALID_*x*	Input	ACLK_x	Write valid. This signal indicates that valid write data and strobes are available.

Table 10: AXI4 Write Response Channel Signals (Interface to FPGA Core Logic)

Signal x is 0 or 1	Direction	Clock Domain	Description
BID_*x*[5:0]	Output	ACLK_x	Response ID tag. This signal is the ID tag of the write response.
BREADY_*x*	Input	ACLK_x	Response ready. This signal indicates that the master can accept a write response.
BRESP_*x*[1:0]	Output	ACLK_x	Read response. This signal indicates the status of the read transfer.
BVALID_*x*	Output	ACLK_x	Write response valid. This signal indicates that the channel is signaling a valid write response.

Table 11: AXI4 Read Address Signals (Interface to FPGA Core Logic)

Signal x is 0 or 1	Direction	Clock Domain	Description
ARADDR_*x*[32:0]	Input	ACLK_x	Read address. It gives the address of the first transfer in a burst transaction.
ARBURST_*x*[1:0]	Input	ACLK_x	Burst type. The burst type and the size determine how the address for each transfer within the burst is calculated. 'b01 = INCR 'b10 = WRAP
ARID_*x*[5:0]	Input	ACLK_x	Address ID. This signal identifies the group of address signals.
ARLEN_*x*[7:0]	Input	ACLK_x	Burst length. This signal indicates the number of transfers in a burst.
ARREADY_*x*	Output	ACLK_x	Address ready. This signal indicates that the slave is ready to accept an address and associated control signals.
ARSIZE_*x*[2:0]	Input	ACLK_x	Burst size. This signal indicates the size of each transfer in the burst.
ARVALID_*x*	Input	ACLK_x	Address valid. This signal indicates that the channel is signaling valid address and control information.
ARLOCK_*x*	Input	ACLK_x	Lock type. This signal provides additional information about the atomic characteristics of the transfer.
ARAPCMD_*x*	Input	ACLK_x	Read auto-precharge.
ARQOS_*x*	Input	ACLK_x	QoS identifier for read transaction.

Table 12: AXI4 Read Data Channel Signals (Interface to FPGA Core Logic)

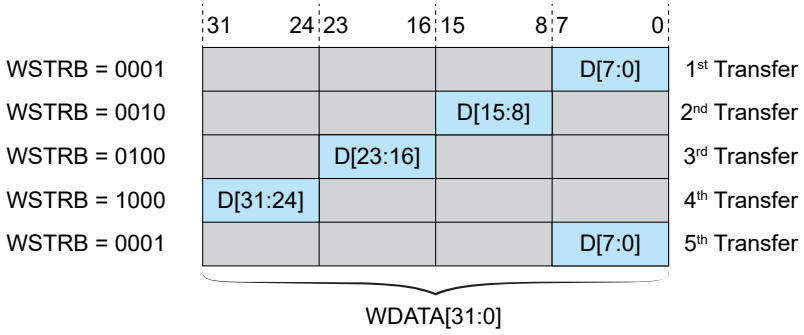
Signal x is 0 or 1	Direction	Clock Domain	Description
RDATA_*x*[511:0]	Output	ACLK_x	Read data.
RID_*x*[5:0]	Output	ACLK_x	Read ID tag. This signal is the identification tag for the read data group of signals generated by the slave.
RLAST_*x*	Output	ACLK_x	Read last. This signal indicates the last transfer in a read burst.
RREADY_*x*	Input	ACLK_x	Read ready. This signal indicates that the master can accept the read data and response information.
RRESP_*x*[1:0]	Output	ACLK_x	Read response. This signal indicates the status of the read transfer.
RVALID_*x*	Output	ACLK_x	Read valid. This signal indicates that the channel is signaling the required read data.

Narrow Transfers

The AXI DDR implementation supports narrow transfers. It is important to set the `WSTRB_x[n:0]` signals correctly when performing narrow transfers. There is one write strobe for each eight bits of the write data bus. A master must ensure that the write strobes are set to logic high for byte lanes that contain valid data.

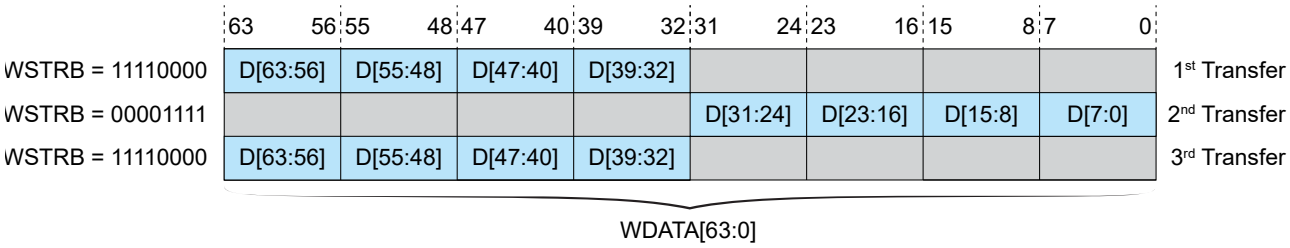
The following figure illustrates an example of a five incremental bursts of an 8-bit transfer on a 32-bit bus with a starting address of 0.

Figure 5: 8-bit Transfer on a 32-bit Bus Example



The following figure illustrates an example of a three incremental burst of a 32-bit transfer on a 64-bit bus with a starting address of 4.

Figure 6: 32-bit Transfer on a 64-bit Bus Example



Learn more: Refer to the AMBA AXI and ACE Protocol Specification for more information about narrow transfer transaction structure.

Arbiter

The arbiter handles simultaneous read and write requests from the AXI 0 and 1 interfaces. It decides which request from the two interfaces to send to the DDR controller based on round-robin arbitration.

The arbiter rotates between the interface numbers. The request of an interface will be sent to the DDR controller when it is its turn if it fulfils the following conditions:

1. That particular interface must have an active request.
2. The DDR controller's command queue is not full.

If an interface's turn comes but there is no active request from that interface, then, that interface will be skipped. This is followed by checking on the other interface. Round-robin operation ensures that each interface's requests can be successfully arbitrated into the controller core every two cycles and no interface will be locked out. Any interface can have its requests serviced at every cycle if the other interface is quiet and the command queue is not full.

Configuration Register

The configuration register stores the settings required for the DDR DRAM interface hard IP block and external memory device to operate properly. During FPGA configuration, this configuration register is programmed automatically by the configuration controller.

Configuration Controller

The configuration controller facilitates the operations required to start the DDR DRAM interface hard IP block and performs the following tasks:

1. Configures the correct settings into the DDR PHY and the controller.
2. Initializes the DRAM device by programming the correct instruction sequence into the controller.
3. Configures the DRAM device **Mode Registers Settings (MRS)**.
4. Works with the DDR PHY to perform calibration and trainings.

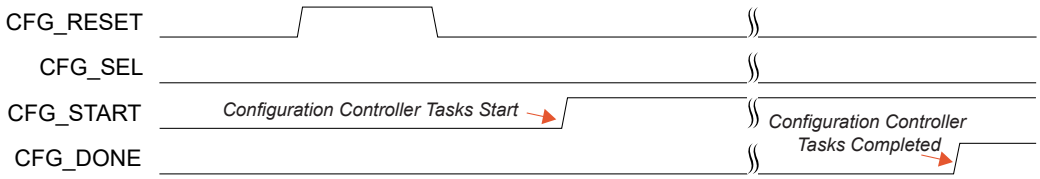
The following table shows the list of signals for the configuration controller.

Table 13: Configuration Controller Signals

Signal	Direction	Description
CFG_RESET	Input	Active-high startup sequencer reset.
CFG_START	Input	Start the startup sequencer.
CFG_DONE	Output	Indicates the startup sequencer is done.
CFG_SEL	Input	Tie this input to low to enable the configuration controller.

The following figure shows the configuration controller signal waveform.

Figure 7: Configuration Controller Signal Waveform



Note:

- CFG_START must stay high even after CFG_DONE goes high.
- CFG_RESET must stay high for at least 5 cycles of the controller clock.

Address Mapping

From the user perspective, the AXI address space is one continuous byte address space starting from byte 0 up to the size limit of the memory device. Behind the scenes, the DDR controller accesses the memory device using bank, column, and row addresses. The data width accessed by each address space is dependent on the DDR controller data width. For example, an x32 data width controller accesses 4 bytes of memory data for each address.

The relationship between the user AXI address and DDR controller address is as follows:

DQ Data Width	DDR Controller & AXI Address Mapping
x32 data width	DDR controller address = AXI address >> 2
x16 data width	DDR controller address = AXI address >> 1

where >> is a Verilog HDL operator that denotes a bit-wise right shift.

Hence, for x32, the least significant bit (LSB) of the DDR controller address is bit 2 (starting from 0) of the AXI address. For x16, the LSB of the controller address is bit 1 of the AXI address.

The AXI address contains 5 fields. The following example shows the AXI address bit numbers for the maximum allowable address space.

32	31:15	14:12	11:2	1:0
Chip select	Row address	Bank address	Column address	Datapath

For accessing lower density memories (with smaller row and column address range), drive the MSBs that are not used with 0s. The following example shows a mapping with MSBs that are not used:

32:28	27	26:12	11:9	8:2	1:0
Not used	Chip select	Row address	Bank address	Column address	Datapath

The chip select, row, bank, and column address fields are used to address an entire memory word, and the datapath bits are used to address individual bytes within that user word. For example, for a read starting at byte address 0x2, the datapath bits must be defined as 'b010 to address this byte directly. Read and write operations are memory word-aligned if all the datapath bits are 0.

Clocking

Depending on the Titanium FPGA package, the DDR DRAM interface hard IP block may require one or two clocks that must be driven directly from the PLL.

DDR DRAM Interface Input Clocks

For M361, M484, and F529 packages, the PLL_TL2 `CLKOUT3` and `CLKOUT4` are clocks to drive the DDR PHY and controller. The `CLKOUT3` drives the DDR PHY and must run at half of the PHY data rate (for example, 2,000 Mbps requires a 1,000 MHz clock). `CLKOUT4` drives the DDR controller and must run at a quarter of the PHY data rate (for example, 2,000 Mbps requires a 500 MHz clock). You only need to instantiate PLL_TL2 with `CLKOUT3` and `CLKOUT4`, enabled with the required frequencies.

For J361, J484, and G529 packages, you only need one clock to drive the DDR DRAM interface block. You can select **CLKIN 0**, **CLKIN 1**, or **CLKIN 2** of the DDR DRAM interface block, which are connected to `CLKOUT4` of PLL_TL0, PLL_TL1, or PLL_TL2, respectively. The clock runs at a quarter of the PHY data rate (for example, 2,000 Mbps requires a 500 MHz clock). You only need to instantiate the `CLKOUT4` of the selected PLL resource, enabled with the required frequencies.

The Efinity software connects the clocks to the DDR DRAM interface block automatically.

Reset and Calibration

The DDR DRAM interface hard IP block has reset inputs that allow you to reset the AXI interfaces, DDR controller, DDR PHY, and DRAM device. The following table summarizes the available resets.

Table 14: Resets

Signal	Description
CFG_RESET	Active-high reset to the Configuration Controller. Asserting this reset will also reset the DDR controller, PHY and the DRAM device.
ARST_X	Active-high reset for the AXI interface.

Note: Efinix recommends that you assert all the resets together after the power supplies are stable.

Asserting `CFG_RESET` resets the DDR controller, DDR PHY, and the DRAM device. After asserting `CFG_RESET`, you should start the Configuration Controller to configure the correct settings into the Configuration Register. Next, initialize the DRAM. The Configuration Controller also works with the DDR PHY to perform the following operations:

- *I/O calibration*—Adjusting the I/O delay for process, voltage, and temperature compensation.
- *CA/CS training*—Aligning the center of the address, command, and chip select to the rising edge of the memory clock.
- *Write leveling*—Aligning the write `DQS` to the memory clock.
- *Read DQS gate training*—Tuning the read `DQS` enable for `DQS` pre-amble.

- *Read data eye training*—Aligning the read DQS to the center of the DQ eye for read operations.
- *Write data eye training*—Aligning the center of the DQ eye to the DQS edge for write operations.

DDR Interface Designer Settings

The following tables describe the settings for the Titanium DDR block in the Interface Designer. The settings should match the DRAM device that you are using.

Table 15: Base Tab

Parameter	Choices	Notes
Instance Name	User defined	Indicate the DDR instance name. This name is the prefix for all DDR signals.
DDR Resource	None, DDR_0	Only one resource available.
Data Width	16, 32	Choose the DQ width. Default: 32 (16 for M361, M484, F529 packages)
Memory Density	2G, 3G, 4G, 6G, 8G, 12G, 16G	Choose the memory density per channel. Default: 4G
Physical Rank	1, 2	Default: 1
Memory Type	LPDDR4, LPDDR4x	Default: LPDDR4
Clock	CLKIN 0, CLKIN 1, CLKIN 2	Choose which PLL resource to use as the DDR clock. Available in J361, J484, and G529 packages only. **CLKIN 0**–PLL_TL0 **CLKIN 1**–PLL_TL1 **CLKIN 2**–PLL_TL2 (default)

Table 16: Advanced Options Tab (FPGA Settings)

Option	Choices	Notes
DQ Pull-Down Drive Strength (Ohm)	34.3, 40, 48, 60, 80, 120, 240	Default: 48
DQ Pull-Down ODT (Ohm)	34.3, 40, 48, 60, 80, 120, 240, High-Z	Default: 60
DQ Pull-Up Drive Strength (Ohm)	34.3, 40, 48, 60, 80, 120, 240	Default: 48
DQ Pull-Up ODT (Ohm)	34.3, 40, 48, 60, 80, 120, 240, High-Z	Default: High-Z
VREF Range Selection	Range 0, Range 1	Default: Range 0
VREF Setting (% of VDDQ)	**LPDDR4, Range 0:** 5.40 - 38.42 (step: 0.26) **LPDDR4, Range 1:** 11.90 - 48.222 (step: 0.286) **LPDDR4x, Range 0:** 11.60 - 49.70 (step: 0.3) **LPDDR4x, Range 1:** 21.20 - 59.30 (step: 0.3)	Default: LPDDR4, Range 0: 21.78 LPDDR4, Range 1: 29.918 LPDDR4x, Range 0: 30.5 LPDDR4x, Range 1: 40.1

Table 17: Advanced Options Tab (Memory Mode Register Settings)

Option	Choices	Notes
Burst Length	BL = 16 Sequential, BL = 16 or 32 Sequential, BL = 32 Sequential	Default: 16 Sequential
CA Bus Receiver On-Die-Termination for CS0/CS1	Disable, RZQ/1, RZQ/2, RZQ/3, RZQ/4, RZQ/5, RZQ/6	Default: Disable
DQ Bus Receiver On-Die-Termination for CS0/CS1	Disable, RZQ/1, RZQ/2, RZQ/3, RZQ/4, RZQ/5, RZQ/6	Default: Disable
Pull-Down Drive Strength (PDDS) for CS0/CS1	RFU, RZQ/1, RZQ/2, RZQ/3, RZQ/4, RZQ/5, RZQ/6	Default: RZQ/6
CA VREF Setting Range Selection	RANGE [0], RANGE [1]	Default: RANGE [1]
CA VREF Settings (% of VDD2)	**RANGE [0]:** 10 - 30 (step: 0.4) **RANGE [1]:** 22 - 42 (step: 0.4)	Default: RANGE [0]: 27.2 RANGE [1]: 27.2
DQ VREF Setting Range Selection	RANGE [0], RANGE [1]	Default: RANGE [1]
DQ VREF Settings (% of VDDQ)	**RANGE [0]:** 10 - 30 (step: 0.4) **RANGE [1]:** 22 - 42 (step: 0.4)	Default: RANGE [0]: 27.2 RANGE [1]: 27.2
Enable DBI Write	On or off	Enable data bus inversion (DBI) for write operation. When enabled, the controller automatically inverts the write data byte if there are 5 or more '1's in the data bus, and indicates the data is inverted by driving the DDR_DM signal high. Default: On
Enable DBI Read	On or off	Enable data bus inversion (DBI) for read operation. When enabled, the controller automatically inverts the read data byte if the DDR_DM signal is high. Default: On
CK ODT CS0/CS1 Enabled for Non-terminating Rank	Override Disabled, Override Enabled	Default: Override Disabled
CS ODT CS/CS1 Enabled for Non-terminating Rank	Override Disabled, Override Enabled	Default: Override Disabled
CA ODT CS/CS1 Termination Disable	Obeys ODT_CA Bond Pad, Disabled	Default: Override Obeys ODT_CA Bond Pad

Table 18: Advanced Options Tab (Memory Timing Settings)

Option	Choices	Notes
tCCD, CAS-to-CAS Delay (cycles)	8 - 31	Default: 8
tCCDMW, CAS-to-CAS Delay Masked Write (cycles)	32 - 63	Default: 32
tFAW, Four-Bank Activate Window (ns)	40 - 100	Default: 40
tPPD, Precharge to Precharge Delay (cycles)	4 - 7	Default: 4
tRAS, Row Active Time (ns)	42 - 100	Default: 42
tRCD, RAS-to-CAS Delay (ns)	18 - 100	Default: 18
tRPab, Row Precharge Time (All Banks) (ns)	21 - 100	Default: 21
tRPpb, Row Precharge Time (Single Bank) (ns)	18 - 100	Default: 18
tRRD, Active Bank-A to Active Bank-B (ns)	10 - 100	Default: 10
tRTP, Internal Read To Precharge Delay (ns)	7.5 - 100	Default: 7.5
tSR, Minimum Self Refresh Time (ns)	15 - 100	Default: 15
tWR, Write Recovery Time (ns)	18 - 60	Default: 18
tWTR, Write-To-Read Delay (ns)	10 - 60	Default: 10

Table 19: Config Controller Tab

Option	Choices	Notes
<description> Pin Name	User defined	Configuration and control pins. You can use the default names or specify your own.

Table 20: AXI 0 and AXI 1 Tabs

Parameter	Choices	Notes
Enable Target 0 Enable Target 1	On or off	Turn on to enable the AXI 0 interface. Turn on to enable the AXI 1 interface.
AXI Clock Input Pin Name	User defined	Specify the name of the AXI input clock pin.
Invert AXI Clock Input	On or off	Turn on to invert the AXI clock.
AXI Reset Pin Name	User defined	Specify the name of the AXI reset clock pin or use the default.
Read Address Channel tab Write Address Channel tab Write Response Channel tab Read Data Channel tab Write Data Channel tab	User defined	These tabs defines the AXI signal names for the channels. Efinix recommends that you use the default names.

Table 21: Controller Status Tab

Option	Choices	Notes
Invert Controller Status Clock Pin	On or off	Turn on if you want to invert the clock. Default: off
<*description*> Pin Name	User defined	Controller status pins. You can use the default names or specify your own.

Table 22: Pin Swizzling Tab

Option	Choices	Notes
Enable Package Pin Swapping	On or off	Turn on if you want to swap package pins. Default: off
DQ/DM Pin Swizzle Group*n*	–	Drag and drop pins in the DRAM column to swap DQ/DM pins. DQ Width = 16 : *n* is 0 and 1 DQ Width = 32 : *n* is 0, 1, 2 and 3
Address Pin Swizzle	–	Drag and drop pins in the DRAM column to swap address pins.

Supported DDR DRAM Devices

Titanium FPGAs support all JEDEC-compliant DDR DRAM devices (LPDDR4, LPDDR4x).

The following table lists devices that Efinix® have verified with Titanium FPGAs.

Table 23: DDR DRAM Devices Verified with Titanium FPGAs

Memory Type	Manufacturer	Part Number
LPDDR4/LPDDR4x	Micron	MT53E256M32D2
LPDDR4/LPDDR4x	Samsung	K4F6E3S4HM-MGCJ

Revision History

Table 24: Revision History

Date	Version	Description
February 2024	2.2	Updated Maximum Burst Length table in AXI section. (DOC-1689) Added in note regarding the number of clock cycles for the CFG_RESET to stay high in the figure Configuration Controller Signal Waveform. (DOC-1720)
February 2024	2.1	Added Maximum Burst Length table in AXI section. (DOC-1689) Updated Ti135, Ti200, and Ti375 in table Titanium FPGAs with LPDDR4/ LPDDR4x DRAM Support.
October 2023	2.0	Added note for Figure: Configuration Controller Signal Waveform. (DOC-1374) Added Pins Swizzling settings in the Efinity Interface Designer Settings. (DOC-1470)
July 2023	1.9	Corrected Maximum frequency (DDR controller) in Titanium DDR Features table. (DOC-1360) Corrected Read and Write operation example waveforms. (DOC-1366)
June 2023	1.8	Updated DDR_DM signal description and added Enable DBI options. (DOC-1322)
May 2023	1.7	Updated DDR PHY supported data rates. (DOC-1249)
April 2023	1.6	Updated DDR DRAM interface input clock to include description for J361, J484, and G529 packages. (DOC-1209) Removed DDR DRAM interface AXI width option and removed AXI Data to DRAM Device DQ Mapping Example with 256 bit AXI data width. (DOC-1210) Added verified DDR DRAM devices table. (DOC-1220)
February 2023	1.5	Updated LPDDR4 interface maximum data rate for M361, M484, and F529 packages. (DOC-1107)
January 2023	1.4	Updated J361 to DQ widths of x16, removed M484 and F529 from DQ widths x16 or x32 in topic Titanium FPGAs with LPDDR4/LPDDR4x DRAM Support. (DOC-1104)
December 2022	1.3	Updated DDR PHY support data rates in Features. (DOC-1025) Updated package information in DDR DRAM Widths Supported for Titanium FPGAs table of topic Titanium FPGAs with LPDDR4/LPDDR4x DRAM Support. Updated DDR DRAM Interface Performance table in Supported Frequencies and Configurations topic. Updated Base Tab table in DDR Interface Designer Settings. Updated title of the figures that show the connection between FPGA and DRAM device. Added in new figure Dual-Rank, x16 Interface. Added in new topic DDR Comparison. Updated Resets table. (DOC-1051)
November 2022	1.2	Updated Dual-Channel, Dual-Rank, x32 interface in the topic Supported Frequencies and Configurations. (DOC-979)

Date	Version	Description
October 2022	1.1	Updated Dual-Channel, Single-Rank, x32 interface and Dual-Channel, Dual-Rank, x32 interface in the topic Supported Frequencies and Configurations. (DOC-964) Topic title changed from Supported DDR DRAM Modules to Supported DDR DRAM Devices. Changed the word module to device. Updated the word module to device in document.
October 2022	1.0	Initial release.