DDR Hard Memory Controller-Calibration and Reset Core User Guide

UG-DDRAUTOCAL-RESET-v1.2
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Contents

Introduction

The DDR Hard Memory Controller-Calibration and Reset core helps you optimize timing and calibrate the Trion DDR controller using write leveling, read leveling, gate training, and reset sequencing (memory initialization). The core supports an automated calibration mode as well as calibration on demand, depending on your configuration.

Use the IP Manager to select IP, customize it, and generate files. The DDR Hard Memory Controller-Calibration and Reset core has an interactive wizard to help you set parameters. The wizard also has options to create a testbench and/or example design targeting an Efinix® development board.

Features

- Automatically performs leveling calibration for the DDR DRAM interface and external memory module
- Supports write leveling, read leveling, reset (memory initialization), and gate training calibration
- x16 and x32 DQ widths
- Verilog RTL and simulation testbench
- Includes an example design targeting the Trion® T120 BGA324 Development Board

Note: Refer to the **Trion DDR DRAM Block User Guide** for the list of supported DDR DRAM modules and the supported DDR PHY frequencies.

Device Support

Table 1: DDR Hard Memory Controller-Calibration and Reset Core Device Support

FPGA Family	Supported Device
Trion	T20 (BGA324 and BGA400 packages only), T35, T55, T85, T120
Titanium	–

Resource Utilization and Performance

Note: The resources and performance values provided are based on some of the supported FPGAs. These values are just guidance and change depending on the device resource utilization, design congestion, and user design.

Table 2: Trion Resource Utilization and Performance

FPGA	Logic Utilizations (LUTs)	Registers	Memory Blocks	Multipliers	Efinity® Version[1]
T120 BGA324 C4	1,706	780	18	0	2022.1

Release Notes

You can refer to the IP Core Release Notes for more information about the IP core changes. The IP Core Release Notes is available in the Efinity Downloads page under each Efinity software release version.

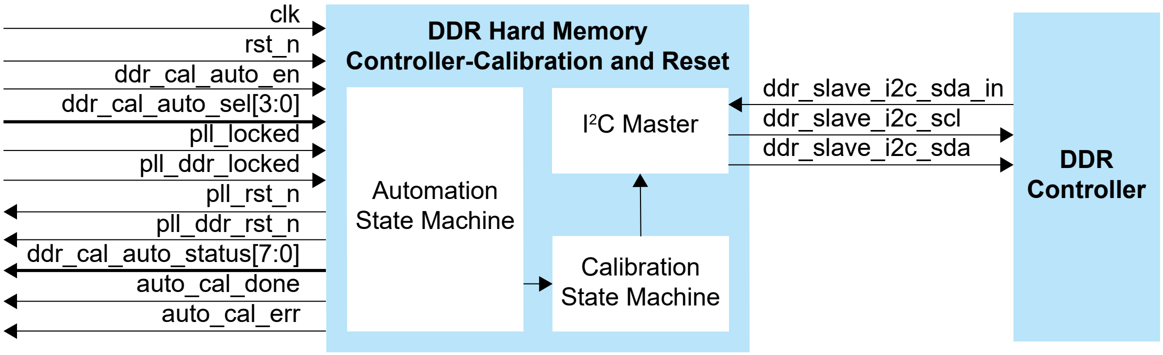
Note: You must be logged in to the Support Portal to view the IP Core Release Notes.

[1] Using Verilog HDL.

Functional Description

The core consists of an automation state machine, a calibration state machine, and an I^{2}C master.

Figure 1: DDR Hard Memory Controller-Calibration and Reset Core Block Diagram



Ports

Table 3: DDR Hard Memory Controller-Calibration and Reset Core Ports

Port	Direction	Description
rst_n	Input	Reset. Asynchronous, active-low reset signal that initializes all internal pointers and output registers.
clk	Input	System clock. This clock drives all signals in the core. Efinix recommends using a clock in the range of 2 to 8 MHz, which generates an I^{2}C clock of 100 to 400 KHz.
ddr_cal_auto_en	Input	Enable signal to start the automation state machine.
ddr_cal_auto_sel[3:0]	Input	Select signal to configure the calibration or reset mode you want to run. Bit 0: Read leveling Bit 1: Gate training Bit 2: Write leveling[2] Bit 3: Reset (Memory Initialization) You need to select the applicable option in the **Control Tab** of the DDR instance in the Interface Designer before instantiating the core. See Using the Core.
pll_locked	Input	PLL lock indicator from the generated system clock. Tie this signal to 1 (high) if the system clock is not from a PLL.
pll_ddr_locked	Input	PLL lock indicator from the DDR generated clock.
pll_rst_n	Output	PLL active-low reset to the generated system clock. Leave this port unconnected if the system clock is not from a PLL.
pll_ddr_rst_n	Output	PLL active-low reset to the generated DDR clock.

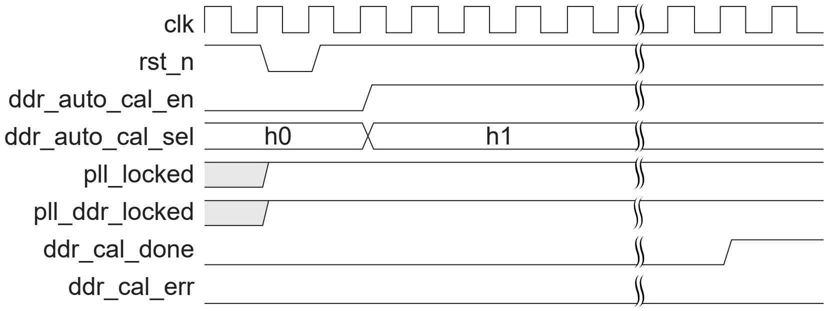
[2] Disable the write leveling (Bit 2 = 0) if you do not use fly-by topology in your board design.

Port	Direction	Description
ddr_cal_auto_status[7:0]	Output	Optional. Status signal for debugging. Bit 0: Indicates read leveling calibration is running. Bit 1: Indicate gate training calibration is running. Bit 2: Indicate write leveling calibration is running. Bit 3: Indicate reset (memory initialization) is running. Bit 4: Base sequence active signal from the calibration state machine. Bit 5: Main loop active signal from the calibration state machine. Bit 6: Sub-loop 1 active signal from the calibration state machine. Bit 7: Sub-loop 2 active signal from the calibration state machine.
auto_cal_done	Output	Optional. Indicates that the automation state machine successfully completed calibration.
auto_cal_err	Output	Optional. Indicates that the automation state machine started with an invalid ddr_cal_auto_sel setting.
ddr_slave_i2c_scl	Output	I^{2}C clock to the DDR controller.
ddr_slave_i2c_sda	Output	I^{2}C data to the DDR controller.
ddr_slave_i2c_sda_in	Input	I^{2}C enable to the DDR controller.

Automation State Machine

This state machine controls the calibration process. When you assert `ddr_cal_auto_en`, the state machine starts. The core uses the value in `ddr_cal_auto_sel` to choose which calibration or reset mode to run. For example, if `ddr_cal_auto_sel` is set to `4'b0101`, the state machine performs write leveling calibration and then read leveling calibration. The core gives highest priority to reset (memory initialization), followed by write leveling, then gate leveling, and lastly read leveling.

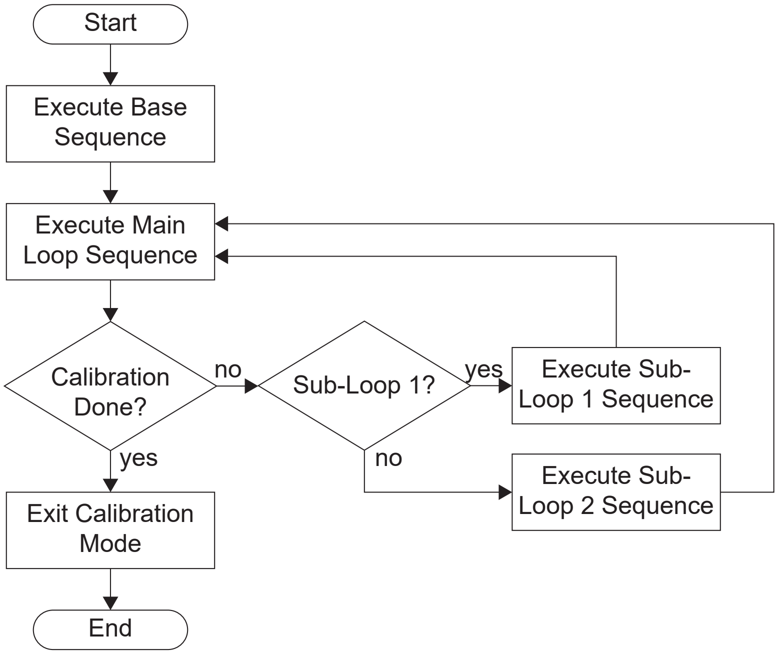
Figure 2: DDR Hard Memory Controller-Calibration and Reset Operation



Calibration State Machine

Each calibration mode executes different a programming sequence or setting. The calibration state machine ensures that the core retrieves the correct instructions from the ROM and send them to the I^2C master according to calibration mode you choose. Instructions continue executing in a loop until the DDR controller indicates that calibration is complete. Therefore, the calibration state machine consists of one base sequence state and 3 loop states, providing flexibility to change the programming execution according to the needs of different calibration modes.

Figure 3: Simplified Calibration State Machine Flow



I^2C Master

A simple I^2C master provides functions including read, write, polling, and masked write with returned data. The I^2C slave address is set to `8'h82`, and only communicates with the DDR controller. The I^2C master receives instructions from the calibration state machine and performs I^2C functions by extracting the most significant 4 bits of the total 108 instruction bits.

Table 4: I^2C Instruction Description

107:100	99:96	95:64	63:32	31:0
Function	Number of instructions	APB mask	APB data	APB address

Table 5: I^2C Functions

Bit	107	106	105	104	103	102
Function	Write	Read	Poll	Read masked write	Reserved	Save returned data

Using the Core

Before generating the DDR Hard Memory Controller-Calibration and Reset core in the Efinity IP Manager, you must create a DDR block in the Interface Designer and set the settings in the **Block Editor**. After creating the DDR block, click the **Generate Efinity Constraints Files** button. Then, instantiate the core with the `ddr_cal_auto_sel[3:0]` input driven accordingly.

Note: Only one DDR block can be added in the Interface Designer for each Trion FPGA.

Examples:

Operation	Interface Designer Block Editor (Control Tab)	ddr_cal_auto_sel[3:0]	Note
Calibration and Reset	Enable Calibration and Reset	ddr_cal_auto_sel[3]=1 ddr_cal_auto_sel[2:0] set as per required calibration	The Interface Designer **Block Editor** (Control Tab) enables the Master Reset Pin. You need to toggle from low to high, before using the core. You cannot disable the reset (memory initialization) in this operation option.
Calibration Only	Enable Calibration	ddr_cal_auto_sel[3]=0 ddr_cal_auto_sel[2:0] set as per required calibration	

Important: For the DDR Hard Memory Controller-Calibration and Reset core to properly propagate settings from the Interface Designer, the project directory name must match the project file names (**<project>.xml** and **<project>.peri.xml**).

You need to regenerate the DDR Hard Memory Controller-Calibration and Reset core each time you change the settings in the Interface Designer.

Note: You should only trigger reset and recalibration after any ongoing calibration is complete (`auto_cal_done` signal is asserted).

IP Manager

The Efinity® IP Manager is an interactive wizard that helps you customize and generate Efinix® IP cores. The IP Manager performs validation checks on the parameters you set to ensure that your selections are valid. When you generate the IP core, you can optionally generate an example design targeting an Efinix development board and/or a testbench. This wizard is helpful in situations in which you use several IP cores, multiple instances of an IP core with different parameters, or the same IP core for different projects.

Note: Not all Efinix IP cores include an example design or a testbench.

Generating the DDR Hard Memory Controller-Calibration and Reset Core with the IP Manager

The following steps explain how to customize an IP core with the IP Configuration wizard.

1. Open the IP Catalog.
2. Choose **Memory Controllers > DDR Hard Memory Controller-Calibration and Reset** core and click **Next**. The **IP Configuration** wizard opens.
3. Enter the module name in the **Module Name** box.

   Note: You cannot generate the core without a module name.

4. Customize the IP core using the options shown in the wizard. For detailed information on the options, refer to the *Customizing the DDR Hard Memory Controller-Calibration and Reset* section.
5. (Optional) In the **Deliverables** tab, specify whether to generate an IP core example design targeting an Efinix® development board and/or testbench. These options are turned on by default.
6. (Optional) In the **Summary** tab, review your selections.
7. Click **Generate** to generate the IP core and other selected deliverables.
8. In the **Review configuration generation** dialog box, click **Generate**. The Console in the **Summary** tab shows the generation status.

   Note: You can disable the **Review configuration generation** dialog box by turning off the **Show Confirmation Box** option in the wizard.

9. When generation finishes, the wizard displays the **Generation Success** dialog box. Click **OK** to close the wizard.

The wizard adds the IP to your project and displays it under **IP** in the Project pane.

Generated Files

The IP Manager generates these files and directories:

- **<module name>_define.vh**—Contains the customized parameters.
- **<module name>_tmpl.v**—Verilog HDL instantiation template.
- **<module name>_tmpl.vhd**—VHDL instantiation template.
- **<module name>.v**—IP source code.
- **settings.json**—Configuration file.
- **<kit name>_devkit**—Has generated RTL, example design, and Efinity® project targeting a specific development board.
- **Testbench**—Contains generated RTL and testbench files.

Customizing the DDR Hard Memory Controller-Calibration and Reset

The core has parameters so you can customize its function. You set the parameters in the General tab of the core's IP Configuration window.

Table 6: DDR Hard Memory Controller-Calibration and Reset Core Parameters

Parameters must be the same as the settings you set for the DDR block in Interface Designer. See **Using the Core** on page 8.

Parameter	Options	Description
DDR Memory Type	LPDDR3, DDR3/ DDR3L, LPDDR2	Set the DDR memory module type. Default: LPDDR3
DDR Memory Width	32-bits, 16-bits	Set the DDR memory width. Default: 16-bits
Gate Leveling Initial Coarse Delay	1 - 5	Set the gate leveling initial coarse delay. Minimum value = roundup (t_{DQSCK}[3] + board delay[4]) / (0.5 * DDR clk period)

[3] t_{DQSCK} = CLK to DQS delay

[4] Board delay = CLK board delay from PHY to the memory + DQS board delay from memory to PHY

DDR Hard Memory Controller-Calibration and Reset Example Design

You can choose to generate the example design when generating the core in the IP Manager Configuration window. Compile the example design project and download the **.hex** or **.bit** file to your board.

Important: Efinix tested the example design generated with the default parameter options only.

The example design targets the Trion® T120 BGA324 Development Board. It implements a memory checker that writes data into the DDR DRAM module on the board and then performs a read operation. The design compares the returned data to the sent data and displays the results using the board's LEDs. You can turn calibration on or off to see how the DDR DRAM module works with and without calibration. The design has two clocks feeding the PLLs, 50 MHz (`pll_ddr_refclk`) and 10 MHz (`pll_refclk`).

Figure 4: DDR Hard Memory Controller-Calibration and Reset Core Example Design

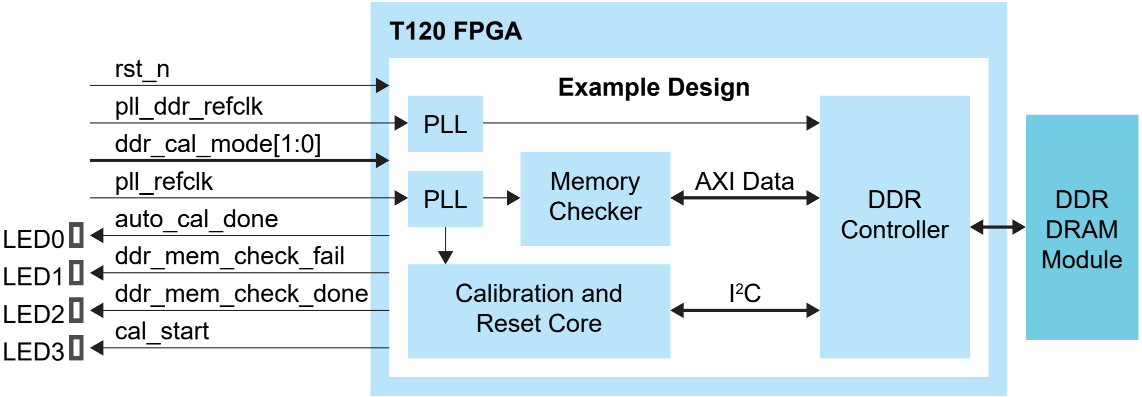


Table 7: Example Design Implementation

FPGA	Logic Utilizations (LUTs)	Registers	Memory Blocks	Multipliers	Efinity® Version[5]
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[5] Using Verilog HDL.

Control the Calibration Mode with DIP Switches

The design lets you switch between write levelling, gate training, and read leveling calibration operations using DIP switches on SW5.

Table 8: DIP Switch Settings

Calibration Operation	SW5 DIP1	SW5 DIP0
Write leveling	On	On
Gate training	On	Off
Read leveling	Off	On
All calibration operations	Off	Off

Using the Example Design

As the example design runs, the user LEDs on the Trion® T120 BGA324 Development Board show the calibration results.

- Three seconds after you reset the board, LED3 turns on to indicate the design is operating. If bypass mode is turned off, calibration begins. If bypass mode is turned on, the design skips calibration.
- When calibration completes (or in bypass mode), LED0 turns on to indicate the memory checker is operating.
- If the memory checker successfully writes and then reads the memory, it turns on LED2.
- LED1 turns on when the write and read data do not match.

First, run the design with bypass mode turned off (default). LED3 turns on, then LED0, and then LED2.

Next, set the `CALIBRATION_BYPASS` parameter to 1, recompile, and download the new bitstream to the board. When you run the design, both LED0 and LED3 are off indicating calibration does not run. After memory check is done, LED2 turns on. If there is a write and read data mismatch, LED1 turns on.

Revision History

Table 9: Revision History

Date	Version	Description
July 2023	1.2	Added Gate Levelling Initial Coarse Delay parameter in IP manager. Added Device Support and release notes sections. (DOC-1234)
February 2023	1.1	Added note about the resource and performance values in the resource and utilization table are for guidance only.
August 2022	1.0	Initial release.