



T35 Data Sheet

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Introduction

The T35 FPGA features the high-density, low-power Efinix® Quantum® architecture wrapped with an I/O interface for easy integration. With a high I/O to logic ratio and differential I/O support, T35 FPGAs supports a variety of applications that need wide I/O connectivity. The T35 also includes a MIPI D-PHY with a built-in, royalty-free CSI-2 controller, which is the most popular camera interface used in the mobile industry. Additionally, T35 FPGAs support a DDR3, LPDDR3, LPDDR2 PHY with memory controller hard IP that provides faster access to data stored in memory. The carefully tailored combination of core resources and I/O provides enhanced capability for applications such as embedded vision, voice and gesture recognition, intelligent sensor hubs, power management, and LED drivers.

Features

- High-density, low-power Quantum® architecture
- Built on SMIC 40 nm process
- FPGA interface blocks
 - GPIO
 - PLL
 - LVDS 800 Mbps per lane with up to 20 TX pairs and 26 RX pairs
 - MIPI DPHY with CSI-2 controller hard IP, 1.5 Gbps per lane
 - DDR3, DDR3L, LPDDR3, LPDDR2 x16 PHY (supporting x16 DQ widths) with memory controller hard IP, up to 1066 Mbps
- Programmable high-performance I/O
 - Supports 1.8, 2.5, and 3.3 V single-ended I/O standards and interfaces
- Flexible on-chip clocking
 - Low-skew global clock signals can be driven from off-chip external clock signals or PLL synthesized clock signals
 - PLL support
- Flexible device configuration
 - Standard SPI interface (active, passive, and daisy chain)
 - JTAG interface
- Fully supported by the Efinity® software, an RTL-to-bitstream compiler

Table 1: T35 FPGA Resources

| LEs ⁽¹⁾ | Global Clock Networks | Global Control Networks | Embedded Memory (kbits) | Embedded Memory Blocks (5 Kbits) | Embedded Multipliers |
|--------------------|-----------------------|-------------------------|-------------------------|----------------------------------|----------------------|
| 31,680 | Up to 16 | Up to 16 | 1,475 | 288 | 120 |

⁽¹⁾ Logic capacity in equivalent LE counts.

Table 2: T35 Package-Dependent Resources

| Resource | BGA256 | BGA324 | BGA400 |
|---|----------------------------|-------------------------------|-------------------------------|
| Available GPIO ⁽²⁾ | 191 | 130 | 230 |
| Global clocks from GPIO pins | 16 | 5 | 16 |
| Global controls from GPIO pins | 16 | 5 | 16 |
| PLLs | 7 | 7 | 7 |
| LVDS | 10 TX pairs 18 RX pairs | 20 TX pairs 26 RX pairs | 20 TX pairs 26 RX pairs |
| MIPI DPHY with CSI-2 controller (4 data lanes, 1 clock lane) | - | 2 TX blocks 2 RX blocks | - |
| DDR3, DDR3L, LPDDR3, LPDDR2 PHY with memory controller | - | 1 block (x8 or x16 DQ widths) | 1 block (x8 or x16 DQ widths) |



Learn more: Refer to the [Trion Packaging User Guide](#) for the package outlines and markings.

Available Package Options

Table 3: Available Packages

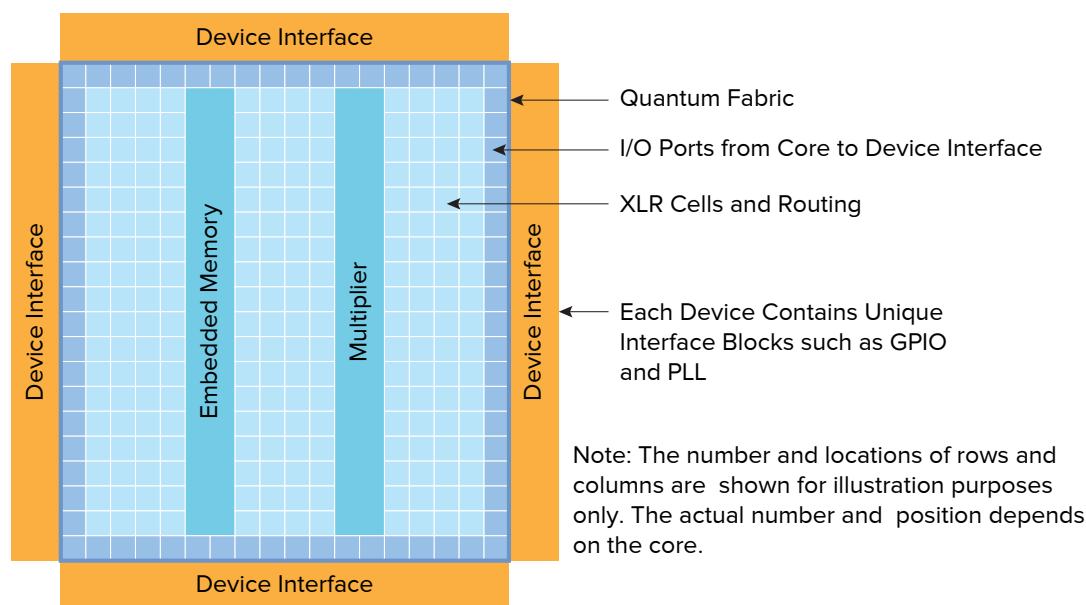
| Package | Dimensions (mm x mm) | Pitch (mm) |
|---------------|----------------------|------------|
| 256-ball FBGA | 13 x 13 | 0.8 |
| 324-ball FBGA | 12 x 12 | 0.65 |
| 400-ball FBGA | 16 x 16 | 0.8 |

⁽²⁾ The LVDS I/O pins are dual-purpose. The full number of GPIO are available when all LVDS I/O pins are in GPIO mode. GPIO and LVDS as GPIO supports different features. See [Table 9: Supported Features for GPIO and LVDS as GPIO](#) on page 13.

Device Core Functional Description

T35 FPGAs feature an eXchangeable Logic and Routing (XLR) cell that Efinix has optimized for a variety of applications. Trion® FPGAs contain three building blocks constructed from XLR cells: logic elements, embedded memory blocks, and multipliers. Each FPGA in the Trion® family has a custom number of building blocks to fit specific application needs. As shown in the following figure, the FPGA includes I/O ports on all four sides, as well as columns of XLR cells, memory, and multipliers. A control block within the FPGA handles configuration.

Figure 1: T35 FPGA Block Diagram



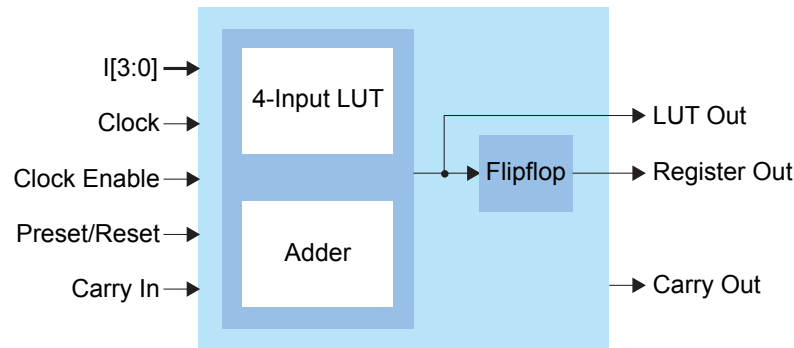
XLR Cell

The eXchangeable Logic and Routing (XLR) cell is the basic building block of the Quantum® architecture. The Efinix XLR cell combines logic and routing and supports both functions interchangeably. This unique innovation greatly enhances the transistor flexibility and utilization rate, thereby reducing transistor counts and silicon area significantly.

Logic Cell

The logic cell comprises a 4-input LUT or a full adder plus a register (flipflop). You can program each LUT as any combinational logic function with four inputs. You can configure multiple logic cells to implement arithmetic functions such as adders, subtractors, and counters.

Figure 2: Logic Cell Block Diagram



Embedded Memory

The core has 5-kbit high-speed, synchronous, embedded SRAM memory blocks. Memory blocks can operate as single-port RAM, simple dual-port RAM, true dual-port RAM, FIFOs, or ROM. You can initialize the memory content during configuration. The Efinity[®] software includes a memory cascading feature to connect multiple blocks automatically to form a larger array. This feature enables you to instantiate deeper or wider memory modules.



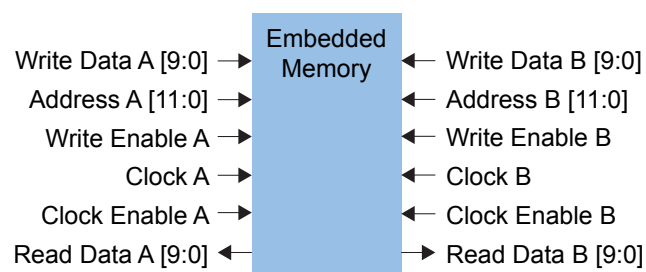
Note: The block RAM content is random and undefined if it is not initialized.

The memory read and write ports have the following modes for addressing the memory (depth x width):

| | | | |
|----------|----------|----------|----------|
| 256 x 16 | 1024 x 4 | 4096 x 1 | 512 x 10 |
| 512 x 8 | 2048 x 2 | 256 x 20 | 1024 x 5 |

The read and write ports support independently configured data widths.

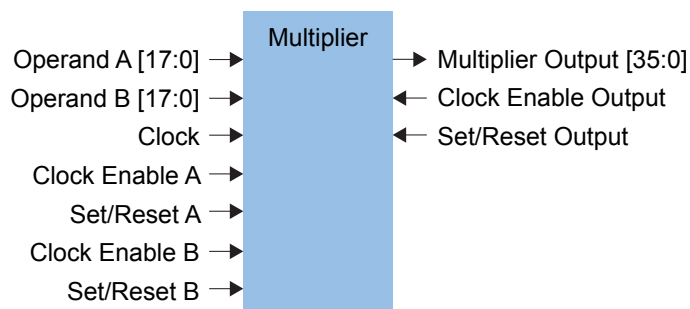
Figure 3: Embedded Memory Block Diagram (True Dual-Port Mode)



Multipliers

The FPGA has high-performance multipliers that support 18 x 18 fixed-point multiplication. Each multiplier takes two signed 18-bit input operands and generates a signed 36-bit output product. The multiplier has optional registers on the input and output ports.

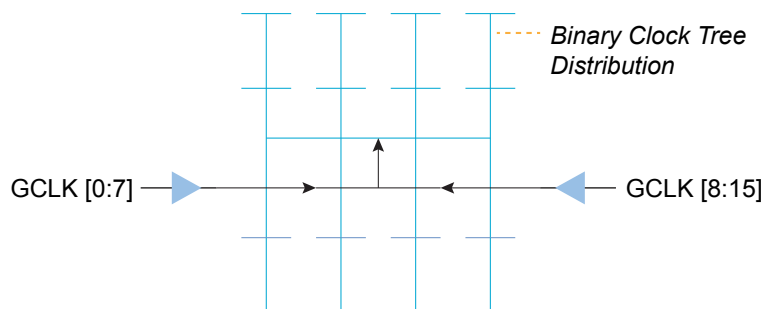
Figure 4: Multiplier Block Diagram



Global Clock Network

The global clock networks are balanced clock trees that feed all FPGA modules. Each network has dedicated clock-enable logic to save power by disabling the clock tree at the root. The logic dynamically enables/disables the network and guarantees no glitches at the output.

Figure 5: Global Clock Network



Clock and Control Distribution Network

The global clock network is distributed through the device to provide clocking for the core's LEs, memory, multipliers, and I/O blocks. Designers can access the T35 global clock network using the global clock GPIO pins, PLL outputs, and core-generated clocks. Similarly, the T35 has GPIO pins (the number varies by package) that the designer can configure as control inputs to access the high-fanout network connected to the LE's set, reset, and clock enable signals.



Learn more: Refer to the [T35 Pinout](#) for information on the location and names of these pins.

Global Clock Location

Table 4: Left Clock Input from GPIO Pins

| Function Name | Resource Name | GCLK[0] | GCLK[1] | GCLK[2] | GCLK[3] | GCLK[4] | GCLK[5] | GCLK[6] | GCLK[7] |
|---------------|---------------|---------|---------|---------|---------|---------|---------|---------|---------|
| CLK0 | GPIOL_66 | ✓ | - | - | - | ✓ | - | - | - |
| CLK1 | GPIOL_67 | - | ✓ | - | - | - | ✓ | - | - |
| CLK2 | GPIOL_68 | - | - | ✓ | - | - | - | ✓ | - |
| CLK3 | GPIOL_69 | - | - | - | ✓ | - | - | - | ✓ |
| CLK4 | GPIOL_70 | ✓ | - | - | - | ✓ | - | - | - |
| CLK5 | GPIOL_71 | - | ✓ | - | - | - | ✓ | - | - |
| CLK6 | GPIOL_72 | - | - | ✓ | - | - | - | ✓ | - |
| CLK7 | GPIOL_73 | - | - | - | ✓ | - | - | - | ✓ |

Table 5: Left Clock from PLL OUTCLK Signal

| PLL Reference | CLKOUT | GCLK[0] | GCLK[1] | GCLK[2] | GCLK[3] | GCLK[4] | GCLK[5] | GCLK[6] | GCLK[7] |
|---------------|---------|---------|---------|---------|---------|---------|---------|---------|---------|
| PLL_BL0 | CLKOUT0 | ✓ | - | - | ✓ | - | - | - | ✓ |
| | CLKOUT1 | - | ✓ | - | - | ✓ | - | ✓ | - |
| | CLKOUT2 | - | - | ✓ | - | - | ✓ | - | - |

Table 6: Right Clock Input from GPIO Pins

| Function Name | Resource Name | GCLK[8] | GCLK[9] | GCLK[10] | GCLK[11] | GCLK[12] | GCLK[13] | GCLK[14] | GCLK[15] |
|---------------|---------------|---------|---------|----------|----------|----------|----------|----------|----------|
| CLK0 | GPIOR_133 | ✓ | - | - | - | - | - | - | - |
| CLK1 | GPIOR_132 | - | ✓ | - | - | - | - | - | - |
| CLK2 | GPIOR_131 | - | - | ✓ | - | - | - | - | - |
| CLK3 | GPIOR_130 | - | - | - | ✓ | - | - | - | - |
| CLK4 | GPIOR_129 | - | - | - | - | ✓ | - | - | - |
| CLK5 | GPIOR_128 | - | - | - | - | - | ✓ | - | - |
| CLK6 | GPIOR_127 | - | - | - | - | - | - | ✓ | - |
| CLK7 | GPIOR_126 | - | - | - | - | - | - | - | ✓ |

Table 7: Right Clock from PLL OUTCLK Signal

| PLL Reference | CLKOUT | GCLK[8] | GCLK[9] | GCLK[10] | GCLK[11] | GCLK[12] | GCLK[13] | GCLK[14] | GCLK[15] |
|---------------|---------|---------|---------|----------|----------|----------|----------|----------|----------|
| PLL_TR0 | CLKOUT0 | ✓ | - | - | - | - | - | ✓ | - |
| | CLKOUT1 | - | ✓ | ✓ | - | - | - | - | - |
| | CLKOUT2 | - | ✓ | ✓ | - | - | - | - | - |
| PLL_TR1 | CLKOUT0 | ✓ | - | - | ✓ | - | - | - | - |
| | CLKOUT1 | - | - | - | - | ✓ | ✓ | - | - |
| | CLKOUT2 | - | - | - | - | ✓ | ✓ | - | - |
| PLL_TR2 | CLKOUT0 | ✓ | - | - | - | - | - | - | ✓ |
| | CLKOUT1 | - | ✓ | ✓ | - | - | - | - | - |
| | CLKOUT2 | - | ✓ | ✓ | - | - | - | - | - |
| PLL_BR0 | CLKOUT0 | - | - | - | ✓ | - | - | - | ✓ |
| | CLKOUT1 | - | - | - | - | ✓ | ✓ | - | - |
| | CLKOUT2 | - | - | - | - | ✓ | ✓ | - | - |
| PLL_BR1 | CLKOUT0 | - | - | ✓ | - | - | - | ✓ | - |
| | CLKOUT1 | - | - | - | ✓ | ✓ | - | - | - |
| | CLKOUT2 | - | - | - | ✓ | ✓ | - | - | - |
| PLL_BR2 | CLKOUT0 | - | - | - | - | - | ✓ | - | - |
| | CLKOUT1 | - | ✓ | - | - | - | - | ✓ | - |
| | CLKOUT2 | - | - | - | - | - | - | - | ✓ |

Device Interface Functional Description

The device interface wraps the core and routes signals between the core and the device I/O pads through a signal interface. Because they use the flexible Quantum[®] architecture, devices in the Trion[®] family support a variety of interfaces to meet the needs of different applications.



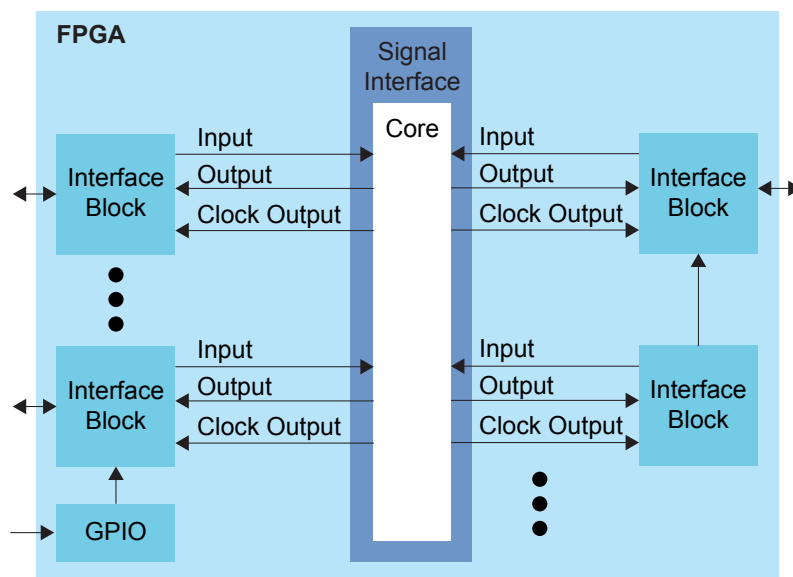
Learn more: The following sections describe the available device interface features in T35 FPGAs. Refer to the [Trion[®] Interfaces User Guide](#) for details on the Efinity[®] Interface Designer settings.

Interface Block Connectivity

The FPGA core fabric connects to the interface blocks through a signal interface. The interface blocks then connect to the package pins. The core connects to the interface blocks using three types of signals:

- *Input*—Input data or clock to the FPGA core
- *Output*—Output from the FPGA core
- *Clock output*—Clock signal from the core clock tree

Figure 6: Interface Block and Core Connectivity



GPIO blocks are a special case because they can operate in several modes. For example, in alternate mode the GPIO signal can bypass the signal interface and directly feed another interface block. So a GPIO configured as an alternate input can be used as a PLL reference clock without going through the signal interface to the core.

When designing for Trion[®] FPGAs, you create an RTL design for the core and also configure the interface blocks. From the perspective of the core, outputs from the core are inputs to the interface block and inputs to the core are outputs from the interface block.

The Efinity netlist always shows signals from the perspective of the core, so some signals do not appear in the netlist:

- GPIO used as reference clocks are not present in the RTL design, they are only visible in the interface block configuration of the Efinity[®] Interface Designer.

- The FPGA clock tree is connected to the interface blocks directly. Therefore, clock outputs from the core to the interface are not present in the RTL design, they are only part of the interface configuration (this includes GPIO configured as output clocks).

The following sections describe the different types of interface blocks. Signals and block diagrams are shown from the perspective of the interface, not the core.

General-Purpose I/O Logic and Buffer

The GPIO support the 3.3 V LVTTL and 1.8 V, 2.5 V, and 3.3 V LVCMOS I/O standards. The GPIOs are grouped into banks. Each bank has its own VCCIO that sets the bank voltage for the I/O standard.

Each GPIO consists of I/O logic and an I/O buffer. I/O logic connects the core logic to the I/O buffers. I/O buffers are located at the periphery of the device.

The I/O logic comprises three register types:

- *Input*—Capture interface signals from the I/O before being transferred to the core logic
- *Output*—Register signals from the core logic before being transferred to the I/O buffers
- *Output enable*—Enable and disable the I/O buffers when I/O used as output

Table 8: GPIO Modes

| GPIO Mode | Description |
|---------------|--|
| Input | Only the input path is enabled; optionally registered. If registered, the input path uses the input clock to control the registers (positively or negatively triggered). Select the alternate input path to drive the alternate function of the GPIO. The alternate path cannot be registered. In DDIO mode, two registers sample the data on the positive and negative edges of the input clock, creating two data streams. |
| Output | Only the output path is enabled; optionally registered. If registered, the output path uses the output clock to control the registers (positively or negatively triggered). The output register can be inverted. In DDIO mode, two registers capture the data on the positive and negative edges of the output clock, multiplexing them into one data stream. |
| Bidirectional | The input, output, and OE paths are enabled; optionally registered. If registered, the input clock controls the input register, the output clock controls the output and OE registers. All registers can be positively or negatively triggered. Additionally, the input and output paths can be registered independently. The output register can be inverted. |
| Clock output | Clock output path is enabled. |

Table 9: Supported Features for GPIO and LVDS as GPIO

LVDS as GPIO are LVDS pins that act as GPIOs instead of the LVDS function.

| Package | GPIO | LVDS as GPIO |
|----------------------------|---|---|
| BGA256 BGA324 BGA400 | DDIO Schmitt Trigger Variable Drive Strength Pull-up Pull-down Slew Rate | Variable Drive Strength Pull-up Slew Rate |

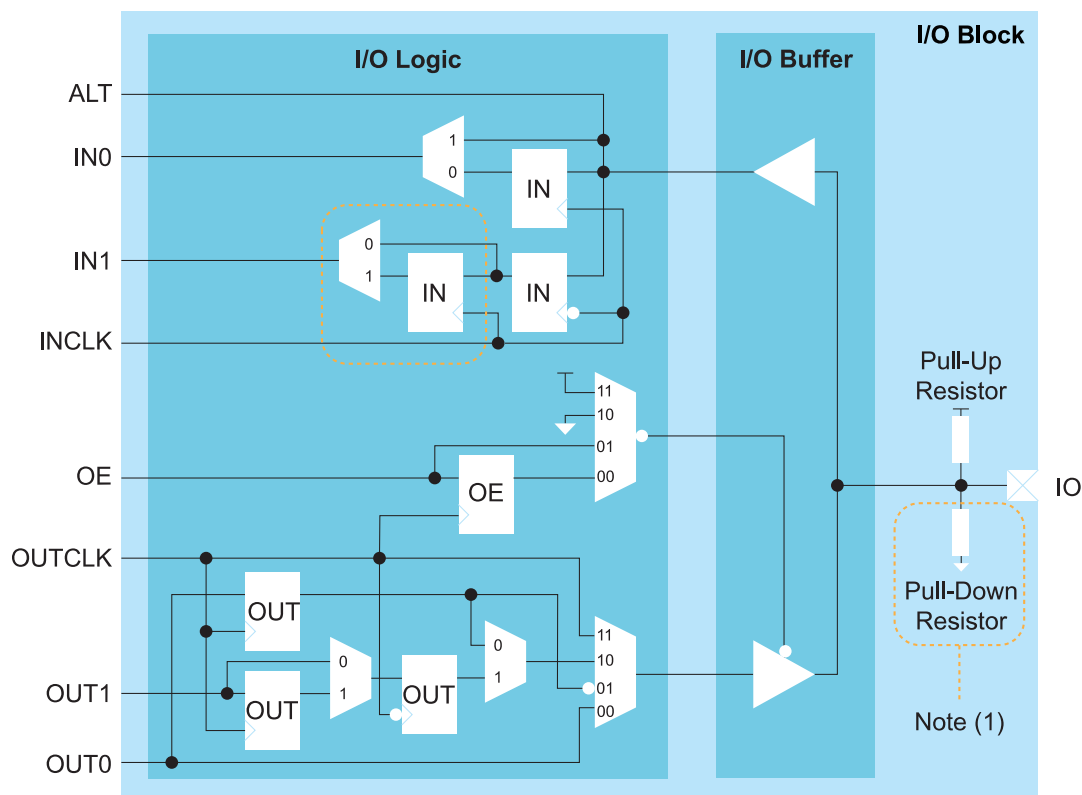


Important: Efinix® recommends that you limit the number of LVDS as GPIO set as output and bidirectional to 14 per bank to avoid switching noise. The Efinity software issues a warning if you exceed the recommended limit.

During configuration, all GPIO pins excluding LVDS as GPIO are configured in weak pull-up mode. The LVDS as GPIO pins are tri-stated without a pull-up or pull-down resistor.

During user mode, unused GPIO pins are tri-stated and configured in weak pull-up mode. You can change the default mode to weak pull-down in the Interface Designer. No glitches if the GPIO is configured as weak pull-up in user mode

Complex I/O Buffer

Figure 7: I/O Interface Block

1. GPIO pins using LVDS resources do not have a pull-down resistor.



Note: LVDS as GPIO do not have double data I/O (DDIO).

Table 10: GPIO Signals (Interface to FPGA Fabric)

| Signal | Direction | Description |
|----------|-----------|--|
| IN[1:0] | Output | Input data from the GPIO pad to the core fabric. IN0 is the normal input to the core. In DDIO mode, IN0 is the data captured on the positive clock edge (HI pin name in the Interface Designer) and IN1 is the data captured on the negative clock edge (LO pin name in the Interface Designer). |
| ALT | Output | Alternative input connection (in the Interface Designer, Register Option is none). Alternative connections are GCLK, GCTRL, PLL_CLKIN, and MIPI_CLKIN. ⁽³⁾ |
| OUT[1:0] | Input | Output data to GPIO pad from the core fabric. OUT0 is the normal output from the core. In DDIO mode, OUT0 is the data captured on the positive clock edge (HI pin name in the Interface Designer) and OUT1 is the data captured on the negative clock edge (LO pin name in the Interface Designer). |
| OE | Input | Output enable from core fabric to the I/O block. Can be registered. |
| OUTCLK | Input | Core clock that controls the output and OE registers. This clock is not visible in the user netlist. |
| INCLK | Input | Core clock that controls the input registers. This clock is not visible in the user netlist. |

Table 11: GPIO Pads

| Signal | Direction | Description |
|--------|---------------|-------------|
| IO | Bidirectional | GPIO pad. |

⁽³⁾ MIPI_CLKIN is only available in packages that support MIPI.

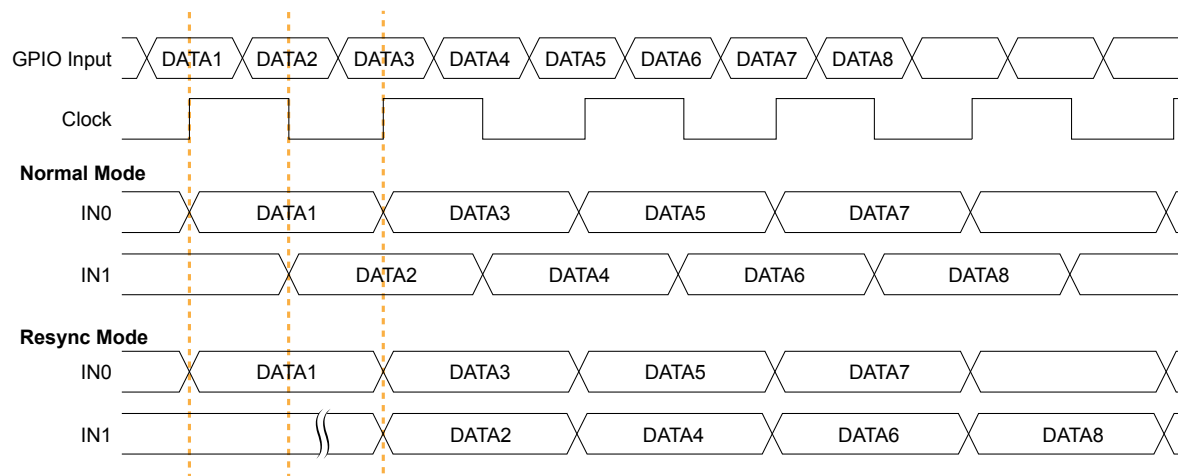
Double-Data I/O

T35 FPGAs support double data I/O (DDIO) on input and output registers. In this mode, the DDIO register captures data on both positive and negative clock edges. The core receives 2 bit wide data from the interface.

In normal mode, the interface receives or sends data directly to or from the core on the positive and negative clock edges. In resync mode, the interface resynchronizes the data to pass both signals on the positive clock edge only.

LVDS as GPIO (that is, single ended I/O) do not support DDIO functionality.

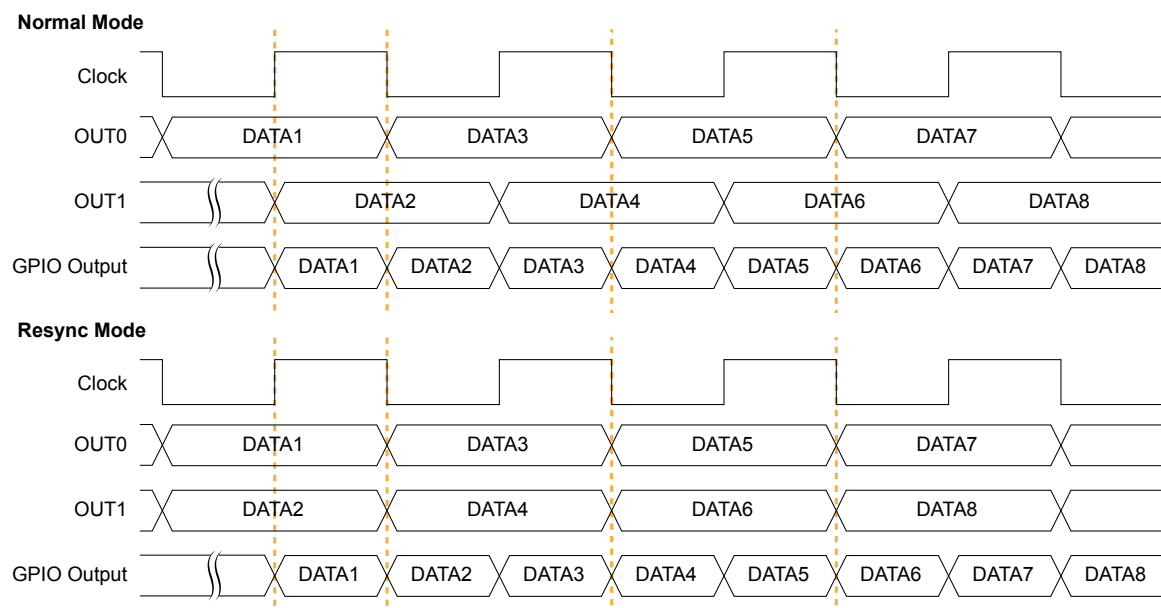
Figure 8: DDIO Input Timing Waveform



In resync mode, the IN1 data captured on the falling clock edge is delayed one half clock cycle.

In the Interface Designer, IN0 is the HI pin name and IN1 is the LO pin name.

Figure 9: DDIO Output Timing Waveform



In the Interface Designer, OUT0 is the HI pin name and OUT1 is the LO pin name.

I/O Banks

Efinix FPGAs have input/output (I/O) banks for general-purpose usage. Each I/O bank has independent power pins. The number and voltages supported vary by FPGA and package.

The number of banks and the voltages they support vary by package.

Some I/O banks are merged at the package level by sharing VCCIO pins. Merged banks have underscores (_) between banks in the name (e.g., 1B_1C means 1B and 1C are connected).

Table 12: I/O Banks by Package

| Package | I/O Banks | Voltage (V) | Banks with DDIO Support | Merged Banks |
|---------|---|---------------|-------------------------|---------------------------------|
| BGA256 | 1A - 1E, 2A, 2B, 3C, 4A, 4B, TR, BR | 1.8, 2.5, 3.3 | 1A - 1E, 3C, TR, BR | 1A_1B, 2A_2B_2C, 3C_TR_BR |
| BGA324 | 1A - 1E, 2A - 2C, 3A - 3C, 4A, 4B, TR, BR | 1.8, 2.5, 3.3 | 1A - 1E, 3C, TR, BR | 1B_1C, 1D_1E, 3C_TR_BR |
| BGA400 | 1A - 1E, 2A - 2C, 3C, 4A, 4B, TR, BR | 1.8, 2.5, 3.3 | 1A - 1E, 3C, TR, BR | 3C_TR |



Learn more: Refer to the [T35 Pinout](#) for information on the I/O bank assignments.

PLL

The T35 has 7 available PLLs to synthesize clock frequencies.



Note: You can cascade the PLLs in T35 FPGAs. To avoid the PLL losing lock, Efinix recommends that you do not cascade more than two PLLs.

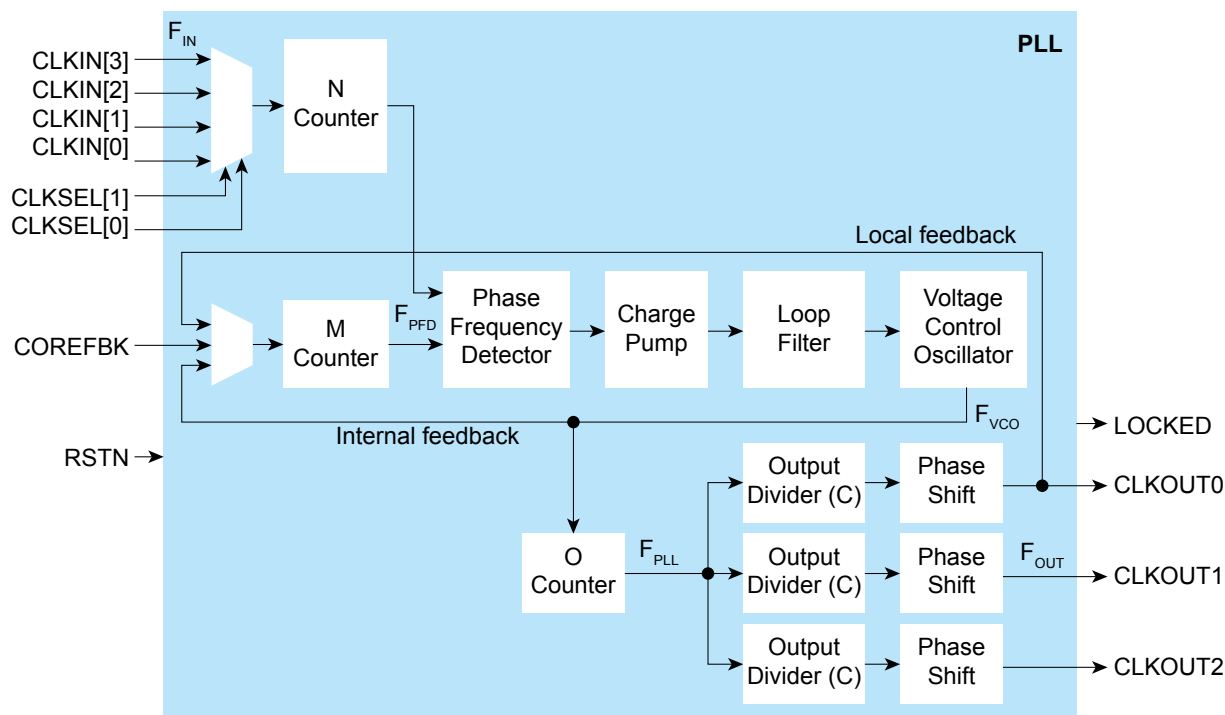
You can use the PLL to compensate for clock skew/delay via external or internal feedback to meet timing requirements in advanced application. The PLL reference clock has up to four sources. You can dynamically select the PLL reference clock with the `CLKSEL` port. (Hold the PLL in reset when dynamically selecting the reference clock source.)

The PLL consists of a pre-divider counter (N counter), a feedback multiplier counter (M counter), a post-divider counter (O counter), and output divider.



Note: Refer to [T35 Interface Floorplan](#) on page 70 for the location of the PLLs on the die. Refer to [Table 98: General Pinouts](#) on page 66 for the PLL reference clock resource assignment.

Figure 10: PLL Block Diagram



The counter settings define the PLL output frequency:

| Internal Feedback Mode | Local and Core Feedback Mode | Where: |
|--|--|---|
| $F_{PFD} = F_{IN} / N$ $F_{VCO} = F_{PFD} \times M$ $F_{OUT} = (F_{IN} \times M) / (N \times O \times C)$ $F_{PLL} = F_{VCO} / O$ | $F_{PFD} = F_{IN} / N$ $F_{VCO} = (F_{PFD} \times M \times O \times C_{FBK})^{(4)}$ $F_{OUT} = (F_{IN} \times M \times C_{FBK}) / (N \times C)$ $F_{PLL} = F_{VCO} / O$ | F_{VCO} is the voltage control oscillator frequency F_{OUT} is the output clock frequency F_{IN} is the reference clock frequency F_{PFD} is the phase frequency detector input frequency F_{PLL} is the post-divider PLL frequency C is the output divider O is the post-divider M is the multiplier N is the pre-divider C_{FBK} is the output divider for CLKOUT0 |



Note: F_{IN} must be within the values stated in [PLL Timing and AC Characteristics](#) on page 61.

⁽⁴⁾ $(M \times O \times C_{FBK})$ must be ≤ 255 .

Figure 11: PLL Interface Block Diagram

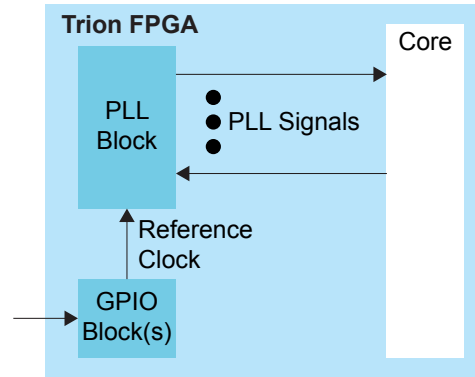


Table 13: PLL Signals (Interface to FPGA Fabric)

| Signal | Direction | Description |
|-------------------------------|-----------|--|
| CLKIN[3:0] | Input | Reference clocks driven by I/O pads or core clock tree. |
| CLKSEL[1:0] | Input | You can dynamically select the reference clock from one of the clock in pins. |
| RSTN | Input | Active-low PLL reset signal. When asserted, this signal resets the PLL; when de-asserted, it enables the PLL. De-assert only when the CLKIN signal is stable. Connect this signal in your design to power up or reset the PLL. Assert the RSTN pin for a minimum pulse of 10 ns to reset the PLL. Assert RSTN when dynamically changing the selected PLL reference clock. |
| COREFBK | Input | Connect to a clock out interface pin when the the PLL feedback mode is set to core. |
| CLKOUT0 CLKOUT1 CLKOUT2 | Output | PLL output. The designer can route these signals as input clocks to the core's GCLK network. |
| LOCKED | Output | Goes high when PLL achieves lock; goes low when a loss of lock is detected; remains at previous state if the CLKIN goes discontinuous. Connect this signal in your design to monitor the lock status. This signal is not synchronized to any clock and the minimum high or low pulse width of the lock signal may be smaller than the CLKOUT's period. |

Table 14: PLL Interface Designer Settings - Properties Tab

| Parameter | Choices | Notes |
|-----------------------------|--------------|--|
| Instance Name | User defined | |
| PLL Resource | | The resource listing depends on the FPGA you choose. |
| Clock Source | External | PLL reference clock comes from external source through the REFCLK pin. Select the available external clock. |
| | Dynamic | PLL reference clock comes from up to four possible sources (external and core), and are controlled by the clock select bus. Specify the clock selector and core clock names. |
| | Core | PLL reference clock comes from the core. Specify the core clock pin name. |
| Automated Clock Calculation | | Pressing this button launches the PLL Clock Calculation window. The calculator helps you define PLL settings in an easy-to-use graphical interface. |

Table 15: PLL Interface Designer Settings - Manual Configuration Tab

| Parameter | Choices | Notes |
|---------------------------------|-----------------------------|---|
| Reset Pin Name | User defined | |
| Locked Pin Name | User defined | |
| Feedback Mode | Internal | PLL feedback is internal to the PLL resulting in no known phase relationship between clock in and clock out. |
| | Local | PLL feedback is local to the PLL. Aligns the clock out phase with clock in. |
| | Core | PLL feedback is from the core. The feedback clock is defined by the COREFBK connection, and must be one of the three PLL output clocks. Aligns the clock out phase with clock in and removes the core clock delay. |
| Reference clock Frequency (MHz) | User defined | |
| Multiplier (M) | 1 - 255 (integer) | M counter. |
| Pre Divider (N) | 1 - 15 (integer) | N counter. |
| Post Divider (O) | 1, 2, 4, 8 | O counter. The value must be 2 or higher if you enable more than 1 PLL output. |
| Clock 0, Clock 1, Clock 2 | On, off | Use these checkboxes to enable or disable clock 0, 1, and 2. |
| Pin Name | User defined | Specify the pin name for clock 0, 1, or 2. |
| Divider (C) | 1 to 256 | Output divider. |
| Phase Shift (Degree) | 0, 45, 90, 135, 180, or 270 | Phase shift CLKOUT by 45°, 90°, 135°, 180°, or 270°. The phase shifts are supported with the following C divider settings: C divider = 2 : 90°, 180°, and 270° C divider = 4 : 45°, 90°, and 135° C divider = 6 : 90° To phase shift 225°, select 45° and invert the clock at the destination. To phase shift 315°, select 135° and invert the clock at the destination. |
| Use as Feedback | On, off | |

Table 16: PLL Reference Clock Resource Assignments (BGA256)

| PLL | REFCLK0 | REFCLK1 |
|---------|------------------|---|
| PLL_BL0 | GPIOL_15_PLLIN0 | GPIOL_19_PLLN1 |
| PLL_BR0 | GPIOR_138_PLLIN0 | Single-ended: GPIOB_TXP09_CLK0 |
| PLL_BR1 | GPIOR_139_PLLIN1 | Single-ended: GPIOB_TXP15_CLK1_CDI15 |
| PLL_BR2 | GPIOR_140_PLLIN2 | Single-ended: GPIOB_TXP19_CLK2 |
| PLL_TR0 | GPIOR_118_PLLIN0 | Differential: GPIOT_RXP08_CLKP0, GPIOT_RXN08_CLKN0 Single-ended: GPIOT_RXP08_CLKP0 |
| PLL_TR1 | GPIOR_119_PLLIN1 | Differential: GPIOT_RXP17_CLKP1, GPIOT_RXN17_CLKN1 Single-ended: GPIOT_RXP17_CLKP1 |
| PLL_TR2 | GPIOR_120_PLLIN2 | - |

Table 17: PLL Reference Clock Resource Assignments (BGA324)

| PLL | REFCLK0 | REFCLK1 |
|------------------------|------------------|---|
| PLL_BL0 | GPIOL_15_PLLIN0 | - |
| PLL_BR0 ⁽⁵⁾ | GPIOR_138_PLLIN0 | Single-ended: GPIOB_TXP09_CLK0 |
| PLL_BR1 | GPIOR_139_PLLIN1 | Single-ended: GPIOB_TXP15_CLK1_CDI15 |
| PLL_BR2 | GPIOR_140_PLLIN2 | Single-ended: GPIOB_TXP19_CLK2 |
| PLL_TR0 | GPIOR_118_PLLIN0 | Differential: GPIOT_RXP08_CLKP0, GPIOT_RXN08_CLKN0 Single-ended: GPIOT_RXP08_CLKP0 |
| PLL_TR1 | GPIOR_119_PLLIN1 | Differential: GPIOT_RXP17_CLKP1, GPIOT_RXN17_CLKN1 Single-ended: GPIOT_RXP17_CLKP1 |
| PLL_TR2 | GPIOR_120_PLLIN2 | Differential: GPIOT_RXP25_CLKP2, GPIOT_RXN25_CLKN2 Single-ended: GPIOT_RXP25_CLKP2 |

Table 18: PLL Reference Clock Resource Assignments (BGA400)

| PLL | REFCLK0 | REFCLK1 |
|------------------------|------------------|---|
| PLL_BL0 | GPIOL_15_PLLIN0 | GPIOL_19_PLLN1 |
| PLL_BR0 ⁽⁵⁾ | GPIOR_138_PLLIN0 | Single-ended: GPIOB_TXP09_CLK0 |
| PLL_BR1 | GPIOR_139_PLLIN1 | Single-ended: GPIOB_TXP15_CLK1_CDI15 |
| PLL_BR2 | GPIOR_140_PLLIN2 | Single-ended: GPIOB_TXP19_CLK2 |
| PLL_TR0 | GPIOR_118_PLLIN0 | Differential: GPIOT_RXP08_CLKP0, GPIOT_RXN08_CLKN0 Single-ended: GPIOT_RXP08_CLKP0 |
| PLL_TR1 | GPIOR_119_PLLIN1 | Differential: GPIOT_RXP17_CLKP1, GPIOT_RXN17_CLKN1 Single-ended: GPIOT_RXP17_CLKP1 |
| PLL_TR2 | GPIOR_120_PLLIN2 | Differential: GPIOT_RXP25_CLKP2, GPIOT_RXN25_CLKN2 Single-ended: GPIOT_RXP25_CLKP2 |

⁽⁵⁾ PLL_BR0 can be used as the PHY clock for DDR DRAM block.

LVDS

The LVDS hard IP transmitters and receivers operate independently.

- LVDS TX consists of LVDS transmitter and serializer logic.
- LVDS RX consists of LVDS receiver, on-die termination, and de-serializer logic.

The T35 has up to three PLLs for use with the LVDS receiver.



Note: You can use the LVDS TX and LVDS RX channels as 3.3 V, 2.5 V, or 1.8 V single-ended GPIO pins, which support a weak pull-up and variable drive strength but do not support a Schmitt trigger. When using LVDS as GPIO, make sure to leave at least 2 pairs of unassigned LVDS pins between any GPIO and LVDS pins. This rule applies for pins on each side of the device (top, bottom, left, right). This separation reduces noise. The Efinity software issues an error if you do not leave this separation.

The LVDS hard IP has these features:

- Supports serialization and deserialization factors: 8:1, 7:1, 6:1, 5:1, 4:1, 3:1, and 2:1
- Ability to disable serialization and deserialization
- Source synchronous clock output edge-aligned with data for LVDS transmitter and receiver
- 100 Ω on-die termination resistor for the LVDS receiver



Note: The LVDS RX supports the sub-lvds, slvs, HiVcm, RSDS and 3.3 V LVPECL differential I/O standards with a transfer rate of up to 800 Mbps.

LVDS TX

Figure 12: LVDS TX Interface Block Diagram

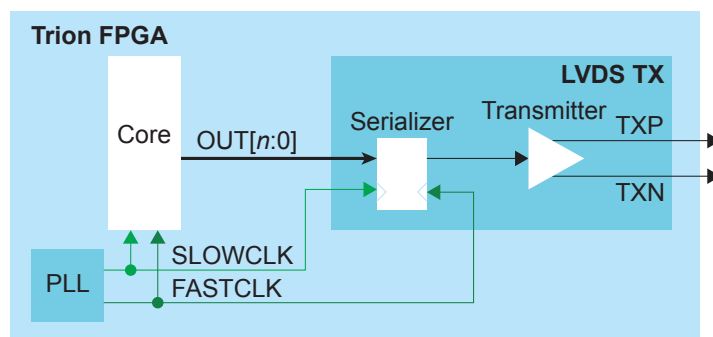


Table 19: LVDS TX Signals (Interface to FPGA Fabric)

| Signal | Direction | Notes |
|------------|-----------|--|
| OUT[n-1:0] | Input | Parallel output data where n is the serialization factor. A width of 1 bypasses the serializer. |
| FASTCLK | Input | Fast clock to serialize the data to the LVDS pads. |
| SLOWCLK | Input | Slow clock to latch the incoming data from the core. |

Table 20: LVDS TX Pads

| Pad | Direction | Description |
|-----|-----------|---------------------|
| TXP | Output | Differential P pad. |
| TXN | Output | Differential N pad. |

The following waveform shows the relationship between the fast clock, slow clock, TX data going to the pad, and byte-aligned data from the core.

Figure 13: LVDS Timing Example Serialization Width of 8

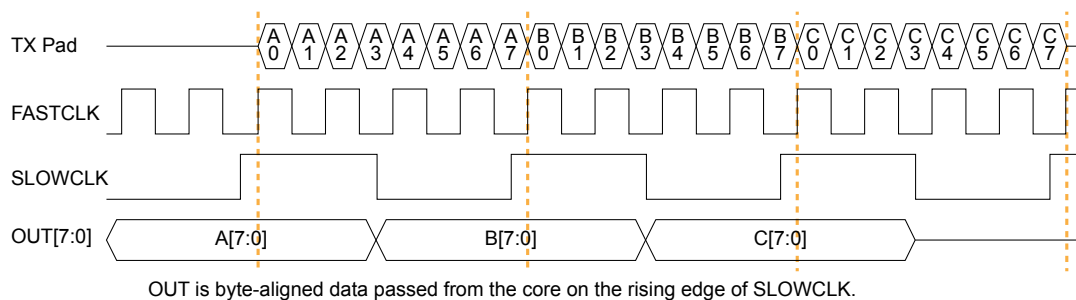


Figure 14: LVDS Timing Data and Clock Relationship Width of 8 (Parallel Clock Division=1)

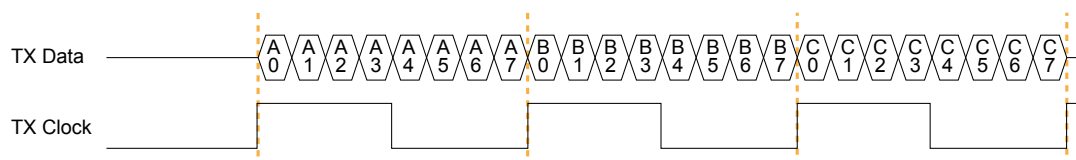
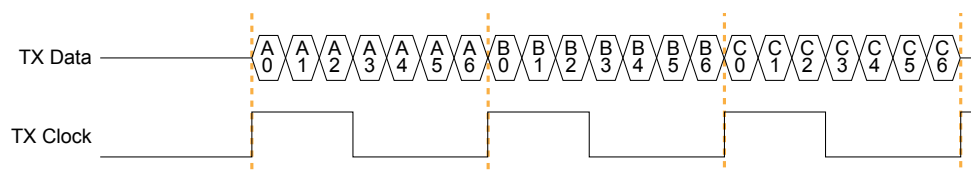


Figure 15: LVDS Timing Data and Clock Relationship Width of 7 (Parallel Clock Division=1)



Note: For LVDS TX interfaces with multiple LVDS TX lanes and an LVDS TX reference clock output, use the LVDS TX blocks from the same side of the FPGA to minimize skew between data lanes and TX reference clock output.

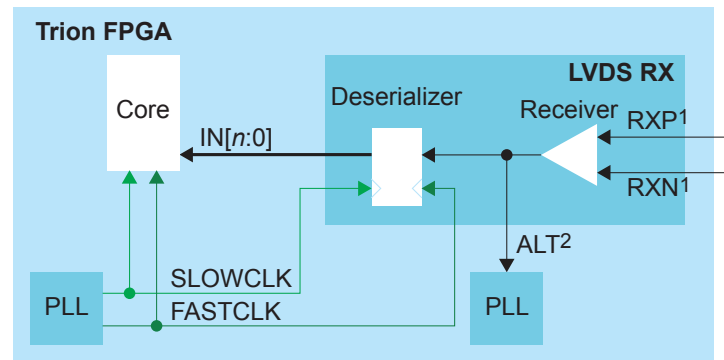
Table 21: LVDS TX Settings in Efinity® Interface Designer

| Parameters | Choices | Notes |
|-------------------------|--|--|
| Instance Name | User defined | |
| LVDS Resource | Resource list | Choose a resource. |
| Mode | serial data output or reference clock output | serial data output —Simple output buffer or serialized output. reference clock output —Use the transmitter as a clock output. When choosing this mode, the Serialization Width you choose should match the serialization for the rest of the LVDS bus. |
| Parallel Clock Division | 1, 2 | 1 —The output clock from the LVDS TX lane is parallel clock frequency. 2 —The output clock from the TX lane is half of the parallel clock frequency. |
| Enable Serialization | On or off | When off, the serializer is bypassed and the LVDS buffer is used as a normal output. |
| Serialization Width | 2, 3, 4, 5, 6, 7, or 8 | Supports 8:1, 7:1, 6:1, 5:1, 4:1, 3:1, and 2:1. Specify the serial clock and parallel clock. |
| Output Pin/Bus Name | User defined | Output pin or bus that feeds the LVDS transmitter parallel data. The width should match the serialization factor. |

| Parameters | Choices | Notes |
|------------------------|---------------|---|
| Output Enable Pin Name | User defined | Use with serial data output mode. Only available when serialization is disabled. |
| Reduce VOD Swing | On or off | When true, enables reduced output swing (similar to slow slew rate). |
| Output Load | 3, 5, 7 or 10 | Output load in pF. Use an output load of 7 pF or higher to achieve the maximum supported toggle rate. See Table 75: Maximum Toggle Rate on page 55. |

LVDS RX

Figure 16: LVDS RX Interface Block Diagram



1. There is a ~30k Ω internal weak pull-up to VCCIO (3.3V).
2. Only available for an LVDS RX resource in bypass mode (deserialization width is 1).

Table 22: LVDS RX Signals (Interface to FPGA Fabric)

| Signal | Direction | Notes |
|-----------|-----------|--|
| IN[n-1:0] | Output | Parallel input data where n is the de-serialization factor. A width of 1 bypasses the deserializer. |
| ALT | Output | Alternative input, only available for an LVDS RX resource in bypass mode (deserialization width is 1; alternate connection type). Alternative connections are PLL_CLKIN. |
| FASTCLK | Input | Fast clock to de-serialize the data from the LVDS pads. |
| SLOWCLK | Input | Slow clock to latch the incoming data to the core. |

Table 23: LVDS RX Pads

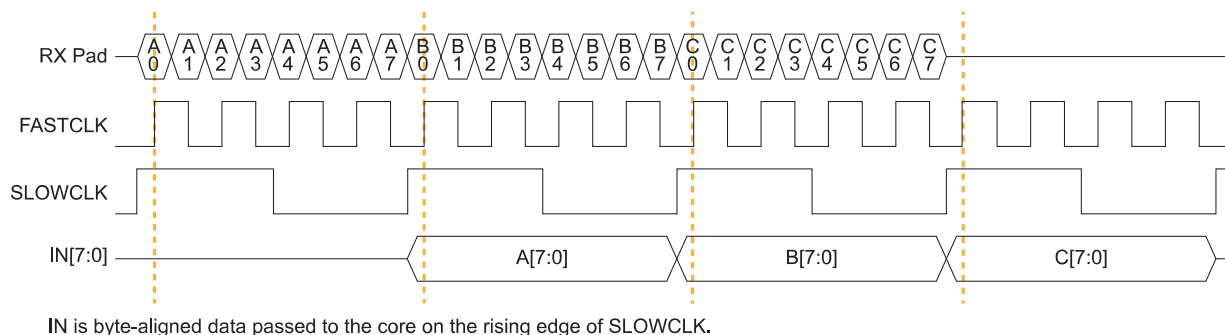
| Pad | Direction | Description |
|-----|-----------|---------------------|
| RXP | Input | Differential P pad. |
| RXN | Input | Differential N pad. |



Note: You need an external DC-biased circuit if the incoming LVDS signals are AC-coupled. Refer to [Trion Hardware Design Checklist and Guidelines](#) for more information.

The following waveform shows the relationship between the fast clock, slow clock, RX data coming in from the pad, and byte-aligned data to the core.

Figure 17: LVDS RX Timing Example Serialization Width of 8



Note: For LVDS RX interfaces with multiple LVDS RX lanes and an LVDS RX clock input, use the LVDS RX blocks from the same side of the FPGA to minimize skew between data lanes and RX clock input.

Table 24: LVDS RX Settings in Efinity® Interface Designer

| Parameter | Choices | Notes |
|---------------------------|------------------------|---|
| Instance Name | User defined | |
| LVDS Resource | Resource list | Choose a resource. |
| Connection Type | normal, pll_clkln | normal —Regular RX function. pll_clkln —Use the PLL CLKIN alternate function of the LVDS RX resource. |
| Input Pin/Bus Name | User defined | Input pin or bus that feeds the LVDS transmitter parallel data. The width should match the deserialization factor. |
| Dynamic Enable Pin Name | User defined | Dynamically enables or disables the LVDS RX buffer. Disabling the buffer can reduce power consumption when the pin is not in use. |
| Enable Deserialization | On or off | When off, the de-serializer is bypassed and the LVDS buffer is used as a normal input. Specify the serial clock and parallel clock. |
| Deserialization Width | 2, 3, 4, 5, 6, 7, or 8 | Supports 8:1, 7:1, 6:1, 5:1, 4:1, 3:1, and 2:1. |
| Enable On-Die Termination | On or off | When on, enables an on-die 100-ohm resistor. |
| Static Mode Delay Setting | 0 - 63 | Choose the amount of static delay, each step adds approximately 25 ps of delay. |

MIPI

The MIPI CSI-2 interface is the most widely used camera interface for mobile.⁽⁶⁾ You can use this interface to build single- or multi-camera designs for a variety of applications.

T35 FPGAs include two hardened MIPI D-PHY blocks (4 data lanes and 1 clock lane) with MIPI CSI-2 IP blocks. The MIPI RX and MIPI TX can operate independently with dedicated I/O banks.

⁽⁶⁾ Source: MIPI Alliance <https://www.mipi.org/specifications/csi-2>



Note: The MIPI D-PHY and CSI-2 controller are hard blocks; users cannot bypass the CSI-2 controller to access the D-PHY directly for non-CSI-2 applications.

The MIPI TX/RX interface supports the MIPI CSI-2 specification v1.3 and the MIPI D-PHY specification v1.1. It has the following features:

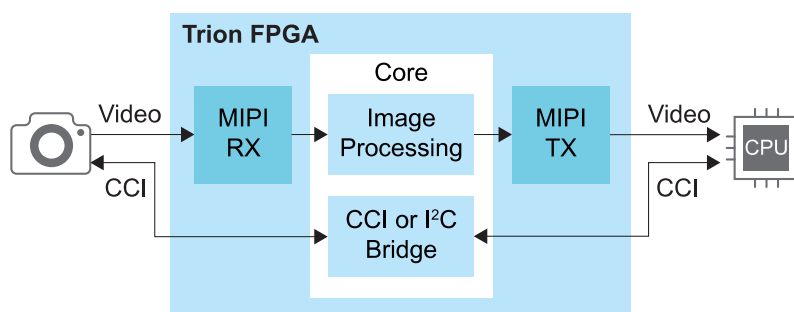
- Programmable data lane configuration supporting 1, 2, or 4 lanes
- High-speed mode supports up to 1.5 Gbps data rates per lane
- Operates in continuous and non-continuous clock modes
- 64 bit pixel interface for cameras
- Supports Ultra-Low Power State (ULPS)

Table 25: MIPI Supported Data Types

| Supported Data Type | Format |
|---------------------|--|
| RAW | RAW6, RAW7, RAW8, RAW10, RAW12, RAW14 |
| YUV | YUV420 8-bit (legacy), YUV420 8-bit, YUV420 10-bit, YUV420 8-bit (CSPS), YUV420 10-bit (CSPS), YUV422 8-bit, YUV422 10-bit |
| RGB | RGB444, RGB555, RGB565, RGB666, RGB888 |
| User Defined | 8 bit format |

With more than one MIPI TX and RX blocks, Trion® FPGAs support a variety of video applications.

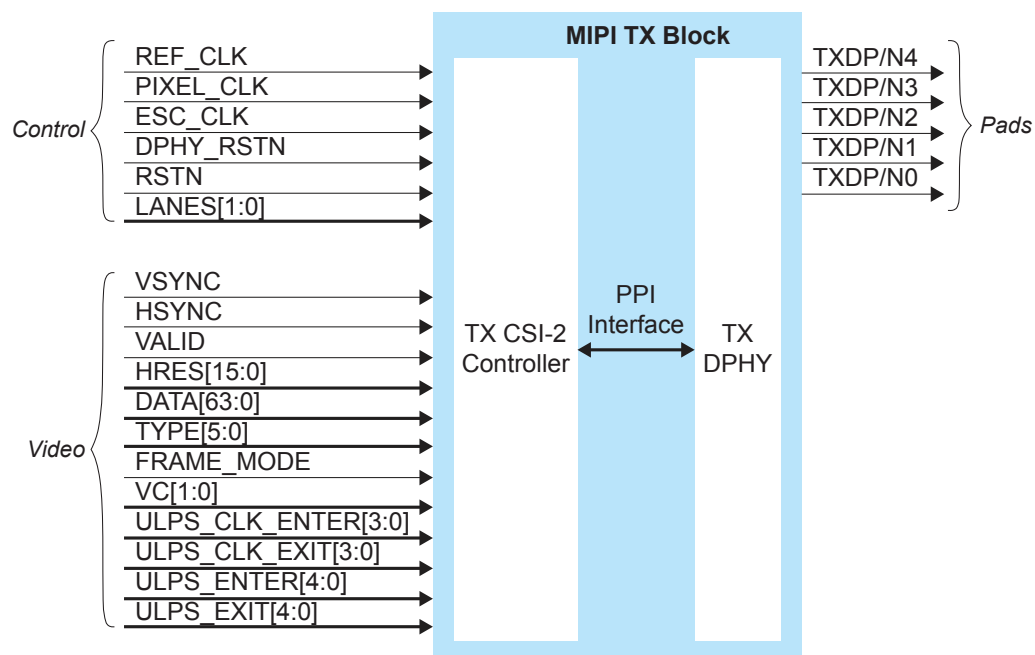
Figure 18: MIPI Example System



MIPI TX

The MIPI TX is a transmitter interface that translates video data from the Trion® core into packetized data sent over the HSSI interface to the board. Five high-speed differential pin pairs (four data, one clock), each of which represent a lane, connect to the board. Control and video signals connect from the MIPI interface to the core.

Figure 19: MIPI TX x4 Block Diagram



The control signals determine the clocking and how many transceiver lanes are used. All control signals are required except the two reset signals. The reset signals are optional, however, you must use both signals or neither.

The MIPI block requires an escape clock (ESC_CLK) for use when the MIPI interface is in escape (low-power) mode, which runs between 11 and 20 MHz.



Note: Efinix recommends that you set the escape clock frequency as close to 20 MHz as possible.

The video signals receive the video data from the core. The MIPI interface block encodes is and sends it out through the MIPI D-PHY lanes.

Figure 20: MIPI TX Interface Block Diagram

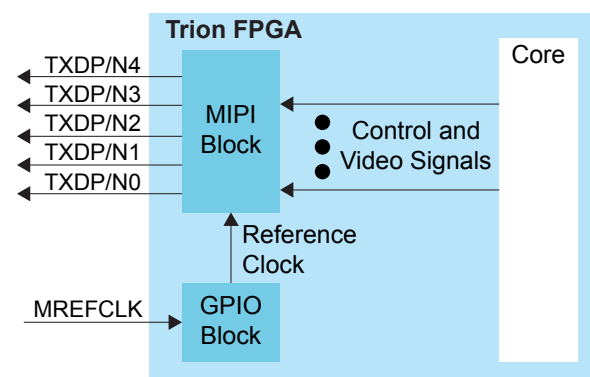


Table 26: MIPI TX Control Signals (Interface to FPGA Fabric)

| Signal | Direction | Clock Domain | Description |
|------------|-----------|--------------|--|
| REF_CLK | Input | N/A | Reference clock for the internal MIPI TX PLL used to generate the transmitted data. The FPGA has a dedicated GPIO resource (MREFCLK) that you must configure to provide the reference clock. All of the MIPI TX blocks share this resource. The frequency is set using Interface Designer configuration options. |
| PIXEL_CLK | Input | N/A | Clock used for transferring data from the core to the MIPI TX block. The frequency is based on the number of lanes and video format. |
| ESC_CLK | Input | N/A | Slow clock for escape mode (11 - 20 MHz). |
| DPHY_RSTN | Input | N/A | (Optional) Reset for the D-PHY logic, active low. Reset with the controller. See MIPI Reset Timing on page 60. |
| RSTN | Input | N/A | (Optional) Reset for the CSI-2 controller logic, active low. Typically, you reset the controller with the PHY (see MIPI Reset Timing on page 60). However, when dynamically changing the horizontal resolution, you only need to trigger RSTN (see TX Requirements for Dynamically Changing the Horizontal Resolution). |
| LANES[1:0] | Input | PIXEL_CLK | Determines the number of lanes enabled. Can only be changed during reset. 00: lane 0 01: lanes 0 and 1 11: all lanes |

Table 27: MIPI TX Video Signals (Interface to FPGA Fabric)

| Signal | Direction | Clock Domain | Description |
|-----------------|-----------|--------------|--|
| VSYNC | Input | PIXEL_CLK | Vertical sync. |
| HSYNC | Input | PIXEL_CLK | Horizontal sync. |
| VALID | Input | PIXEL_CLK | Valid signal. |
| HRES[15:0] | Input | PIXEL_CLK | Horizontal resolution. Can only be changed when VSYNC is low, and should be stable for at least one TX pixel clock cycle before VSYNC goes high. |
| DATA[63:0] | Input | PIXEL_CLK | Video data; the format depends on the data type. New data arrives on every pixel clock. |
| TYPE[5:0] | Input | PIXEL_CLK | Video data type. Can only be changed when HSYNC is low, and should be stable for at least one TX pixel clock cycle before HSYNC goes high. |
| FRAME_MODE | Input | PIXEL_CLK | Selects frame format. ⁽⁷⁾ 0: general frame 1: accurate frame Can only be changed during reset. |
| VC[1:0] | Input | PIXEL_CLK | Virtual channel (VC). Can only be changed when VSYNC is low, and should be stable at least one TX pixel clock cycle before VSYNC goes high. |
| ULPS_CLK_ENTER | Input | PIXEL_CLK | Place the clock lane into ULPS mode. Should not be active at the same time as ULPS_CLK_EXIT. Each high pulse should be at least 5 μ s. |
| ULPS_CLK_EXIT | Input | PIXEL_CLK | Remove clock lane from ULPS mode. Should not be active at the same time as ULPS_CLK_ENTER. Each high pulse should be at least 5 μ s. |
| ULPS_ENTER[3:0] | Input | PIXEL_CLK | Place the data lane into ULPS mode. Should not be active at the same time as ULPS_EXIT[3:0]. Each high pulse should be at least 5 μ s. |
| ULPS_EXIT[3:0] | Input | PIXEL_CLK | Remove the data lane from ULPS mode. Should not be active at the same time as ULPS_ENTER[3:0]. Each high pulse should be at least 5 μ s. |

Table 28: MIPI TX Pads

| Pad | Direction | Description |
|-----------|-----------|--------------------------|
| TXDP[4:0] | Output | MIPI transceiver P pads. |
| TXDN[4:0] | Output | MIPI transceiver N pads. |

⁽⁷⁾ Refer to the MIPI Camera Serial Interface 2 (MIPI CSI-2) for more information about frame formats.

Table 29: MIPI TX Settings in Efinity® Interface Designer

| Tab | Parameter | Choices | Notes |
|--------------------|--|--|--|
| Base | PHY Bandwidth (Mbps) | 80.00 - 1500.00 | Choose one of the possible PHY bandwidth values. |
| | Frequency (reference clock) | 6, 12, 19.2, 25, 26, 27, 38.4, or 52 MHz | Reference clock frequency. |
| | Enable Continuous PHY Clocking | On or Off | Turns continuous clock mode on or off. |
| Control | Escape Clock Pin Name | User defined | |
| | Invert Escape Clock | On or Off | |
| | Pixel Clock Pin Name | User defined | |
| | Invert Pixel Clock | On or Off | |
| Lane Mapping | TXD0, TXD1, TXD2, TXD3, TXD4 | clk, data0, data1, data2, or data3 | Map the physical lane to a clock or data lane. |
| Clock Timer | | | |
| Timing | T _{CLK-POST} T _{CLK-TRAIL} T _{CLK-PREPARE} T _{CLK-ZERO} | Varies depending on the PHY frequency | Changes the MIPI transmitter timing parameters per the DPHY specification. Refer to D-PHY Timing Parameters on page 36. |
| | Escape Clock Frequency (MHz) | User defined | Specify a number between 11 and 20 MHz. |
| | T _{CLK-PRE} | Varies depending on the escape clock frequency | Changes the MIPI transmitter timing parameters per the DPHY specification. Refer to D-PHY Timing Parameters on page 36. |
| | Data Timer | | |
| | T _{HS-PREPARE} T _{HS-ZERO} T _{HS-PTRAIL} | Varies depending on the PHY frequency | Changes the MIPI transmitter timing parameters per the DPHY specification. Refer to D-PHY Timing Parameters on page 36. |

MIPI TX Video Data TYPE[5:0] Settings

The video data type can only be changed when HSYNC is low.

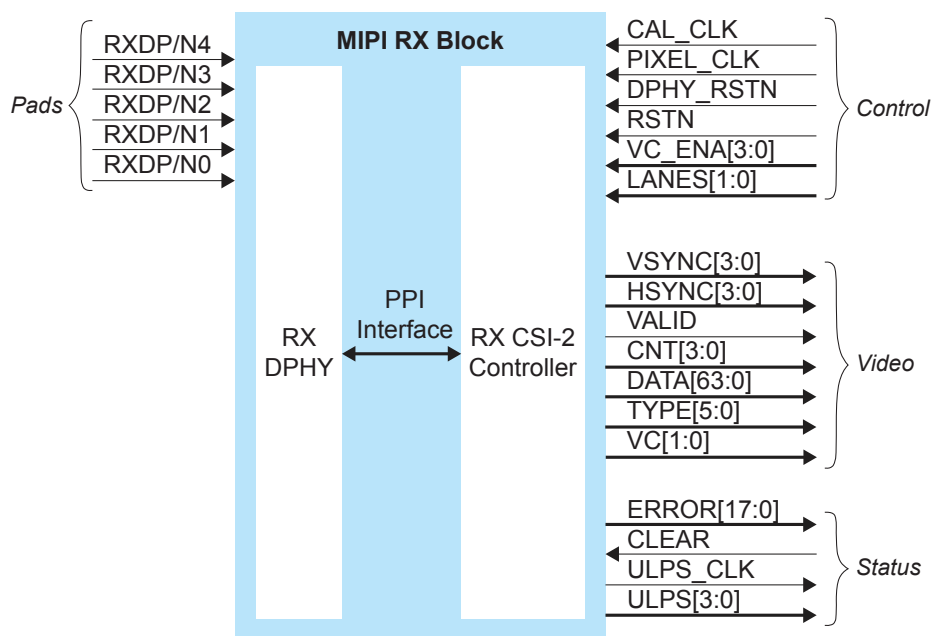
Table 30: MIPI TX TYPE[5:0]

| TYPE[5:0] | Data Type | Pixel Data Bits per Pixel Clock | Pixels per Clock | Bits per Pixel | Maximum Data Pixels per Line |
|-----------|----------------------|---------------------------------|-----------------------------|-----------------------------------|------------------------------|
| 0x20 | RGB444 | 48 | 4 | 12 | 2,880 |
| 0x21 | RGB555 | 60 | 4 | 15 | 2,880 |
| 0x22 | RGB565 | 64 | 4 | 16 | 2,880 |
| 0x23 | RGB666 | 54 | 3 | 18 | 2,556 |
| 0x24 | RGB888 | 48 | 2 | 24 | 1,920 |
| 0x28 | RAW6 | 60 | 10 | 6 | 7,680 |
| 0x29 | RAW7 | 56 | 8 | 7 | 6,576 |
| 0x2A | RAW8 | 64 | 8 | 8 | 5,760 |
| 0x2B | RAW10 | 60 | 6 | 10 | 4,608 |
| 0x2C | RAW12 | 60 | 5 | 12 | 3,840 |
| 0x2D | RAW14 | 56 | 4 | 14 | 3,288 |
| 0x18 | YUV420 8 bit | Odd line: 64 Even line: 64 | Odd line: 8 Even line: 4 | Odd line: 8 Even line: 8, 24 | 2,880 |
| 0x19 | YUV420 10 bit | Odd line: 60 Even line: 40 | Odd line: 6 Even line: 2 | Odd line: 10 Even line: 10, 30 | 2,304 |
| 0x1A | Legacy YUV420 8 bit | 48 | 4 | 8, 16 | 3,840 |
| 0x1C | YUV420 8 bit (CSPS) | Odd line: 64 Even line: 64 | Odd line: 8 Even line: 4 | Odd line: 8 Even line: 8, 24 | 2,880 |
| 0x1D | YUV420 10 bit (CSPS) | Odd line: 60 Even line: 40 | Odd line: 6 Even line: 2 | Odd line: 10 Even line: 10, 30 | 2,304 |
| 0x1E | YUV422 8 bit | 64 | 4 | 8, 24 | 2,880 |
| 0x1F | YUV422 10 bit | 40 | 2 | 10, 30 | 2,304 |
| 0x30 - 37 | User defined 8 bit | 64 | 8 | 8 | 5,760 |

MIPI RX

The MIPI RX is a receiver interface that translates HSSI signals from the board to video data in the Trion® core. Five high-speed differential pin pairs (one clock, four data), each of which represent a lane, connect to the board. Control, video, and status signals connect from the MIPI interface to the core.

Figure 21: MIPI RX x4 Block Diagram



The control signals determine the clocking, how many transceiver lanes are used, and how many virtual channels are enabled. All control signals are required except the two reset signals. The reset signals are optional, however, you must use both signals or neither.

The video signals send the decoded video data to the core. All video signals must fully support the MIPI standard.

The status signals provide optional status and error information about the MIPI RX interface operation.

Figure 22: MIPI RX Interface Block Diagram

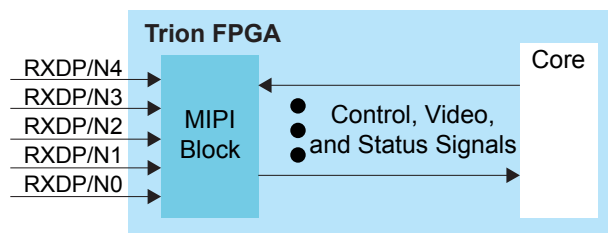


Table 31: MIPI RX Control Signals (Interface to FPGA Fabric)

| Signal | Direction | Clock Domain | Notes |
|-------------|-----------|--------------|--|
| CAL_CLK | Input | N/A | Used for D-PHY calibration; must be between 80 and 120 MHz. |
| PIXEL_CLK | Input | N/A | Clock used for transferring data to the core from the MIPI RX block. The frequency based on the number of lanes and video format. |
| DPHY_RSTN | Input | N/A | (Optional) Reset for the D-PHY logic, active low. Must be used if RSTN is used. See MIPI Reset Timing on page 60. |
| RSTN | Input | N/A | (Optional) Reset for the CSI-2 controller logic, active low. Must be used if DPHY_RSTN is used. See MIPI Reset Timing on page 60. |
| VC_ENA[3:0] | Input | PIXEL_CLK | Enables different VC channels by setting their index high. |
| LANES[1:0] | Input | PIXEL_CLK | Determines the number of lanes enabled: 00: lane 0 01: lanes 0 and 1 11: all lanes Can only be set during reset. |

Table 32: MIPI RX Video Signals (Interface to FPGA Fabric)

| Signal | Direction | Clock Domain | Notes |
|------------|-----------|--------------|--|
| VSYNC[3:0] | Output | PIXEL_CLK | Vsync bus. High if vsync is active for this VC. |
| HSYNC[3:0] | Output | PIXEL_CLK | Hsync bus. High if hsync is active for this VC |
| VALID | Output | PIXEL_CLK | Valid signal. |
| CNT[3:0] | Output | PIXEL_CLK | Number of valid pixels contained in the pixel data. |
| DATA[63:0] | Output | PIXEL_CLK | Video data, format depends on data type. New data every pixel clock. |
| TYPE[5:0] | Output | PIXEL_CLK | Video data type. |
| VC[1:0] | Output | PIXEL_CLK | Virtual channel (VC). |

Table 33: MIPI RX Status Signals (Interface to FPGA Fabric)

| Signal | Direction | Signal Interface | Clock Domain | Notes |
|-------------|-----------|------------------|--------------|---|
| ERROR[17:0] | Output | IN | PIXEL_CLK | Error bus register. Refer to Table 34: MIPI RX Error Signals (ERROR[17:0]) on page 33 for details. |
| CLEAR | Input | OUT | PIXEL_CLK | Reset the error registers. |
| ULPS_CLK | Output | IN | PIXEL_CLK | High when the clock lane is in the Ultra-Low-Power State (ULPS). |
| ULPS[3:0] | Output | IN | PIXEL_CLK | High when the lane is in the ULPS mode. |

Table 34: MIPI RX Error Signals (ERROR[17:0])

| Bit | Name | Description |
|-----|-------------------|--|
| 0 | ERR_ESC | Escape Entry Error. Asserted when an unrecognized escape entry command is received. |
| 1 | CRC_ERROR_VC0 | CRC Error VC0. Set to 1 when a checksum error occurs. |
| 2 | CRC_ERROR_VC1 | CRC Error VC1. Set to 1 when a checksum error occurs. |
| 3 | CRC_ERROR_VC2 | CRC Error VC2. Set to 1 when a checksum error occurs. |
| 4 | CRC_ERROR_VC3 | CRC Error VC3. Set to 1 when a checksum error occurs. |
| 5 | HS_RX_TIMEOUT_ERR | HS RX Timeout Error. The protocol should time out when no EoT is received within a certain period in HS RX mode. |
| 6 | ECC_1BIT_ERROR | ECC Single Bit Error. Set to 1 when there is a single bit error. |
| 7 | ECC_2BIT_ERROR | ECC 2 Bit Error. Set to 1 if there is a 2 bit error in the packet. |
| 8 | ECCBIT_ERROR | ECC Error. Asserted when an error exists in the ECC. |
| 9 | ECC_NO_ERROR | ECC No Error. Asserted when an ECC is computed with a result zero. This bit is high when the receiver is receiving data correctly. |
| 10 | FRAME_SYNC_ERROR | Frame Sync Error. Asserted when a frame end is not paired with a frame start on the same virtual channel. |
| 11 | INVLD_PKT_LEN | Invalid Packet Length. Set to 1 if there is an invalid packet length. |
| 12 | INVLD_VC | Invalid VC ID. Set to 1 if there is an invalid CSI VC ID. |
| 13 | INVALID_DATA_TYPE | Invalid Data Type. Set to 1 if the received data is invalid. |
| 14 | ERR_FRAME | Error In Frame. Asserted when VSYNC END received when CRC error is present in the data packet. |
| 15 | CONTROL_ERR | Control Error. Asserted when an incorrect line state sequence is detected. |
| 16 | SOT_ERR | Start-of-Transmission (SoT) Error. Corrupted high-speed SoT leader sequence while proper synchronization can still be achieved. |
| 17 | SOT_SYNC_ERR | SoT Synchronization Error. Corrupted high-speed SoT leader sequence while proper synchronization cannot be expected. |



Note: If error report is all logic low, there is an EOT or a contention error. Check the physical connection of MIPI lanes or adjust the EXIT and TRAIL parameters according to the MIPI Utility.

Table 35: MIPI RX Pads

| Pad | Direction | Description |
|-----------|-----------|--------------------------|
| RXDP[4:0] | Input | MIPI transceiver P pads. |
| RXDN[4:0] | Input | MIPI transceiver N pads. |

Table 36: MIPI RX Settings in Efinity® Interface Designer

| Tab | Parameter | Choices | Notes |
|--------------|----------------------------------|------------------------------------|---|
| Control | DPHY Calibration Clock Pin Name | User defined | |
| | Invert DPHY Calibration Clock | On or Off | |
| | Pixel Clock Pin Name | User defined | |
| | Invert Pixel Clock | On or Off | |
| Status | Enable Status | On or Off | Indicate whether you want to use the status pins. |
| Lane Mapping | RXD0, RXD1, RXD2, RXD3, RXD4 | clk, data0, data1, data2, or data3 | Map the physical lane to a clock or data lane. |
| | Swap P&N Pin | On or Off | Reverse the P and N pins for the physical lane. |
| Timing | Calibration Clock Freq (MHz) | User defined | Specify a number between 80 and 120 MHz. |
| | Clock Timer ($T_{CLK-SETTLE}$) | 40 - 2,590 ns | Changes the MIPI receiver timing parameters per the DPHY specification. Refer to D-PHY Timing Parameters on page 36. |
| | Data Timer ($T_{HS-SETTLE}$) | 40 - 2,590 ns | Changes the MIPI receiver timing parameters per the DPHY specification. Refer to D-PHY Timing Parameters on page 36. |

MIPI RX Video Data TYPE[5:0] Settings

The video data type can only be changed when HSYNC is low.

Table 37: MIPI RX TYPE[5:0]

| TYPE[5:0] | Data Type | Pixel Data Bits per Pixel Clock | Pixels per Clock | Bits per Pixel | Maximum Data Pixels per Line |
|-----------|----------------------|---------------------------------|-----------------------------|-----------------------------------|------------------------------|
| 0x20 | RGB444 | 48 | 4 | 12 | 2,880 |
| 0x21 | RGB555 | 60 | 4 | 15 | 2,880 |
| 0x22 | RGB565 | 64 | 4 | 16 | 2,880 |
| 0x23 | RGB666 | 54 | 3 | 18 | 2,556 |
| 0x24 | RGB888 | 48 | 2 | 24 | 1,920 |
| 0x28 | RAW6 | 48 | 8 | 6 | 7,680 |
| 0x29 | RAW7 | 56 | 8 | 7 | 6,576 |
| 0x2A | RAW8 | 64 | 8 | 8 | 5,760 |
| 0x2B | RAW10 | 40 | 4 | 10 | 4,608 |
| 0x2C | RAW12 | 48 | 4 | 12 | 3,840 |
| 0x2D | RAW14 | 56 | 4 | 14 | 3,288 |
| 0x18 | YUV420 8 bit | Odd line: 64 Even line: 64 | Odd line: 8 Even line: 4 | Odd line: 8 Even line: 8, 24 | 2,880 |
| 0x19 | YUV420 10 bit | Odd line: 40 Even line: 40 | Odd line: 4 Even line: 2 | Odd line: 10 Even line: 10, 30 | 2,304 |
| 0x1A | Legacy YUV420 8 bit | 48 | 4 | 8, 16 | 3,840 |
| 0x1C | YUV420 8 bit (CSPS) | Odd line: 64 Even line: 64 | Odd line: 8 Even line: 4 | Odd line: 8 Even line: 8, 24 | 2,880 |
| 0x1D | YUV420 10 bit (CSPS) | Odd line: 40 Even line: 40 | Odd line: 4 Even line: 2 | Odd line: 10 Even line: 10, 30 | 2,304 |
| 0x1E | YUV422 8 bit | 64 | 4 | 8, 24 | 2,880 |
| 0x1F | YUV422 10 bit | 40 | 2 | 10, 30 | 2,304 |
| 0x30 - 37 | User defined 8 bit | 64 | 8 | 8 | 5,760 |

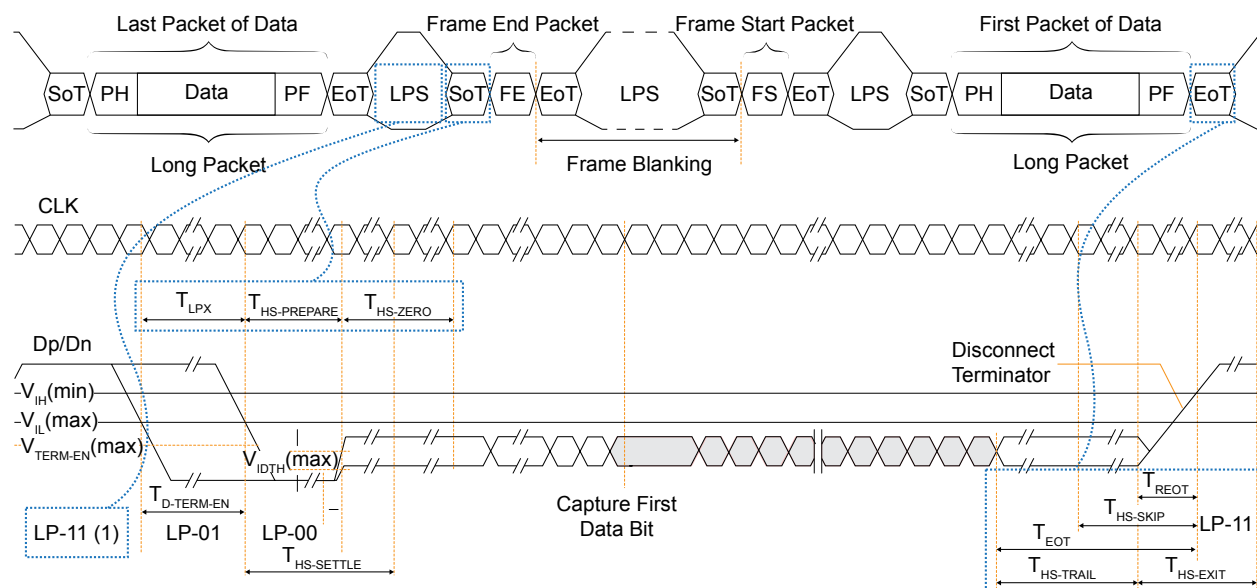
D-PHY Timing Parameters

During CSI-2 data transmission, the MIPI D-PHY alternates between low power mode and high-speed mode. The D-PHY specification defines timing parameters to facilitate the correct hand-shaking between the MIPI TX and MIPI RX during mode transitions.

You set the timing parameters to correspond to the specifications of your hardware in the Efinity® Interface Designer.

- *RX parameters*— $T_{CLK-SETTLE}$, $T_{HS-SETTLE}$ (see **Table 31: MIPI RX Control Signals (Interface to FPGA Fabric)** on page 32)
- *TX parameters*— $T_{CLK-POST}$, $T_{CLK-TRAIL}$, $T_{CLK-PREPARE}$, $T_{CLK-ZERO}$, $T_{CLK-PRE}$, $T_{HS-PREPARE}$, $T_{HS-ZERO}$, $T_{HS-TRAIL}$ (see **Table 29: MIPI TX Settings in Efinity Interface Designer** on page 29)

Figure 23: High-Speed Data Transmission in Bursts Waveform



Note:

1. To enter high-speed mode, the D-PHY goes through states LP-11, LP-01, and LP-00. The D-PHY generates LP-11 to exit high-speed mode.

Figure 24: Switching the Clock Lane between Clock Transmission and Low Power Mode Waveform

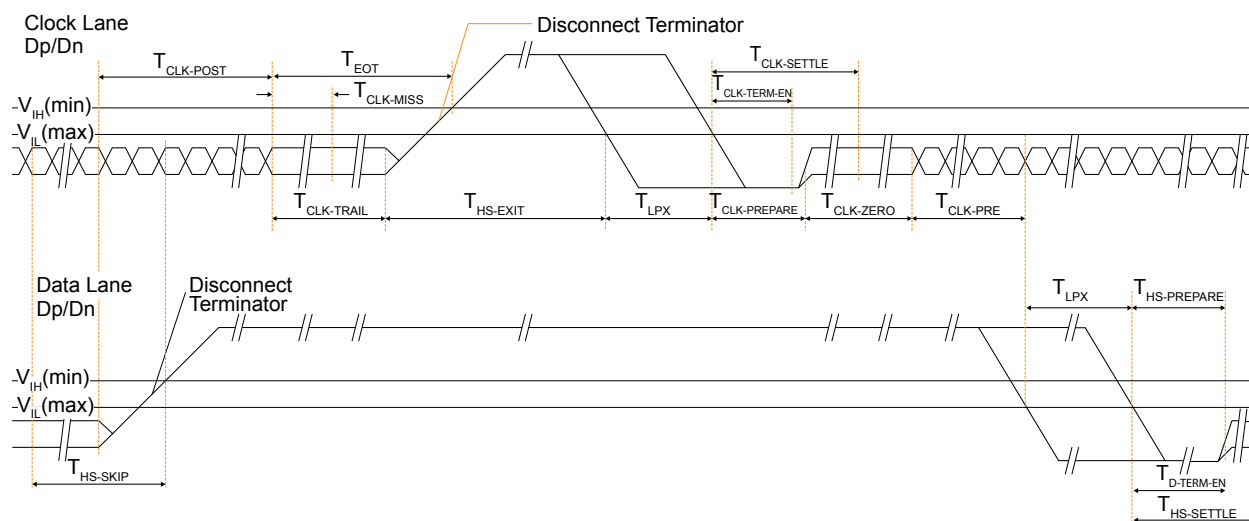


Table 38: D-PHY Timing Specifications

| Parameter | Description | Min | Typ | Max | Unit |
|----------------------------------|--|---|-----|-------------------------|------|
| $T_{CLK-POST}$ | Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$. | $60\text{ ns} + 52*UI$ | – | – | ns |
| $T_{CLK-PRE}$ | Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode. | 8 | – | – | UI |
| $T_{CLK-PREPARE}$ | Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission. | 38 | – | 95 | ns |
| $T_{CLK-SETTLE}$ | Time interval during which the HS receiver should ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PREPARE}$. | 95 | – | 300 | ns |
| $T_{CLK-TRAIL}$ | Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst. | 60 | – | – | ns |
| $T_{CLK-PREPARE} + T_{CLK-ZERO}$ | $T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock. | 300 | – | – | ns |
| $T_{HS-PREPARE}$ | Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission | $40\text{ ns} + 4*UI$ | – | $85\text{ ns} + 6*UI$ | ns |
| $T_{HS-SETTLE}$ | Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HS-PREPARE}$. The HS receiver shall ignore any Data Lane transitions before the minimum value, and the HS receiver shall respond to any Data Lane transitions after the maximum value. | $85\text{ ns} + 6*UI$ | – | $145\text{ ns} + 10*UI$ | ns |
| $T_{HS-TRAIL}$ | Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst. | $\max(n*8*UI, 60\text{ ns} + n*4*UI)^{(8)}$ | – | – | ns |
| T_{LPX} | Transmitted length of any Low-Power state period | 50 | – | – | ns |
| $T_{HS-PREPARE} + T_{HS-ZERO}$ | $T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence. | $145\text{ ns} + 10*UI$ | – | – | ns |

⁽⁸⁾ Where $n = 1$ in Forward-direction HS mode and $n = 4$ for Reverse-direction HS mode.

DDR DRAM

Some T35 FPGAs have a x16 DDR PHY interface supporting DDR3, DDR3L, LPDDR3, and LPDDR2 as well as a memory controller hard IP block. The DDR PHY supports data rates up to 1066 Mbps per lane. The memory controller provides two 128 bit AXI buses to communicate with the FPGA core.

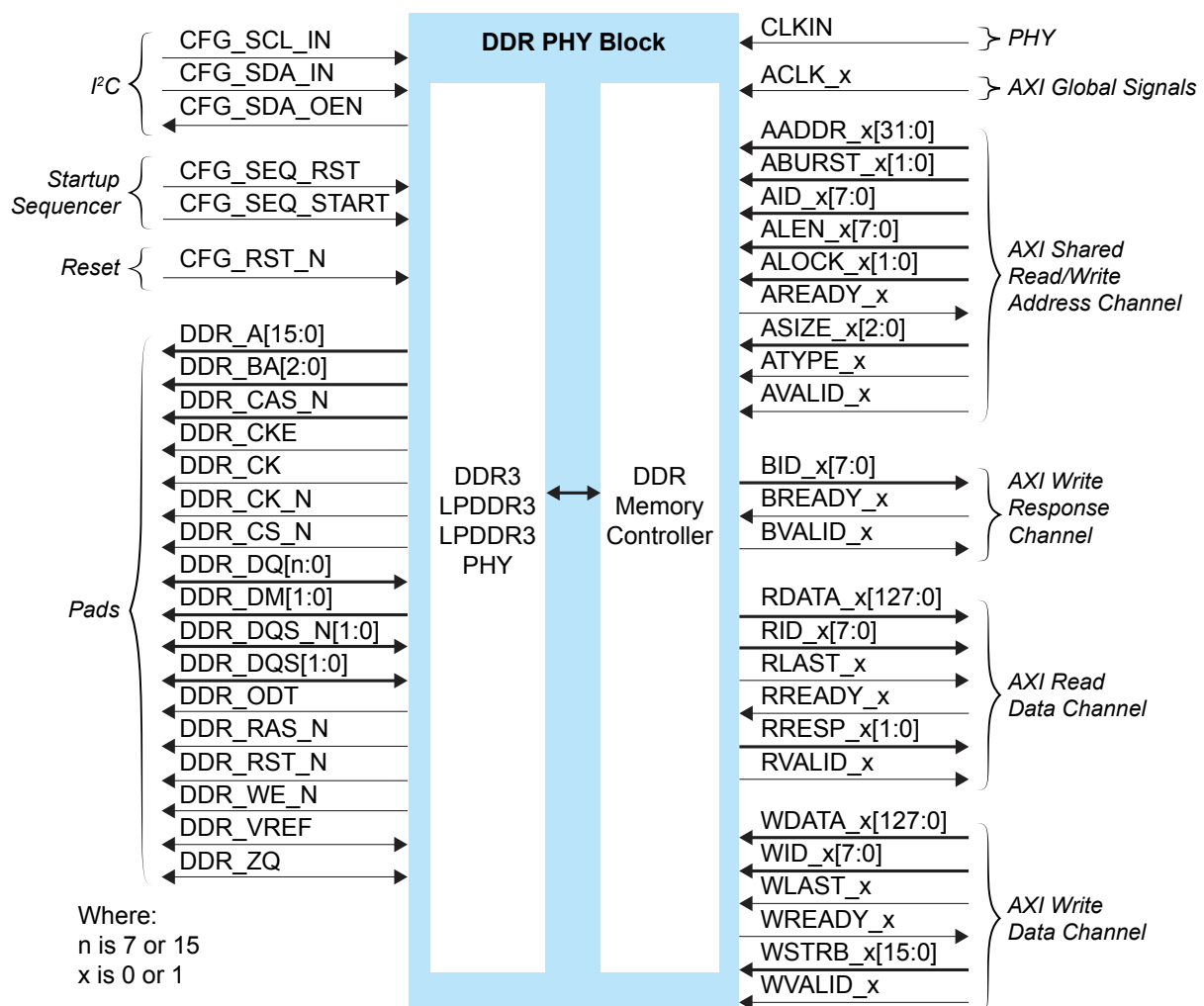


Note: The DDR PHY and controller are hard blocks; you cannot bypass the DDR DRAM memory controller to access the PHY directly for non-DDR memory controller applications.

Table 39: DDR DRAM Performance

| DDR DRAM Interface | Voltage (V) | Maximum Data Rate (Mbps) per Lane |
|--------------------|-------------|-----------------------------------|
| DDR3 | 1.5 | 1066 |
| DDR3L | 1.35 | 1066 |
| LPDDR3 | 1.2 | 1066 |
| LPDDR2 | 1.2 | 1066 |

Figure 25: DDR DRAM Block Diagram



The DDR DRAM block supports an I²C calibration bus that can read/write the DDR configuration registers. You can use this bus to fine tune the DDR PHY for high performance.

Figure 26: DDR DRAM Interface Block Diagram

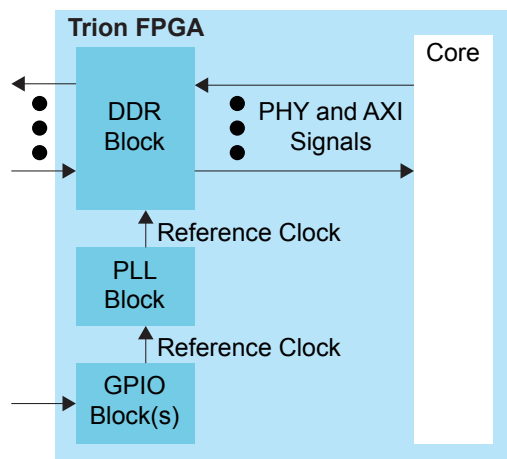


Table 40: PHY Signals (Interface to FPGA Fabric)

| Signal | Direction | Clock Domain | Description |
|--------|-----------|--------------|--|
| CLKIN | Input | N/A | High-speed clock to drive the DDR PHY. A PLL must generate this clock. The clock runs at half of the PHY data rate (for example, 800 Mbps requires a 400 MHz clock). The DDR DRAM block uses the PLL_BR0 CLKOUT0 resource as the PHY clock. |

The PLL reference clock must be driven by I/O pads. The Efinix[®] software issues a warning if you do not connect the reference clock to an I/O pad. (Using the clock tree may induce additional jitter and degrade the DDR performance.) Refer to [PLL](#) on page 16 for more information about the PLL block.



Important: Efinix strongly recommends that you do not use any LVDS pins (either single-ended I/O or differential pair) as the primary clock to drive the PLL_BR0 or the DDR interface will not be initialized during the configuration phase. Make sure to incorporate a user reset and instantiate the DDR Hard Memory Controller-Reset IP to initialize the DDR interface in user mode. Contact Efinix support if you need LVDS pins as the primary clock for the PLL_BR0 DDR interface

Table 41: AXI Global Signals (Interface to FPGA Fabric)

| Signal | Direction | Clock Domain | Description |
|----------------|-----------|--------------|-------------------|
| ACLK_0, ACLK_1 | Input | N/A | AXI clock inputs. |

Table 42: AXI Shared Read/Write Signals (Interface to FPGA Fabric)

| Signal x is 0 or 1 | Direction | Clock Domain | Description |
|-----------------------|-----------|-----------------|---|
| AADDR_x[31:0] | Input | ACLK_x | Address. ATYPE defines whether it is a read or write address. It gives the address of the first transfer in a burst transaction. |
| ABURST_x[1:0] | Input | ACLK_x | Burst type. The burst type and the size determine how the address for each transfer within the burst is calculated. |
| AID_x[7:0] | Input | ACLK_x | Address ID. This signal identifies the group of address signals. Depends on ATYPE, the ID can be for a read or write address group. |
| ALEN_x[7:0] | Input | ACLK_x | Burst length. This signal indicates the number of transfers in a burst. |
| ALOCK_x[1:0] | Input | ACLK_x | Lock type. This signal provides additional information about the atomic characteristics of the transfer. |
| AREADY_x | Output | ACLK_x | Address ready. This signal indicates that the slave is ready to accept an address and associated control signals. |
| ASIZE_x[2:0] | Input | ACLK_x | Burst size. This signal indicates the size of each transfer in the burst. |
| ATYPE_x | Input | ACLK_x | This signal distinguishes whether it is a read or write operation. 0 = read and 1 = write. |
| AVALID_x | Input | ACLK_x | Address valid. This signal indicates that the channel is signaling valid address and control information. |

Table 43: AXI Write Response Channel Signals (Interface to FPGA Fabric)

| Signal x is 0 or 1 | Direction | Clock Domain | Description |
|-----------------------|-----------|-----------------|---|
| BID_x[7:0] | Output | ACLK_x | Response ID tag. This signal is the ID tag of the write response. |
| BREADY_x | Input | ACLK_x | Response ready. This signal indicates that the master can accept a write response. |
| BVALID_x | Output | ACLK_x | Write response valid. This signal indicates that the channel is signaling a valid write response. |

Table 44: AXI Read Data Channel Signals (Interface to FPGA Fabric)

| Signal x is 0 or 1 | Direction | Clock Domain | Description |
|-----------------------|-----------|-----------------|---|
| RDATA_x[127:0] | Output | ACLK_x | Read data. |
| RID_x[7:0] | Output | ACLK_x | Read ID tag. This signal is the identification tag for the read data group of signals generated by the slave. |
| RLAST_x | Output | ACLK_x | Read last. This signal indicates the last transfer in a read burst. |
| RREADY_x | Input | ACLK_x | Read ready. This signal indicates that the master can accept the read data and response information. |
| RRESP_x[1:0] | Output | ACLK_x | Read response. This signal indicates the status of the read transfer. |
| RVALID_x | Output | ACLK_x | Read valid. This signal indicates that the channel is signaling the required read data. |

Table 45: AXI Write Data Channel Signals (Interface to FPGA Fabric)

| Signal x is 0 or 1 | Direction | Clock Domain | Description |
|-----------------------|-----------|-----------------|---|
| WDATA_x[127:0] | Input | ACLK_x | Write data. |
| WID_x[7:0] | Input | ACLK_x | Write ID tag. This signal is the ID tag of the write data transfer. |
| WLAST_x | Input | ACLK_x | Write last. This signal indicates the last transfer in a write burst. |
| WREADY_x | Output | ACLK_x | Write ready. This signal indicates that the slave can accept the write data. |
| WSTRB_x[15:0] | Input | ACLK_x | Write strobes. This signal indicates which byte lanes hold valid data. There is one write strobe bit for each eight bits of the write data bus. |
| WVALID_x | Input | ACLK_x | Write valid. This signal indicates that valid write data and strobes are available. |

Table 46: DDR DRAM I²C Interface Signals

| Signal | Direction | Description |
|-------------|-----------|--------------------|
| CFG_SCL_IN | Input | Clock input. |
| CFG_SDA_IN | Input | Data input. |
| CFG_SDA_OEN | Output | SDA output enable. |

Table 47: DDR DRAM Startup Sequencer Signals

| Signal | Direction | Description |
|---------------|-----------|---|
| CFG_SEQ_RST | Input | Active-high DDR configuration controller reset. |
| CFG_SEQ_START | Input | Start the DDR configuration controller. |

Table 48: DDR DRAM Reset Signal

| Signal | Direction | Description |
|-----------|-----------|--|
| CFG_RST_N | Input | Active-low master DDR DRAM reset. After you de-assert RST_N, you need to reconfigure and initialize before performing memory operations. |

Table 49: DDR DRAM Pads

| Signal | Direction | Description |
|----------------|---------------|---|
| DDR_A[15:0] | Output | Address signals to the memories. |
| DDR_BA[2:0] | Output | Bank signals to/from the memories. |
| DDR_CAS_N | Output | Active-low column address strobe signal to the memories. |
| DDR_CKE | Output | Active-high clock enable signals to the memories. |
| DDR_CK | Output | Active-high clock signals to/from the memories. The clock to the memories and to the memory controller must be the same clock frequency and phase. |
| DDR_CK_N | Output | Active-low clock signals to/from the memories. The clock to the memories and to the memory controller must be the same clock frequency and phase. |
| DDR_CS_N | Output | Active-low chip select signals to the memories. |
| DDR_DQ[n:0] | Bidirectional | Data bus to/from the memories. For writes, the pad drives these signals. For reads, the memory drives these signals. These signals are connected to the DQ inputs on the memories. <i>n</i> is 7 or 15 depending on the DQ Width Configuration setting. |
| DDR_DM[n] | Output | Active-high data-mask signals to the memories. <i>n</i> is 0 or 1:0 depending on the DQ width. |
| DDR_DQS_N[n:0] | Bidirectional | Differential data strobes to/from the memories. For writes, the pad drives these signals. For reads, the memory drives these signals. These signals are connected to the DQS inputs on the memories. <i>n</i> is 0 or 1:0 depending on the DQ width. |
| DDR_DQS[n:0] | Bidirectional | |
| DDR_ODT | Output | ODT signal to the memories. |
| DDR_RAS_N | Output | Active-low row address strobe signal to the memories. |
| DDR_RST_N | Output | Active-low reset signals to the memories. |
| DDR_WE_N | Output | Active-low write enable strobe signal to the memories. |
| DDR_VREF | Bidirectional | Reference voltage. |
| DDR_ZQ | Bidirectional | ZQ calibration pin. |

DDR Interface Designer Settings

The following tables describe the settings for the DDR block in the Interface Designer.

Table 50: Base Tab

| Parameter | Choices | Notes |
|---------------|----------------------|--|
| DDR Resource | None, DDR_0 | Only one resource available. |
| Instance Name | User defined | Indicate the DDR instance name. This name is the prefix for all DDR signals. |
| Memory Type | DDR3, LPDDR2, LPDDR3 | Choose the memory type you want to use. |

Table 51: Configuration Tab

| Parameter | Choices | Notes |
|---------------------------------|---------------------------------|---|
| Select Preset | | The Select Preset button opens a list of popular DDR memory configurations. Choose a preset to populate the configuration choices. If you do not want to use a preset, you can specify the memory configuration manually. |
| DQ Width | x8, x16 | DQ bus width. |
| Type | DDR3, LPDDR2, LPDDR3 | Memory type. |
| Enable Advanced Density Setting | On, Off | If you do not want to use the available density from the Density parameter, you can set the memory row and column width. |
| Row Width | 0 - 99 | Specify the memory row width. |
| Column Width | 0 - 99 | Specify the memory column width. |
| DDR3 | | |
| Speed Grade | 1066E, 1066F, 1066G, 800D, 800E | Memory speed. |
| Width | x8, x16 | Memory width. |
| Density | 1G, 2G, 4G, 8G | Memory density in bits. |
| LPDDR2 | | |
| Speed Grade | 400, 533, 667, 800, 1066 | Memory speed. |
| Width | x16 | Memory width. |
| Density | 256M, 512M, 1G, 2G, 4G | Memory density in bits. |
| LPDDR3 | | |
| Speed Grade | 800, 1066 | Memory speed. |
| Width | x16 | Memory width. |
| Density | 4G, 8G | Memory density in bits. |

Table 52: Advanced Options Tab - FPGA Setting Subtab

| Parameter | Choices | Notes |
|-------------------------|-------------------------------------|---|
| FPGA Input Termination | Varies depending on the memory type | Specify the termination value for the FPGA input/output pins. |
| FPGA Output Termination | | |

Table 53: Advanced Options Tab - Memory Mode Register Settings Subtab

| Parameter | Choices | Notes |
|-------------------------------------|---|---|
| DDR3 | | |
| Burst Length | 8 | Specify the burst length (only 8 is supported). |
| DLL Precharge Power Down | On, Off | Specify whether the DLL in the memory device is off or on during precharge power-down. |
| Memory Auto Self-Refresh | Auto, Manual | Turn on or off auto-self refresh feature in memory device. |
| Memory CAS Latency (CL) | 5 - 14 | Specify the number of clock cycle between read command and the availability of output data at the memory device. |
| Memory Write CAS Latency (CWL) | 5 - 12 | Specify the number of clock cycle from the releasing of the internal write to the latching of the first data in at the memory device. |
| Memory Dynamic ODT (Rtt_WR) | Off, RZQ/2, RZQ/4 | Specify the mode of dynamic ODT feature of memory device. |
| Memory Input Termination (Rtt_nom) | Off, RZQ/2, RZQ/4, RZQ/6, RZQ/8, RZQ/12 | Specify the input termination value of the memory device. |
| Memory Output Termination | RZQ/6, RZQ/7 | Specify the output termination value of the memory device. |
| Read Burst Type | Interleaved, Sequential | Specify whether accesses within a give burst are in sequential or interleaved order. |
| Self-Refresh Temperature | Extended, Normal | Specify whether the self refresh temperature is normal or extended mode. |
| LPDDR2 | | |
| FPGA Input Termination (Ω) | 120, Off | Specify the input termination of the FPGA device. Used in non-JEDEC standard only. |
| Burst Length | 8 | Specify the burst length (only 8 is supported). |
| Output Drive Strength | 34.3, 40, 48, 60, 80, 120 | Specify the output termination value of memory device. |
| Read Burst Type | Interleaved, Sequential | Specify whether accesses within a given burst are in sequential or interleaved order. |
| Read/Write Latency | RL=3/WL=1, RL=4/WL=2 RL=5/WL=2, RL=6/WL=3 RL=7/WL=4, RL=8/WL=4 | Specify the read/write latency of the memory device. |
| LPDDR3 | | |
| DQ ODT | Disable, RZQ1, RZQ2, RZQ4 | Specify the input termination value of memory device. |
| Output Drive Strength | 34.3 34.3 pull-down/40 pull up 34.3 pull-down/48 pull up 40 40 pull down/48 pull up 48 | Specify the output termination value of memory device. |
| Read/Write Latency | RL=3/WL=1, RL=6/WL=3 RL=8/WL=4, RL=9/WL=5 | Specify the read/write latency of the memory device. |

Table 54: Advanced Options Tab - Memory Timing Settings Subtab

| Parameter | Choices | Notes |
|--|--------------|--|
| tFAW, Four Bank Active Window (ns) | User defined | Enter the timing parameters from the memory device's data sheet. |
| tRAS, Active to Precharge Command Period (ns) | | |
| tRC, Active to Active or REF Command Period (ns) | | |
| tRCD, Active to Read or Write Delay (ns) | | |
| tREFI, Average Periodic Refresh Interval (ns) | | |
| tRFC, Refresh to Active or Refresh to Refresh Delay (ns) | | |
| tRP, Precharge Command Period (ns) | | |
| tRRD, Active to Active Command Period (ns) | | |
| tRTP, Internal Read to Precharge Delay (ns) | | |
| tWTR, Internal Write to Read Command Delay (ns) | | |

Table 55: Advanced Options Tab - Controller Settings Subtab

| Parameter | Choices | Notes |
|--------------------------------------|---|--|
| Controller to Memory Address Mapping | BANK-ROW-COL ROW-BANK-COL ROW-COL_HIGH-BANK-COL_LOW | Specify the mapping between the address of AXI interface and column, row, and bank address of memory device. |
| Enable Auto Power Down | Active, Off, Pre-Charge | Specify whether to allow automatic entry into power-down mode (pre-charge or active) after a specific amount of idle time. |
| Enable Self Refresh Controls | No, Yes | Specify whether to enable automatic entry into self-refresh mode after specific amount of idle period. |

Table 56: Advanced Options Tab - Gate Delay Tuning Settings Subtab

| Parameter | Choices | Notes |
|----------------------------|-----------|---|
| Enable Gate Delay Override | On or off | Turning this option on allows you to fine-tune the gate-delay values. This is an expert only setting. |
| Gate Coarse Delay Tuning | 0 - 5 | |
| Gate Fine Delay Tuning | 0 - 255 | |

Table 57: Control Tab

| Option | Notes |
|------------------------------|---|
| Disable Control | When selected, this option disables calibration and user reset. |
| Enable Calibration | Turn on to enable optional PHY calibration pins (master reset, SCL, and SDA pins). Efinix recommends that you use the default pin names. The names are prefixed with the instance name you specified in the Base tab. These pins connect to the DDR Hard Memory Controller - Calibration and Reset IP core. |
| Enable User Reset | Turn on to enable optional reset pins (master reset and sequencer start/reset). Efinix recommends that you use the default pin names. The names are prefixed with the instance name you specified in the Base tab. These pins connect to the DDR Hard Memory Controller - Reset IP core. |
| Enable Reset and Calibration | Turn on to enable the pins for calibration and user reset. These pins connect to the DDR Hard Memory Controller - Calibration and Reset IP core. |

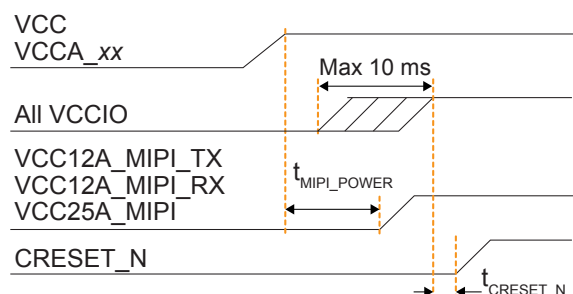
Table 58: AXI 0 and AXI 1 Tabs

| Parameter | Choices | Notes |
|--|--------------|---|
| Enable Target 0 Enable Target 1 | On or off | Turn on to enable the AXI 0 interface. Turn on to enable the AXI 1 interface. |
| AXI Clock Input Pin name | User defined | Specify the name of the AXI input clock pin. |
| Invert AXI Clock Input | On or off | Turn on to invert the AXI clock. |
| Shared Read/Write Address Channel tab Write Response Channel tab Read Data Channel tab Write Data Channel tab | User defined | This tab defines the AXI signal names. Efinix recommends that you use the default names. The signals are prefixed with the instance name you specified in the Base tab. |

Power Up Sequence

Efnix® recommends the following power up sequence when powering Trion® FPGAs:

Figure 27: Trion® FPGAs Power Up Sequence



1. Power up VCC and VCCA_xx first.
2. When VCC and VCCA_xx are stable, power up all VCCIO pins. There is no specific timing delay between the VCCIO pins.
3. Apply power to VCC12A_MIPI_TX, VCC12A_MIPI_RX, and VCC25A_MIPI at least $t_{\text{MIPI_POWER}}$ after VCC is stable.



Important: Ensure the power ramp rate is within VCCIO/10 V/ms to 10 V/ms.

4. After all power supplies are stable, hold CRESET_N low for a duration of $t_{\text{CRESET_N}}$ before asserting CRESET_N from low to high to trigger active SPI programming (the FPGA loads the configuration data from an external flash device).

When you are not using the GPIO, MIPI, DDR or PLL resources, connect the pins as shown in the following table.

Table 59: Connection Requirements for Unused Resources

| Unused Resource | Pin | Note |
|-----------------|----------------|---|
| GPIO Bank | VCCIOxx | Connect to either 1.8 V, 2.5 V, or 3.3 V. |
| PLL | VCCA_PLL | Connect to VCC (1.2 V). |
| MIPI | VCC12A_MIPI_TX | Connect to VCC (1.2 V). |
| | VCC12A_MIPI_RX | Connect to VCC (1.2 V). |
| | VCC25A_MIPI | Connect to VCC (1.2 V). |
| DDR | VCCIO_DDR | Floating. Leave unconnected. |
| | DDR_VREF | Connect to ground. |



Learn more: Refer to [Trion Hardware Design Checklist and Guidelines](#) for connection requirements for unused resources.



Note: Refer to [Configuration Timing](#) and [MIPI Power-Up Timing](#) on page 60 for timing information.

Power Supply Current Transient

You may observe an inrush current on the dedicated power rail during power-up. You must ensure that the power supplies selected in your board meets the current requirement during power-up and the estimated current during user mode. Use the Power Estimator to calculate the estimated current during user mode.

Table 60: Maximum Power Supply Current Transient

| Power Supply | Maximum Power Supply Current Transient ⁽⁹⁾⁽¹⁰⁾ | Unit |
|--------------|---|------|
| VCC | 57 | mA |

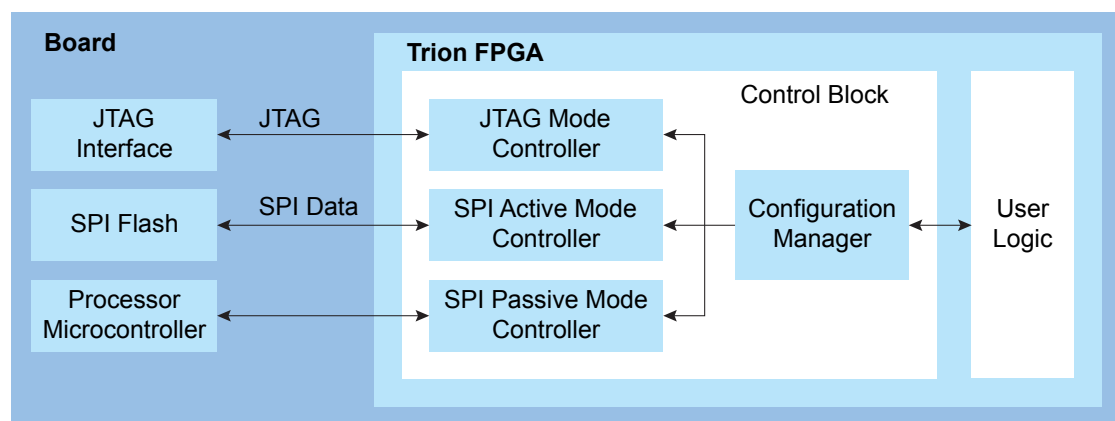
Configuration

The T35 FPGA contains volatile Configuration RAM (CRAM). The user must configure the CRAM for the desired logic function upon power-up and before the FPGA enters normal operation. The FPGA's control block manages the configuration process and uses a bitstream to program the CRAM. The Efinity[®] software generates the bitstream, which is design dependent. You can configure the T35 FPGA(s) in SPI active, SPI passive, or JTAG mode.



Learn more: Refer to [AN 006: Configuring Trion FPGAs](#) for details on the dedicated configuration pins and how to configure FPGA(s).

Figure 28: High-Level Configuration Options



In active mode, the FPGA controls the configuration process. An oscillator circuit within the FPGA provides the configuration clock. The bitstream is typically stored in an external serial flash device, which provides the bitstream when the FPGA requests it.

The control block sends out the instruction and address to read the configuration data. First, it issues a release from power-down instruction to wake up the external SPI flash. Then, it waits for at least 30 μ s before issuing a fast read command to read the content of SPI flash from address 24h'000000.

⁽⁹⁾ Inrush current for other power rails are not significant in Trion[®] FPGAs.

⁽¹⁰⁾ Measured at room temperature.

In passive mode, the FPGA is the slave and relies on an external master to provide the control, bitstream, and clock for configuration. Typically the master is a microcontroller or another FPGA in active mode.

In JTAG mode, you configure the FPGA via the JTAG interface.

Supported Configuration Modes

Table 61: T35 Configuration Modes by Package

| Configuration Mode | Width | BGA256 | BGA324, BGA400 |
|--------------------|-------|--------|-------------------|
| Active | x1 | ✓ | ✓ ⁽¹¹⁾ |
| | x2 | ✓ | ✓ |
| | x4 | ✓ | ✓ |
| Passive | x1 | ✓ | ✓ |
| | x2 | ✓ | ✓ |
| | x4 | ✓ | ✓ |
| | x8 | ✓ | ✓ |
| | x16 | ✓ | ✓ |
| | x32 | - | ✓ |
| JTAG | x1 | ✓ | ✓ |



Learn more: Refer to [AN 006: Configuring Trion FPGAs](#) for more information.

⁽¹¹⁾ These packages do not support active SPI multi-image configuration in x1 mode. Instead, use x2 or x4, or alternatively, use the internal reconfiguration feature as described in AN 010: Using the Internal Reconfiguration Feature to Remotely Update Trion FPGAs.

DC and Switching Characteristics

Table 62: Absolute Maximum Ratings

Conditions beyond those listed may cause permanent damage to the device. Device operation at the absolute maximum ratings for extended periods of time has adverse effects on the device.

| Symbol | Description | Min | Max | Units |
|------------------------------------|--|------|------|-------|
| VCC | Core power supply | -0.5 | 1.42 | V |
| VCCIO | I/O bank power supply | -0.5 | 4.6 | V |
| VCCA_PLL | PLL analog power supply | -0.5 | 1.42 | V |
| VCCIO_DDR | DDR power supply | -0.5 | 1.65 | V |
| VCC25A_MIP10 VCC25A_MIP11 | 2.5 V analog power supply for MIPI | -0.5 | 2.75 | V |
| VCC12A_MIP10_TX VCC12A_MIP11_TX | 1.2 V TX analog power supply for MIPI | -0.5 | 1.42 | V |
| VCC12A_MIP10_RX VCC12A_MIP11_RX | 1.2 V RX analog power supply for MIPI | -0.5 | 1.42 | V |
| V _{IN} | I/O input voltage | -0.5 | 4.6 | V |
| I _{IN} | Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode. ⁽¹³⁾ | - | 10 | mA |
| T _J | Operating junction temperature | -40 | 125 | °C |
| T _{STG} | Storage temperature, ambient | -55 | 150 | °C |

⁽¹²⁾ Supply voltage specification applied to the voltage taken at the device pins with respect to ground, not at the power supply.

⁽¹³⁾ Should not exceed a total of 120 mA per bank.

Table 63: Recommended Operating Conditions (C3, C4, and I4 Speed Grades)⁽¹²⁾

| Symbol | Description | Min | Typ | Max | Units |
|------------------------------------|--|-------|------|----------------|-------|
| VCC | Core power supply | 1.15 | 1.2 | 1.25 | V |
| VCCIO | 1.8 V I/O bank power supply | 1.71 | 1.8 | 1.89 | V |
| | 2.5 V I/O bank power supply | 2.38 | 2.5 | 2.63 | V |
| | 3.3 V I/O bank power supply | 3.14 | 3.3 | 3.47 | V |
| VCCIO_DDR | DDR3 | 1.425 | 1.5 | 1.575 | V |
| | DDR3L | 1.283 | 1.35 | 1.45 | V |
| | LPDDR3 | 1.14 | 1.2 | 1.3 | V |
| | LPDDR2 | 1.14 | 1.2 | 1.3 | V |
| VCCA_PLL | PLL analog power supply | 1.15 | 1.2 | 1.25 | V |
| VCC25A_MIP10 VCC25A_MIP11 | 2.5 V analog power supply for MIPI | 2.38 | 2.5 | 2.63 | V |
| VCC12A_MIP10_TX VCC12A_MIP11_TX | 1.2 V TX analog power supply for MIPI | 1.15 | 1.2 | 1.25 | V |
| VCC12A_MIP10_RX VCC12A_MIP11_RX | 1.2 V RX analog power supply for MIPI | 1.15 | 1.2 | 1.25 | V |
| V _{IN} | I/O input voltage ⁽¹⁴⁾ | -0.3 | - | VCCIO + 0.3 | V |
| T _{JCOM} | Operating junction temperature, commercial | 0 | - | 85 | °C |
| T _{JIND} | Operating junction temperature, industrial | -40 | - | 100 | °C |

⁽¹⁴⁾ Values applicable to both input and tri-stated output configuration.

Table 64: Recommended Operating Conditions (C4L and I4L Speed Grades) ⁽¹²⁾

| Symbol | Description | Min | Typ | Max | Units |
|------------------------------------|--|-------|------|----------------|-------|
| VCC | Core power supply | 1.05 | 1.1 | 1.15 | V |
| VCCIO | 1.8 V I/O bank power supply | 1.71 | 1.8 | 1.89 | V |
| | 2.5 V I/O bank power supply | 2.38 | 2.5 | 2.63 | V |
| | 3.3 V I/O bank power supply | 3.14 | 3.3 | 3.47 | V |
| VCCIO_DDR | DDR3 | 1.425 | 1.5 | 1.575 | V |
| | DDR3L | 1.283 | 1.35 | 1.45 | V |
| | LPDDR3 | 1.14 | 1.2 | 1.3 | V |
| | LPDDR2 | 1.14 | 1.2 | 1.3 | V |
| VCCA_PLL | PLL analog power supply | 1.05 | 1.1 | 1.15 | V |
| VCC25A_MIP10 VCC25A_MIP11 | 2.5 V analog power supply for MIPI | 2.38 | 2.5 | 2.63 | V |
| VCC12A_MIP10_TX VCC12A_MIP11_TX | 1.2 V TX analog power supply for MIPI | 1.05 | 1.1 | 1.15 | V |
| VCC12A_MIP10_RX VCC12A_MIP11_RX | 1.2 V RX analog power supply for MIPI | 1.05 | 1.1 | 1.15 | V |
| V _{IN} | I/O input voltage ⁽¹⁵⁾ | -0.3 | - | VCCIO + 0.3 | V |
| T _{JCOM} | Operating junction temperature, commercial | 0 | - | 85 | °C |
| T _{JIND} | Operating junction temperature, industrial | -40 | - | 100 | °C |

Table 65: Power Supply Ramp Rates

| Symbol | Description | Min | Max | Units |
|-------------------|--|----------|-----|-------|
| t _{RAMP} | Power supply ramp rate for all supplies. | VCCIO/10 | 10 | V/ms |

⁽¹⁵⁾ Values applicable to both input and tri-stated output configuration.

Table 66: Single-Ended I/O DC Electrical Characteristics

| I/O Standard | V _{IL} (V) | | V _{IH} (V) | | V _{OL} (V) | V _{OH} (V) |
|--------------|---------------------|--------------|---------------------|-------------|---------------------|---------------------|
| | Min | Max | Min | Max | Max | Min |
| 3.3 V LVCMOS | -0.3 | 0.8 | 2 | VCCIO + 0.3 | 0.2 | VCCIO - 0.2 |
| 3.3 V LVTTTL | -0.3 | 0.8 | 2 | VCCIO + 0.3 | 0.4 | 2.4 |
| 2.5 V LVCMOS | -0.3 | 0.7 | 1.7 | VCCIO + 0.3 | 0.5 | 1.8 |
| 1.8 V LVCMOS | -0.3 | 0.35 * VCCIO | 0.65 * VCCIO | VCCIO + 0.3 | 0.45 | VCCIO - 0.45 |

Table 67: Single-Ended I/O and Dedicated Configuration Pins Schmitt Trigger Buffer Characteristic

| Voltage (V) | VT+ (V) Schmitt Trigger Low-to-High Threshold | VT- (V) Schmitt Trigger High-to-Low Threshold | Input Leakage Current (μA) | Tri-State Output Leakage Current (μA) |
|-------------|---|---|----------------------------|---------------------------------------|
| 3.3 | 1.73 | 1.32 | ±10 | ±10 |
| 2.5 | 1.37 | 1.01 | ±10 | ±10 |
| 1.8 | 1.05 | 0.71 | ±10 | ±10 |

Table 68: Single-Ended I/O Buffer Drive Strength Characteristics

Junction temperature at T_J = 25 °C, power supply at nominal voltage.

CDONE has a drive strength of 1.

| I/O Standard | 3.3 V | | 2.5 V | | 1.8 V | |
|----------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|
| Drive Strength | I _{OH} (mA) | I _{OL} (mA) | I _{OH} (mA) | I _{OL} (mA) | I _{OH} (mA) | I _{OL} (mA) |
| 1 | 14.4 | 8.0 | 9.1 | 8.0 | 5.1 | 4.4 |
| 2 | 19.1 | 10.5 | 12.2 | 10.5 | 6.8 | 5.8 |
| 3 | 23.9 | 13.3 | 15.2 | 13.4 | 8.6 | 7.3 |
| 4 | 28.7 | 15.8 | 18.2 | 15.9 | 10.3 | 8.6 |

Table 69: Single-Ended I/O Internal Weak Pull-Up and Pull-Down Resistance

CDONE and CRESET_N also have an internal weak pull-up with these values.

| I/O Standard | Internal Pull-Up | | | Internal Pull-Down | | | Units |
|---------------------|------------------|-----|-----|--------------------|-----|-----|-------|
| | Min | Typ | Max | Min | Typ | Max | |
| 3.3 V LVTTTL/LVCMOS | 27 | 40 | 65 | 30 | 47 | 83 | kΩ |
| 2.5 V LVCMOS | 35 | 55 | 120 | 37 | 62 | 118 | kΩ |
| 1.8 V LVCMOS | 70 | 90 | 200 | 80 | 99 | 300 | kΩ |

Table 70: LVDS Pins Configured as Single-Ended I/O DC Electrical Characteristics

| I/O Standard | V _{IL} (V) | | V _{IH} (V) | | V _{OL} (V) | V _{OH} (V) |
|--------------|---------------------|--------------|---------------------|-------------|---------------------|---------------------|
| | Min | Max | Min | Max | Max | Min |
| 3.3 V LVCMOS | -0.3 | 0.8 | 2 | VCCIO + 0.3 | 0.2 | VCCIO - 0.2 |
| 3.3 V LVTTTL | -0.3 | 0.8 | 2 | VCCIO + 0.3 | 0.4 | 2.4 |
| 2.5 V LVCMOS | -0.3 | 0.7 | 1.7 | VCCIO + 0.3 | 0.5 | 1.8 |
| 1.8 V LVCMOS | -0.3 | 0.35 * VCCIO | 0.65 * VCCIO | VCCIO + 0.3 | 0.45 | VCCIO - 0.45 |

Table 71: LVDS Pins Configured as Single-Ended I/O DC Electrical Characteristics

| Voltage (V) | Input Leakage Current (μA) | Tri-State Output Leakage Current (μA) |
|-------------|----------------------------|---------------------------------------|
| 3.3 | ±10 | ±10 |

Table 72: LVDS Pins Configured as Single-Ended I/O Buffer Drive Strength Characteristics

Junction temperature at T_J = 25 °C, power supply at nominal voltage.

| I/O Standard | 3.3 V | | 2.5 V | | 1.8 V | |
|----------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|
| Drive Strength | I _{OH} (mA) | I _{OL} (mA) | I _{OH} (mA) | I _{OL} (mA) | I _{OH} (mA) | I _{OL} (mA) |
| 1 | 14.4 | 8.0 | 9.1 | 8.0 | 5.1 | 4.4 |
| 2 | 19.1 | 10.5 | 12.2 | 10.5 | 6.8 | 5.8 |
| 3 | 23.9 | 13.3 | 15.2 | 13.4 | 8.6 | 7.3 |
| 4 | 28.7 | 15.8 | 18.2 | 15.9 | 10.3 | 8.6 |

Table 73: LVDS Pins Configured as Single-Ended I/O Internal Weak Pull-Up Resistance

| I/O Standard | Internal Pull-Up | | | Units |
|---------------------|------------------|-----|-----|-------|
| | Min | Typ | Max | |
| 3.3 V LVTTTL/LVCMOS | 27 | 40 | 65 | kΩ |
| 2.5 V LVCMOS | 35 | 55 | 95 | kΩ |
| 1.8 V LVCMOS | 53 | 90 | 167 | kΩ |

Table 74: Single-Ended I/O and LVDS Pins Configured as Single-Ended I/O Rise and Fall Time

Data are based on the following IBIS simulation setup:

- Weakest drive strength model
- Typical simulation corner setting
- RLC circuit with 6.6 pF capacitance, 16.6 nH inductance, 0.095 ohm resistance, and 25 °C temperature



Note: For a more accurate data, you need to perform the simulation with your own circuit.

| I/O Standard | Rise Time (T_R) | | Fall Time (T_F) | | Units |
|---|------------------------|-------------------------|------------------------|-------------------------|-------|
| | Slow Slew Rate Enabled | Slow Slew Rate Disabled | Slow Slew Rate Enabled | Slow Slew Rate Disabled | |
| 3.3 V LVTTTL/LVCMOS | 1.13 | 1.02 | 1.24 | 1.17 | ns |
| 2.5 V LVCMOS | 1.4 | 1.3 | 1.44 | 1.31 | ns |
| 1.8 V LVCMOS | 2.14 | 2.01 | 2.05 | 1.85 | ns |
| LVDS pins configured as 3.3 V LVTTTL/LVCMOS | 0.45 | | 0.44 | | ns |

Table 75: Maximum Toggle Rate

Efinix recommends that you perform simulations using the IBIS model to determine the maximum toggle rate for your design.

| I/O Standard | Max Toggle Rate | Units |
|---------------------|-----------------|-------|
| 3.3 V LVTTTL/LVCMOS | 400 | Mbps |
| 2.5 V LVCMOS | 400 | Mbps |
| 1.8 V LVCMOS | 400 | Mbps |
| LVDS | 800 | Mbps |

Table 76: Block RAM Characteristics

| Symbol | Description | Speed Grade | | Units |
|-----------|------------------------------|--------------|--------|-------|
| | | C3, C4L, I4L | C4, I4 | |
| f_{MAX} | Block RAM maximum frequency. | 310 | 400 | MHz |

Table 77: Multiplier Block Characteristics

| Symbol | Description | Speed Grade | | Units |
|-----------|-------------------------------------|--------------|--------|-------|
| | | C3, C4L, I4L | C4, I4 | |
| f_{MAX} | Multiplier block maximum frequency. | 310 | 400 | MHz |

LVDS I/O Electrical and Timing Specifications

The LVDS pins comply with the EIA/TIA-644 electrical specifications.



Note: The LVDS RX supports the sub-lvds, slvs, HiVcm, RSDS and 3.3 V LVPECL differential I/O standards with a transfer rate of up to 800 Mbps.

Table 78: LVDS I/O Electrical Specifications

| Parameter | Description | Test Conditions/ Options | Min | Typ | Max | Unit |
|------------------|------------------------------|-------------------------------------|-------|-------|-------|---------|
| V_{CCIO} | LVDS I/O Supply Voltage | - | 2.97 | 3.3 | 3.63 | V |
| LVDS TX | | | | | | |
| V_{OD} | Output Differential Voltage | Reduce VOD Swing option disabled | 250 | 350 | 450 | mV |
| | | Reduce VOD Swing option enabled | 150 | 200 | 250 | mV |
| ΔV_{OD} | Change in V_{OD} | - | - | - | 50 | mV |
| V_{OCM} | Output Common Mode Voltage | $RT = 100\ \Omega$ | 1,125 | 1,250 | 1,375 | mV |
| ΔV_{OCM} | Change in V_{OCM} | - | - | - | 50 | mV |
| V_{OH} | Output High Voltage | $RT = 100\ \Omega$ | - | - | 1,600 | mV |
| V_{OL} | Output Low Voltage | $RT = 100\ \Omega$ | 900 | - | - | mV |
| I_{SAB} | Output Short Circuit Current | - | - | - | 24 | mA |
| LVDS RX | | | | | | |
| V_{ID} | Input Differential Voltage | - | 100 | - | 600 | mV |
| V_{ICM} | Input Common Mode Voltage | - | 100 | - | 2,000 | mV |
| V_{TH} | Differential Input Threshold | - | -100 | - | 100 | mV |
| I_{IL} | Input Leakage Current | - | - | - | 20 | μA |

Figure 29: LVDS RX I/O Electrical Specification Waveform

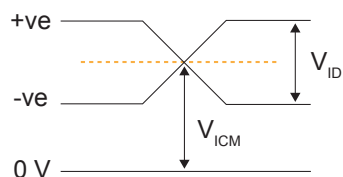
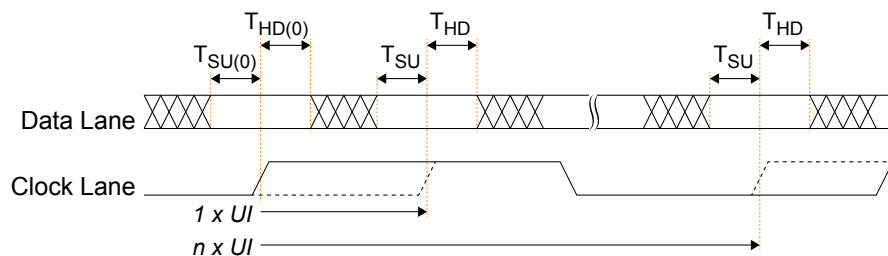
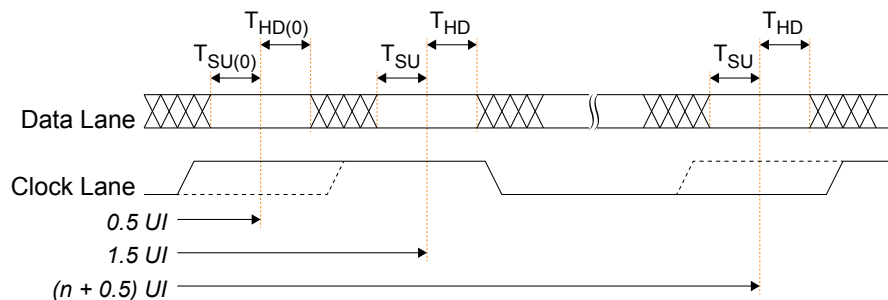


Table 79: LVDS Timing Specifications

| Parameter | Description | Min | Typ | Max | Unit |
|------------------|--|-----|-----|-----|------|
| t_{LVDS_CPA} | LVDS TX reference clock phase accuracy | -5 | - | +5 | % |
| t_{LVDS_skew} | LVDS TX lane-to-lane skew (edge-aligned) | - | - | 200 | ps |
| | LVDS TX lane-to-lane skew (center-aligned) | - | - | 250 | ps |
| t_{LVDS_SU} | LVDS RX Data to CLK setup time | 344 | - | - | ps |
| t_{LVDS_HD} | LVDS RX Data to CLK hold time | 344 | - | - | ps |

Figure 30: LVDS RX Timing (Center-Aligned)**Figure 31: LVDS RX Timing (Edge-Aligned)**

ESD Performance

Refer to the [Trion Reliability Report](#) for ESD performance data.

MIPI Electrical Specifications and Timing



Important: All specifications are preliminary and pending hardware characterization.

The MIPI D-PHY transmitter and receiver are compliant to the MIPI Alliance Specification for D-PHY Revision 1.1.

Table 80: High-Speed MIPI D-PHY Transmitter (TX) DC Specifications

| Parameter | Description | Min | Typ | Max | Unit |
|--------------------------|---|-----|-----|-----|----------|
| V_{CMTX} | High-speed transmit static common-mode voltage | 150 | 200 | 250 | mV |
| $ \Delta V_{CMTX(1,0)} $ | V_{CMTX} mismatch when output is Differential-1 or Differential-0 | - | - | 5 | mV |
| $ V_{OD} $ | High-speed transmit differential voltage | 140 | 200 | 270 | mV |
| $ \Delta V_{OD} $ | V_{OD} mismatch when output is Differential-1 or Differential-0 | - | - | 14 | mV |
| V_{OHHS} | High-speed output high voltage | - | - | 360 | mV |
| Z_{OS} | Single ended output impedance | 40 | 50 | 60 | Ω |
| ΔZ_{OS} | Single ended output impedance mismatch | - | - | 20 | % |

Table 81: High-Speed MIPI D-PHY Transmitter (TX) AC Specifications

| Parameter | Description | Min | Typ | Max | Unit |
|-----------------------|---|-----|-----|------|--------------------|
| $\Delta V_{CMTX(HF)}$ | Common-level variations above 450 MHz | - | - | 15 | mV _{RMS} |
| $\Delta V_{CMTX(LF)}$ | Common-level variations between 50 to 450 MHz | - | - | 25 | mV _{PEAK} |
| t_R and t_F | Rise and fall time < 1.0Gbps | - | - | 0.3 | UI |
| | Rise and fall time > 1.0Gbps | - | - | 0.35 | UI |
| | Rise and fall time > 1.5Gbps | - | - | 0.4 | UI |

Table 82: Low-Power MIPI D-PHY Transmitter (TX) DC Specifications

| Parameter | Description | Min | Typ | Max | Unit |
|-----------|---|------|-----|-----|----------|
| V_{OH} | Thevenin output high level | 0.95 | 1.2 | 1.3 | V |
| V_{OL} | Thevenin output low level | -50 | - | 50 | mV |
| Z_{OLP} | Output impedance of low-power transmitter | 110 | - | - | Ω |

Table 83: Low-Power MIPI D-PHY Transmitter (TX) AC Specifications

| Parameter | Description | Min | Typ | Max | Unit |
|--------------------------|---|-----|-----|-----|-------|
| T_{RLP}/T_{FLP} | 15%-85% rise time and fall time | - | - | 25 | ns |
| T_{REOT} | 30%-85% rise time and fall time | - | - | 35 | ns |
| $T_{LP-PULSE-TX}$ | Pulse width of first LP exclusive-OR clock pulse after Stop state or last pulse before Stop state | 40 | - | - | ns |
| | Pulse width of all other pulses | - | 20 | - | ns |
| $T_{LP-PER-TX}$ | Period of the LP exclusive-OR clock | 90 | - | - | ns |
| $\delta V/\delta t_{SR}$ | Slew rate @ $C_{LOAD} = 50\text{pF} < 1.5\text{ Gbps}$ | 30 | - | 150 | mV/ns |
| | Slew rate @ $C_{LOAD} = 50\text{pF} > 1.5\text{ Gbps}$ | 25 | - | 150 | mV/ns |

Table 84: High-Speed MIPI D-PHY Receiver (RX) DC Specifications

| Parameter | Description | Min | Typ | Max | Unit |
|----------------|---|-----|-----|-----|----------|
| $V_{CMRX(DC)}$ | Common mode voltage high-speed receive mode | 70 | - | 330 | mV |
| Z_{ID} | Differential input impedance | 80 | 100 | 120 | Ω |

Table 85: High-Speed MIPI D-PHY Receiver (RX) AC Specifications

| Parameter | Description | Min | Typ | Max | Unit |
|-----------------------|--|-----|-----|-----|------|
| $\Delta V_{CMRX(HF)}$ | Common-point interference above 450 MHz | - | - | 50 | mV |
| $\Delta V_{CMRX(LF)}$ | Common-point interference between 50 MHz to 450 MHz | - | - | 25 | mV |
| V_{IDTH} | Differential input high threshold | - | - | 40 | mV |
| V_{IDTL} | Differential input low threshold | -40 | - | - | mV |
| V_{IHHS} | Single-ended input high voltage | - | - | 460 | mV |
| V_{ILHS} | Single-ended input low voltage | -40 | - | - | mV |
| $V_{TERM-EN}$ | Single-ended threshold for high-speed termination enable | - | - | 450 | mV |
| CCP | Common-point termination | - | - | 60 | pF |

Table 86: Low-Power MIPI D-PHY Receiver (RX) DC Specifications

| Parameter | Description | Min | Typ | Max | Unit |
|---------------|---|-----|-----|-----|------|
| V_{IH} | Logic 1 input voltage | 740 | - | - | mV |
| V_{IL} | Logic 0 input voltage, not in ULP state | - | - | 550 | mV |
| $V_{IL-ULPS}$ | Logic 0 input voltage, ULP state | - | - | 300 | mV |
| V_{HYST} | Input hysteresis | 25 | - | - | mV |

Table 87: Low-Power MIPI D-PHY Receiver (RX) AC Specifications

| Parameter | Description | Min | Typ | Max | Unit |
|---------------------|------------------------------|-----|-----|-----|------|
| $T_{\text{MIN-RX}}$ | Minimum pulse width response | 20 | – | – | ns |
| V_{INT} | Peak interference amplitude | – | – | 200 | mV |
| f_{INT} | Interference frequency | 450 | – | – | MHz |

MIPI Power-Up Timing

Apply power to VCC12A_MIPIx_TX, VCC12A_MIPIx_RX, , and VCC25A_MIPIx at least $t_{\text{MIPI_POWER}}$ after VCC is stable. See **Power Up Sequence** on page 47 for a power-up sequence diagram.

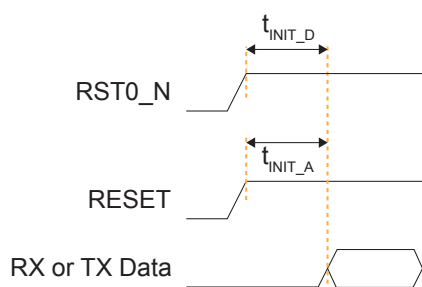
Table 88: MIPI Timing

| Symbol | Parameter | Min | Typ | Max | Units |
|--------------------------|---|-----|-----|-----|---------------|
| $t_{\text{MIPI_POWER}}$ | Minimum time after VCC is stable before powering MIPI power supplies. | 1 | – | – | μs |

MIPI Reset Timing

The MIPI RX and TX interfaces have two reset signals (RESET and RST0_N) to reset the D-PHY controller logic. These signals are active low, and you should use them together to reset the MIPI interface.

The following waveform illustrates the minimum time required to reset the MIPI interface.

Figure 32: RESET and RST0_N Timing Diagram**Table 89: MIPI Timing**

| Symbol | Parameter | Min | Typ | Max | Units |
|----------------------|---|-----|-----|-----|---------------|
| $t_{\text{INIT_A}}$ | Minimum time between the rising edge of RESET and the start of MIPI RX or TX data. | 350 | – | – | μs |
| $t_{\text{INIT_D}}$ | Minimum time between the rising edge of RST0_N and the start of MIPI RX or TX data. | 1 | – | – | clk |

PLL Timing and AC Characteristics

The following tables describe the PLL timing and AC characteristics.

Table 90: PLL Timing (C3, C4, and I4)

| Symbol | Parameter | Min | Typ | Max | Units |
|-----------------|--|------|-----|-------|-------|
| $F_{IN}^{(16)}$ | Input clock frequency from core. | 10 | – | 330 | MHz |
| | Input clock frequency from GPIO. | 10 | – | 200 | MHz |
| | Input clock frequency from LVDS. | 10 | – | 400 | MHz |
| F_{OUT} | Output clock frequency. | 0.24 | – | 500 | MHz |
| F_{OUT} | Output clock frequency for PLL BR0 CLKOUT0 (DDR PHY input clock). | 0.24 | – | 533 | MHz |
| F_{VCO} | PLL VCO frequency for internal feedback mode. | 500 | – | 1,600 | MHz |
| | PLL VCO frequency for local and core feedback mode | 500 | – | 3,600 | MHz |
| F_{PLL} | Post-divider PLL VCO frequency if all output divider values ≤ 64 | 62.5 | – | 1,800 | MHz |
| | Post-divider PLL VCO frequency if any of the output divider value > 64 | 62.5 | – | 1,400 | MHz |
| F_{PFD} | Phase frequency detector input frequency. | 10 | – | 100 | MHz |

Table 91: PLL Timing (C4L and I4L)

| Symbol | Parameter | Min | Typ | Max | Units |
|-----------------|--|------|-----|-------|-------|
| $F_{IN}^{(16)}$ | Input clock frequency from core. | 10 | – | 330 | MHz |
| | Input clock frequency from GPIO. | 10 | – | 200 | MHz |
| | Input clock frequency from LVDS. | 10 | – | 400 | MHz |
| F_{OUT} | Output clock frequency. | 0.24 | – | 500 | MHz |
| F_{OUT} | Output clock frequency for PLL BR0 CLKOUT0 (DDR PHY input clock). | 0.24 | – | 533 | MHz |
| F_{VCO} | PLL VCO frequency for internal feedback mode. | 500 | – | 1,600 | MHz |
| | PLL VCO frequency for local and core feedback mode | 500 | – | 3,200 | MHz |
| F_{PLL} | Post-divider PLL VCO frequency if all output divider values ≤ 64 | 62.5 | – | 1,600 | MHz |
| | Post-divider PLL VCO frequency if any of the output divider value > 64 | 62.5 | – | 1,200 | MHz |
| F_{PFD} | Phase frequency detector input frequency. | 10 | – | 100 | MHz |

⁽¹⁶⁾ When using the Dynamic clock source mode, the maximum input clock frequency is limited by the slowest clock frequency of the assigned clock source. For example, the maximum input clock frequency of a Dynamic clock source mode from core and GPIO is 200 MHz.

Table 92: PLL AC Characteristics⁽¹⁷⁾

| Symbol | Parameter | Min | Typ | Max | Units |
|--------------------------------------|--|------|-----|-----|-------|
| t _{DT} | Output clock duty cycle. | 40 | 50 | 60 | % |
| t _{OPJIT} (PK - PK) (18) | Output clock period jitter (PK-PK). | - | - | 200 | ps |
| t _{PLL_HLW} | PLL input clock from GPIO, HIGH/LOW pulse width. | 2.25 | - | - | ns |
| | PLL input clock from LVDS, HIGH/LOW pulse width. | 1.13 | - | - | ns |
| t _{ILJIT} (PK - PK) | Input clock long-term jitter (PK-PK) | - | - | 800 | ps |
| t _{LOCK} | PLL lock-in time. | - | - | 0.5 | ms |

⁽¹⁷⁾ Test conditions at 3.3 V and room temperature.⁽¹⁸⁾ The output jitter specification applies to the PLL jitter when an input jitter of 20 ps is applied.

Configuration Timing

The T35 FPGA has the following configuration timing specifications. Refer to [AN 006: Configuring Trion FPGAs](#) for detailed configuration information.

Timing Waveforms

Figure 33: SPI Active Mode (x1) Timing Sequence

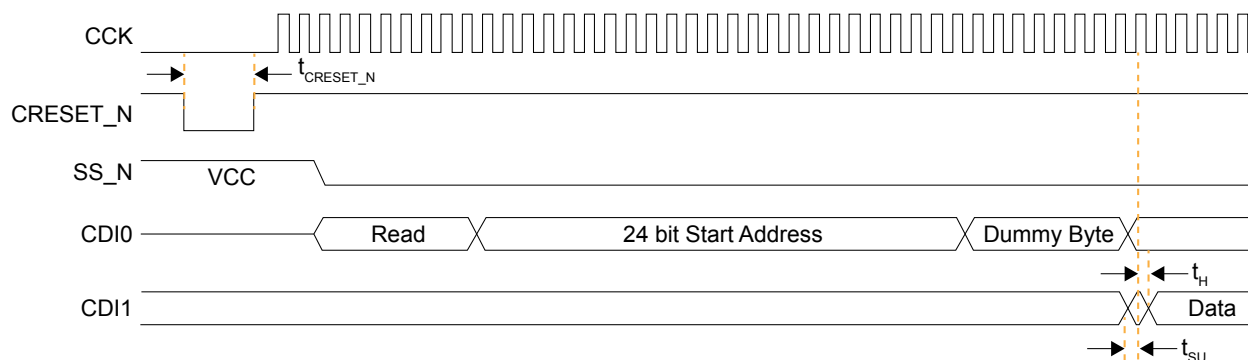


Figure 34: SPI Passive Mode Timing Sequence

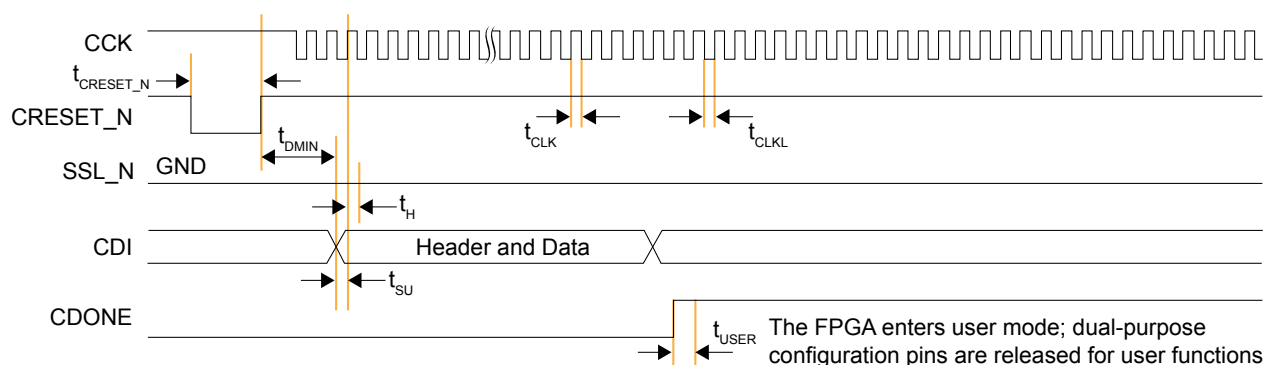
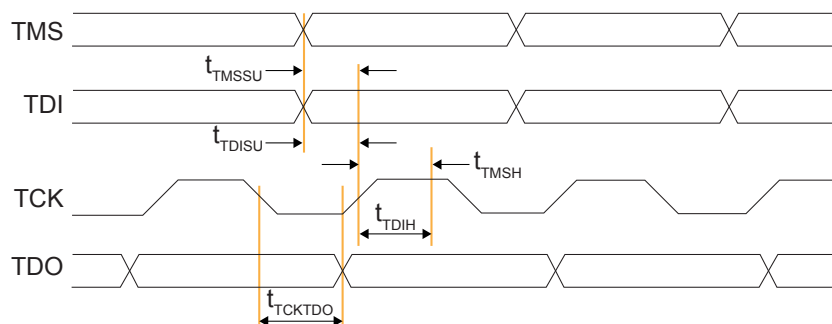


Figure 35: Boundary-Scan Timing Waveform



Timing Parameters

Table 93: All Modes

| Symbol | Parameter | Min | Typ | Max | Units |
|-----------------------|--|-----|-----|------|---------|
| t _{CRESET_N} | Minimum creset_n low pulse width required to trigger re-configuration. | 320 | – | – | ns |
| t _{USER} | Minimum configuration duration after CDONE goes high before entering user mode. ⁽¹⁹⁾⁽²⁰⁾ Test condition at 10 k Ω pull-up resistance and 10 pF output loading on CDONE pin. | 25 | – | (21) | μ s |

Table 94: Active Mode

| Symbol | Parameter | Frequency | Min | Typ | Max | Units |
|--------------------|---|-----------|-----|-----|-----|-------|
| f _{MAX_M} | Active mode configuration clock frequency. ⁽²²⁾ | DIV4 | 14 | 20 | 26 | MHz |
| | | DIV8 | 7 | 10 | 13 | MHz |
| t _{SU} | Setup time. Test condition at 3.3 V I/O standard and 0 pF output loading. | – | 7.5 | – | – | ns |
| t _H | Hold time. Test condition at 3.3 V I/O standard and 0 pF output loading. | – | 1 | – | – | ns |

Table 95: Passive Mode

| Symbol | Parameter | Min | Typ | Max | Units |
|--------------------|---|------------------------------|-----|-----|---------|
| f _{MAX_S} | Passive mode X1 configuration clock frequency. | – | – | 25 | MHz |
| | Passive mode X2, X4 or X8 configuration clock frequency. | – | – | 50 | MHz |
| | Passive mode X16 or X32 configuration clock frequency. | – | – | 100 | MHz |
| t _{CLKH} | Configuration clock pulse width high. | $0.48 \times 1 / f_{MAX_S}$ | – | – | ns |
| t _{CLKL} | Configuration clock pulse width low. | $0.48 \times 1 / f_{MAX_S}$ | – | – | ns |
| t _{SU} | Setup time. | 6.5 | – | – | ns |
| t _H | Hold time. | 1 | – | – | ns |
| t _{DMIN} | Minimum time between deassertion of CRESET_N to first valid configuration data. | 1.2 | – | – | μ s |

⁽¹⁹⁾ The FPGA may go into user mode before t_{USER} has elapsed. However, Efinix recommends that you keep the system interface to the FPGA in reset until t_{USER} has elapsed.

⁽²⁰⁾ For JTAG programming, the min t_{USER} configuration time is required after CDONE goes high and FPGA receives the ENTERUSER instruction from JTAG host (TAP controller in UPDATE_IR state).

⁽²¹⁾ See **Maximum t_{USER} for SPI Active and Passive Modes** on page 65

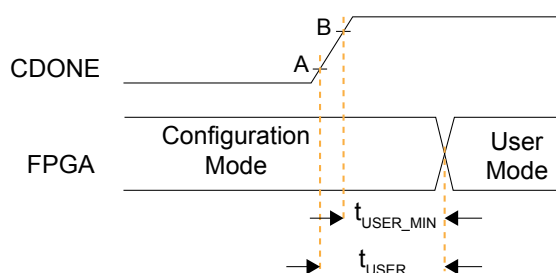
⁽²²⁾ For parallel daisy chain x2 and x4, the active configuration clock frequency, f_{MAX_M}, must be set to DIV4.

Table 96: JTAG Mode

| Symbol | Parameter | Min | Typ | Max | Units |
|-------------|---------------------------------|-----|-----|------|-------|
| f_{TCK} | TCK frequency. | - | - | 25 | MHz |
| t_{DISU} | TDI setup time. | 3.5 | - | - | ns |
| t_{DIH} | TDI hold time. | 2.5 | - | - | ns |
| t_{MSSU} | TMS setup time. | 3 | - | - | ns |
| t_{MSH} | TMS hold time. | 2.5 | - | - | ns |
| t_{CKTDO} | TCK falling edge to TDO output. | - | - | 10.5 | ns |

Maximum t_{USER} for SPI Active and Passive Modes

The following waveform illustrates the minimum and maximum values for t_{USER} .



- Point A—User-defined trigger point to start counter on t_{USER}
- Point B— V_{IH} (with Schmitt Trigger) of Trion I/Os

The maximum t_{USER} value can be derived based on the following formula:

Table 97: t_{USER} Maximum

| Configuration Setup | t_{USER} Maximum |
|--|--|
| Single Trion FPGA | $t_{USER} = t_{\text{(from A to B)}} + t_{USER_MIN}$ |
| Slave FPGA in a dual-Trion FPGA SPI chain | |
| Master FPGA in a dual-Trion FPGA SPI chain | $t_{USER} = (1344 / SPI_WIDTH) * CCK \text{ period} + t_{USER_MIN} + t_{\text{(from A to B)}}$ |

Pinout Description

The following tables describe the pinouts for power, ground, configuration, and interfaces.

Table 98: General Pinouts

| Function | Group | Direction | Description |
|--|------------------------|-----------|--|
| VCC | Power | - | Core power supply. |
| VCCA _{xx} | Power | - | PLL analog power supply. <i>xx</i> indicates the location. |
| VCCIO _{xx} | Power | - | I/O pin power supply. <i>xx</i> indicates the bank location. |
| VCCIO _{xx_yy_zz} | Power | - | Power for I/O banks that are shorted together. <i>xx</i> , <i>yy</i> , and <i>zz</i> are the bank locations. For example: VCCIO1B_1C shorts banks 1B and 1C VCCIO3C_TR_BR shorts banks 3C, TR, and BR |
| GND | Ground | - | Ground. |
| CLK _{<i>n</i>} | Alternate | Input | Global clock network input. <i>n</i> is the number. The number of inputs is package dependent. |
| CTRL _{<i>n</i>} | Alternate | Input | Global network input used for high fanout and global reset. <i>n</i> is the number. The number of inputs is package dependent. |
| PLLIN | Alternate | Input | PLL reference clock resource. There are 7 PLL reference clock resource assignments. Assign the reference clock resource based on the PLL you are using. |
| MREFCLK | Alternate | Input | MIPI TX PLL reference clock source. |
| GPIO _{<i>x_n</i>} | GPIO | I/O | General-purpose I/O for user function. User I/O pins are single-ended. <i>x</i> : Indicates the bank (L or R) <i>n</i> : Indicates the GPIO number. |
| GPIO _{<i>x_n_yyy</i>} GPIO _{<i>x_n_yyy_zzz</i>} GPIO _{<i>zzzn</i>} | GPIO Multi-Function | I/O | Multi-function, general-purpose I/O. These pins are single ended. If these pins are not used for their alternate function, you can use them as user I/O pins. <i>n</i> : Indicates the GPIO number. <i>yyy</i> , <i>yyy_zzz</i> : Indicates the alternate function. <i>zzzn</i> : Indicates LVDS TX or RX and number. |
| TXN _{<i>n</i>} , TXP _{<i>n</i>} | LVDS | I/O | LVDS transmitter (TX). <i>n</i> : Indicates the number. |
| RXN _{<i>n</i>} , RXP _{<i>n</i>} | LVDS | I/O | LVDS receiver (RX). <i>n</i> : Indicates the number. |
| CLKN _{<i>n</i>} , CLKP _{<i>n</i>} | LVDS | I/O | Dedicated LVDS receiver clock input. <i>n</i> : Indicates the number. |
| RXN _{<i>n</i>} _EXTFB _{<i>n</i>} RXP _{<i>n</i>} _EXTFB _{<i>n</i>} | LVDS | I/O | LVDS PLL external feedback. <i>n</i> : Indicates the number. |
| REF_RES | - | - | REF_RES is a reference resistor to generate constant current for LVDS TX. Connect a 12 kΩ resistor with a tolerance of ±1% to the REF_RES pin with respect to ground. If none of the pins in a bank are used for LVDS, leave this pin floating. |

Table 99: Dedicated Configuration Pins

These pins cannot be used as general-purpose I/O after configuration.

All the pins are in internal weak pull-up during configuration except for TCK and TDO.

| Pins | Direction | Description | External Weak Pull-Up/ Pull Down Requirement |
|----------|-----------|--|---|
| CDONE | I/O | Configuration done status pin. CDONE is an open drain output; connect it to an external pull-up resistor to VCCIO. When CDONE = 1, the configuration is complete and the FPGA enters user mode. You can hold CDONE low and release it to synchronize the FPGAs entering user mode. | Pull up |
| CRESET_N | Input | Active-low FPGA reset and re-configuration trigger. Pulse CRESET_N low for a duration of $t_{\text{reset_N}}$ before releasing CRESET_N from low to high to initiate FPGA re-configuration. This pin does not perform a system reset. | Pull up |
| TCK | Input | JTAG test clock input (TCK). The rising edge loads signals applied at the TAP input pins (TMS and TDI). The falling edge clocks out signals through the TAP TDO pin. | Pull up |
| TMS | Input | JTAG test mode select input (TMS). The I/O sequence on this input controls the test logic operation. The signal value typically changes on the falling edge of TCK. TMS has an internal weak pull-up; when it is not driven by an external source, the test logic perceives a logic 1. | Pull up |
| TDI | Input | JTAG test data input (TDI). Data applied at this serial input is fed into the instruction register or into a test data register depending on the sequence previously applied at TMS. Typically, the signal applied at TDI changes state following the falling edge of TCK while the registers shift in the value received on the rising edge. Like TMS, TDI has an internal weak pull-up; when it is not driven from an external source, the test logic perceives a logic 1. | Pull up |
| TDO | Output | JTAG test data output (TDO). This serial output from the test logic is fed from the instruction register or a test data register depending on the sequence previously applied at TMS. The shift out content is based on the issued instruction. The signal driven through TDO changes state following the falling edge of TCK. When data is not being shifted through the device, TDO is set to an inactive drive state (e.g., high-impedance). | Pull up |



Note: All dedicated configuration pins have Schmitt Trigger buffer. See [Table 67: Single-Ended I/O and Dedicated Configuration Pins Schmitt Trigger Buffer Characteristic](#) on page 53 for the Schmitt Trigger buffer specifications.

Table 100: Dual-Purpose Configuration Pins

In user mode (after configuration), you can use these dual-purpose pins as general I/O.

| Pins | Direction | Description | Use External Weak Pull-Up |
|------------|-----------|--|--------------------------------------|
| CBUS[2:0] | Input | Configuration bus width select. CBUS has an internal weak pull-up. However, Efinix recommends that you use an external pull-up accordingly. See <i>Selecting the Configuration Mode</i> in AN 006: Configuring Trion FPGAs | Pull up or pull down ⁽²³⁾ |
| CBSEL[1:0] | Input | Optional multi-image selection input (if external multi-image configuration mode is enabled). | Pull up or pull down ⁽²⁴⁾ |
| CCK | I/O | Passive SPI input configuration clock or active SPI output configuration clock (active low). Includes an internal weak pull-up. | Optional ⁽²⁵⁾ |
| CDIn | I/O | n is a number from 0 to 31 depending on the SPI configuration. 0: Passive serial data input or active serial output. 1: Passive serial data output or active serial input. n : Parallel I/O. In multi-bit daisy chain connection, the CDIn (31:0) connects to the data bus in parallel. | Optional ⁽²⁵⁾ |
| CSI | Input | Chip select. 0: The FPGA is not selected or enabled and will not be configured. 1: Selects the FPGA for all configuration modes. | Pull up |
| CSO | Output | Chip select output. Selects the next device for cascading configuration. | N/A |
| NSTATUS | Output | Status (active low). Indicates a configuration error. When the FPGA drives this pin low, it indicates an ID mismatch, the bitstream CRC check has failed, or remote update has failed. | N/A |
| SS_N | Input | SPI slave select (active low). Includes an internal weak pull-up resistor to VCCIO during configuration. During configuration, the logic level samples on this pin determine the configuration mode. This pin is an input when sampled at the start of configuration (SS is low); an output in active SPI flash configuration mode. The FPGA senses the value of SS_N when it comes out of reset (pulse CRESET_N low to high). 0: Passive mode 1: Active mode | Optional ⁽²⁵⁾ |
| TEST_N | Input | Active-low test mode enable signal. Set to 1 to disable test mode. During all configuration modes, rely on the external weak pull-up or drive this pin high. | Pull up |

⁽²³⁾ Optional for x1 mode.

⁽²⁴⁾ Not applicable to single-image or remote update.

⁽²⁵⁾ Optional unless pull-up is required by external load.

Table 101: MIPI Pinouts (Dedicated)*n* Indicates the number. *L* indicates the lane

| Function | Group | Direction | Description |
|--|--------|-----------|---------------------------------------|
| VCC25A_MIPI0 VCC25A_MIPI1 | Power | - | MIPI 2.5 V analog power supply. |
| VCC12A_MIPI0_TX VCC12A_MIPI1_TX | Power | - | MIPI 1.2 V TX analog power supply. |
| VCC12A_MIPI0_RX VCC12A_MIPI1_RX | Power | - | MIPI 1.2 V RX analog power supply. |
| GNDA_MIPI | Ground | - | Ground for MIPI analog power supply. |
| MIPI _n _TXDPL MIPI _n _TXDNL | MIPI | I/O | MIPI differential transmit data lane. |
| MIPI _n _RXDPL MIPI _n _RXDNL | MIPI | I/O | MIPI differential receive data lane. |
| MREFCLK | Clock | Input | MIPI PLL reference clock source. |

Table 102: DDR Pinouts (Dedicated)*n* indicates the number.

| Function | Direction | Description |
|--------------------|-----------|--|
| VCCIO_DDR | - | DDR power supply. |
| DDR_A[n] | Output | Address signals to the memories. |
| DDR_BA[n] | Output | Bank signals to the memories. |
| DDR_CAS_N | Output | Active-low column address strobe signal to the memories. |
| DDR_CKE | Output | Active-high clock enable signals to the memories. |
| DDR_CK DDR_CK_N | Output | Differential clock output pins to the memories. |
| DDR_CS_N | Output | Active-low chip select signals to the memories. |
| DDR_DQ[n] | I/O | Data bus to/from the memories. |
| DDR_DM[n] | Output | Active-high data-mask signals to the memories. |
| DDR_DQS_N[n] | I/O | Differential data strobes to/from the memories. |
| DDR_DQS[n] | I/O | Differential data strobes to/from the memories. |
| DDR_ODT | Output | ODT signal to the memories. |
| DDR_RAS_N | Output | Active-low row address strobe signal to the memories. |
| DDR_RST_N | Output | Active-low reset signals to the memories. |
| DDR_WE_N | Output | Active-low write enable strobe signal to the memories. |
| DDR_VREF | I/O | Reference voltage. |
| DDR_ZQ | I/O | ZQ calibration pin. |

Efinity Software Support

The Efinity[®] software provides a complete tool flow from RTL design to bitstream generation, including synthesis, place-and-route, and timing analysis. The software has a graphical user interface (GUI) that provides a visual way to set up projects, run the tool flow, and view results. The software also has a command-line flow and Tcl command console. The Efinity[®] software supports simulation flows using the ModelSim, NCSim, or free iVerilog simulators. An integrated hardware Debugger with Logic Analyzer and Virtual I/O debug cores helps you probe signals in your design. The software-generated bitstream file configures the T35 FPGA. The software supports the Verilog HDL and VHDL languages.

T35 Interface Floorplan



Note: The numbers in the floorplan figures indicate the GPIO and LVDS number ranges. Some packages may not have all GPIO or LVDS pins in the range bonded out. Refer to the **T35 pinout** for information on which pins are available in each package.

Figure 36: Floorplan Diagram for BGA256 Packages

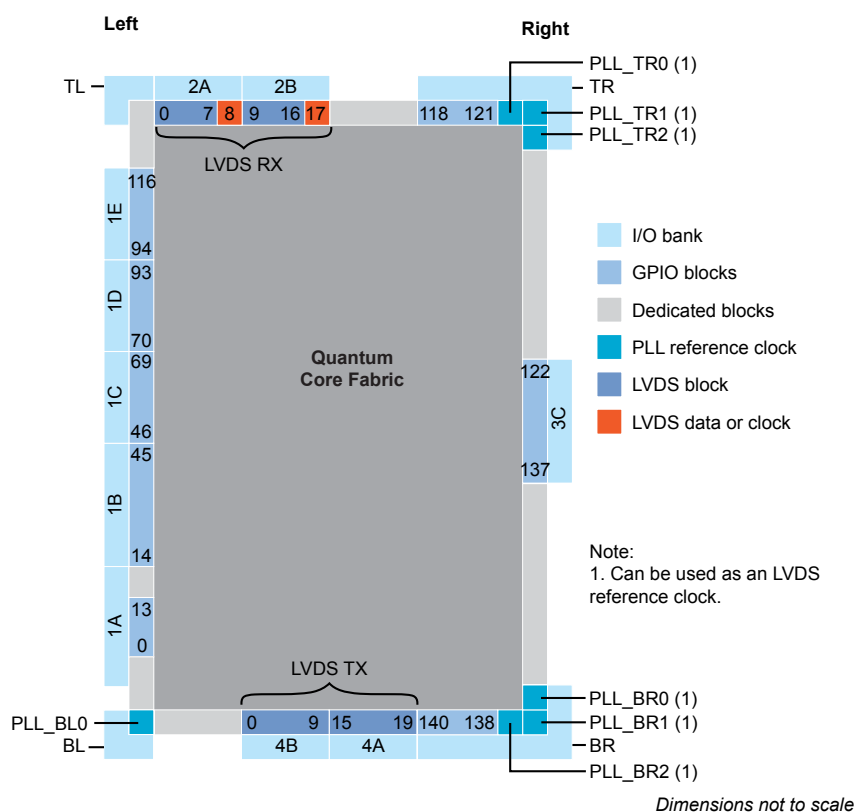


Figure 37: Floorplan Diagram for BGA324 Packages (with DDR and MIPI)

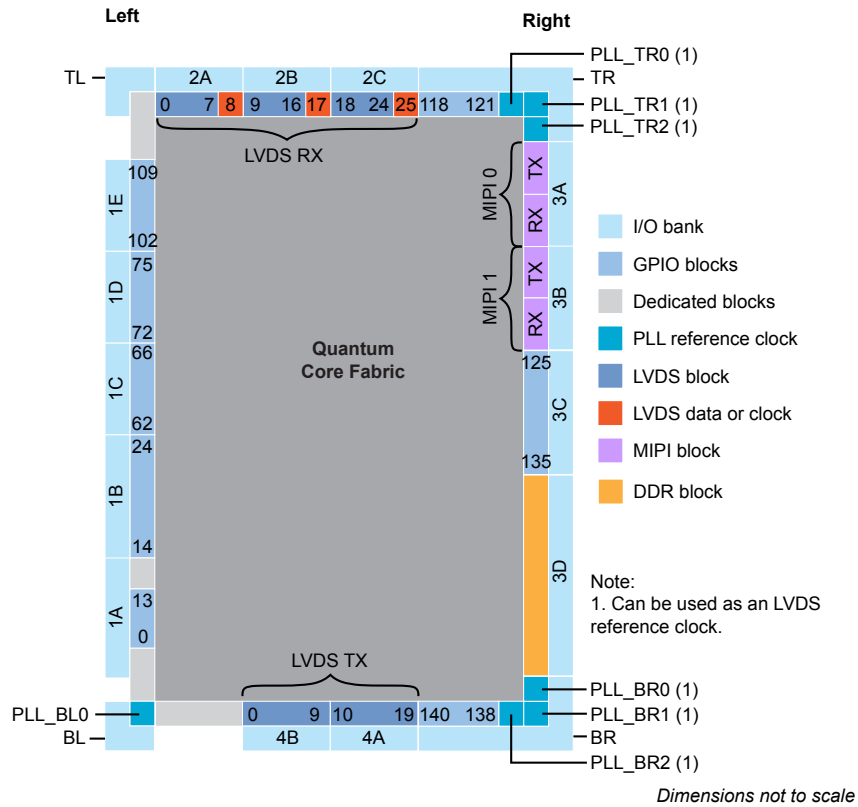
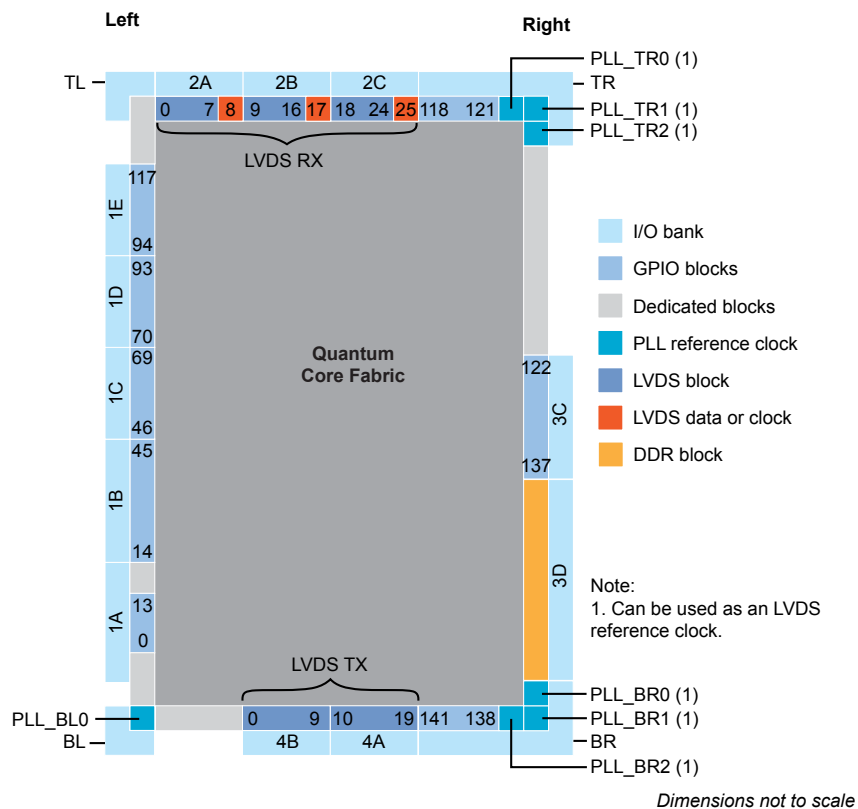


Figure 38: Floorplan Diagram for BGA400 Packages (with DDR)



Ordering Codes

Refer to the [Trion Selector Guide](#) for the full listing of T35 ordering codes.

Revision History

Table 103: Revision History

| Date | Version | Description |
|----------------|---------|--|
| March 2024 | 3.2 | Added BGA256 package information. Corrected merged banks for BGA324 package (see I/O Banks on page 16). |
| February 2024 | 3.1 | Updated SPI passive timing waveform. Added note about external DC-biased circuit is required if the incoming LVDS signals are AC-coupled and link to Trion Hardware Design Checklist and Guidelines. (DOC-1532) MIPI D-PHY specification is v1.1. (DOC-1610) |
| October 2023 | 3.0 | Added LVDS RX Static Mode Delay Setting. (DOC-1473) Updated Maximum Toggle Rate table by adding recommendation to run simulation for actual toggle rate. (DOC-1468) Updated 2.5 V and 1.8 LVCMOS Single-Ended I/O Internal Weak Pull-Up and Pull-Down Resistance. (DOC-1476) |
| June 2023 | 2.9 | Removed t_{LVDS_DT} and t_{INDT} specs, and replaced with t_{PLL_HLW} and t_{LVDS_CPA} . (DOC-1189) Updated PLL LOCKED signal description. (DOC-1208) |
| April 2023 | 2.8 | Corrected t_{LVDS_SU} and t_{LVDS_HD} specs (DOC-1070) Updated PLL RSTN signal description about de-asserting only when CLKIN is stable. (DOC-1226) |
| February 2023 | 2.7 | Updated t_{LVDS_skew} specs. (DOC-1111) Updated t_{LVDS_SU} specs (DOC-1070) Updated power up sequence diagram. (DOC-954) Added note to use LVDS blocks from the same side to minimize skew. (DOC-1150) Updated Advanced PLL Settings table descriptions. (DOC-945) |
| November 2022 | 2.6 | Added note recommending up to only 2 cascading PLLs. (DOC-931) Corrected I_{OH} and I_{OL} in buffer drive strength characteristic specifications. (DOC-933) Updated F_{VCO} , F_{PLL} , and F_{PFD} PLL Timing parameter specifications and PLL Interface Designer Settings - Manual Configuration Tab notes. (DOC-1019) Added t_{LVDS_SU} , t_{LVDS_HD} specs and LVDS RX timing waveforms. |
| September 2022 | 2.5 | Removed PLL_EXTFB from alternative input. (DOC-849) Updated output clock frequency for BR0 CLKOUT0 specs. (DOC-271) Updated Advanced PLL LOCKED signal description. (DOC-763) |

| Date | Version | Description |
|----------------|---------|---|
| April 2022 | 2.4 | <p>Added note about not using LVDS RX as a reference clock resource to drive the PLL BR0. (DOC-768)</p> <p>Updated test condition load to maximum load in Maximum Toggle Rate Table. (DOC-781)</p> <p>Updated Connection Requirements for Unused Resources table by specifying VCC value. (DOC-770)</p> <p>Updated note about leaving at least 2 pairs of unassigned LVDS pins between any GPIO and LVDS in the same device side. (DOC-769)</p> |
| March 2022 | 2.3 | <p>Updated behaviour description for GPIO and LVDS as GPIO pins during configuration, and unused GPIO pins during user mode. (DOC-720)</p> <p>Added note about the block RAM content is random and undefined if it is not initialized. (DOC-729)</p> <p>Updated DDR description in features list. (DOC-733)</p> <p>Updated power supply ramp rate and power up sequence diagram. (DOC-631)</p> |
| January 2022 | 2.2 | Corrected power supply ramp rate. (DOC-699) |
| January 2022 | 2.1 | <p>Added Output Differential Voltage with Reduce VOD Swing option enabled specs. (DOC-648)</p> <p>Added maximum I/O pin input current, I_{IN}, and maximum per bank specs. (DOC-652)</p> <p>Added PLL input clock duty cycle, t_{INDT}, specs. (DOC-661)</p> <p>Updated CDONE pin direction as bidirectional. (DOC-672)</p> |
| November 2021 | 2.0 | <p>Added storage temperature, T_{STG} spec. (DOC-560)</p> <p>Updated maximum JTAG mode TCK frequency, f_{TCK}. (DOC-574)</p> <p>Updated CSI pin description. (DOC-546)</p> <p>Updated LVDS Pins Configured as Single-Ended I/O Buffer Drive Strength specifications. (DOC-578)</p> <p>Update LVDS standard compliance which is TIA/EIA-644. (DOC-592)</p> <p>Updated t_{CLKH} and t_{CLKL}, and corrected SPI Passive Mode (x1) Timing Sequence waveform. (DOC-590)</p> <p>Updated REF_RES_xx description. (DOC-602, DOC-605)</p> <p>Updated Maximum Toggle Rate table. (DOC-630)</p> <p>Updated minimum Power Supply Ramp Rates. (DOC-631)</p> |
| September 2021 | 1.9 | <p>Added Single-Ended I/O and LVDS Pins Configured as Single-Ended I/O Rise and Fall Time specs. (DOC-522)</p> <p>Added note to Active mode configuration clock frequency stating that for parallel daisy chain x2 and x4 configuration, f_{MAX_M}, must be set to DIV4. (DOC-528)</p> <p>Added Global Clock Location topic. (DOC-532)</p> <p>Added Maximum t_{USER} for SPI Active and Passive Modes topic. (DOC-535)</p> |
| August 2021 | 1.8 | <p>Added internal weak pull-up and pull-down resistor specs. (DOC-485)</p> <p>Updated table title for Single-Ended I/O Schmitt Trigger Buffer Characteristic. (DOC-507)</p> <p>Added note in Pinout Description stating all dedicated configuration pins have Schmitt Trigger buffer. (DOC-507)</p> |
| June 2021 | 1.7 | Updated CRESET_N pin description. (DOC-450) |
| April 2021 | 1.6 | <p>Updated PLL specs; t_{LJIT} (PK - PK) and t_{DT}. (DOC-403)</p> <p>Added note about limiting number of LVDS as GPIO output and bidirectional per I/O bank to avoid switching noise. (DOC-411)</p> |

| Date | Version | Description |
|----------------|---------|---|
| March 2021 | 1.5 | Added LVDS TX reference clock output duty cycle and lane-to-lane skew specs. (DOC-416) |
| February 2021 | 1.4 | Corrected LVDS TX Settings in Efinity® Interface Designer Output Load default value. (DOC-375) Updated Density parameter description and added 256Mb to choice to LPDDR2 in DDR Interface Designer Settings. (DOC-377) Added I/O input voltage, V_{IN} specification. (DOC-389) Added LVDS TX data and timing relationship waveform. (DOC-359) Added LVDS RX I/O electrical specification waveform. (DOC-346) |
| December 2020 | 1.3 | Updated the notes for Output Load parameter in LVDS TX Settings in Efinity Interface Designer. (DOC-309) Added data for C4L and I4L DC speed grades. (DOC-268) Added a table to Power Up Sequence topic describing pin connection when PLL, GPIO, MIPI, or DDR is not used. (DOC-325) Updated NSTATUS pin description. (DOC-335) Updated PLL reference clock input note by asking reader to refer to PLL Timing and AC Characteristics. (DOC-336) Added other PLL input clock frequency sources in PLL Timing and AC Characteristics. (DOC-336) Removed OE and RST from LVDS block as they are not supported in software. (DOC-328) For the DDR reference clock, the software issues a warning (instead of error) if you do not connect the reference clock to an I/O pad. (DOC-264) |
| September 2020 | 1.2 | Updated pinout links. Corrected speed grades for single-ended I/O and LVDS configured as single-ended I/O f_{MAX} . |
| August 2020 | 1.1 | Update MIPI TX and RX Interface Block Diagram to include signal names. Updated REF_CLK description for clarity. Updated t_{USER} timing parameter values and added a note about the conditions for the values. Correct the VDDIO_DDR to VCCIO_DDR. Updated description for GPIO pins state during configuration to exclude LVDS as GPIO. Added f_{MAX} for single-ended I/O and LVDS configured as single-ended I/O. Added maximum power supply current transient during power-up. Correct the VDDIO_DDR to VCCIO_DDR. |

| Date | Version | Description |
|-----------|---------|--|
| July 2020 | 1.0 | <p>Removed preliminary note from DC and switching characteristics, LVDS I/O electrical specifications, MIPI electrical specifications and timing, PLL timing and AC characteristics, and configuration timing. These specifications are final.</p> <p>Added VDDIO_DDR absolute maximum ratings.</p> <p>Added VDDIO_DDR for DDR3, DDR3L, LPDDR3, and LPDDR2 recommended operating conditions.</p> <p>Updated timing parameter symbols in boundary scan timing waveform to reflect JTAG mode parameter symbols.</p> <p>Added supported GPIO features.</p> <p>Updated the maximum F_{VCO} for PLL to 1,600 MHz.</p> <p>Updated the C divider requirement for the 90 degrees phase shift in the PLL Interface Designer Settings - Manual Configuration Tab.</p> <p>Updated the DDR DRAM reset signal from RST_N to CFG_RST_N.</p> <p>Corrected DDR DRAM block diagram by adding DDR_CK signal.</p> <p>Updated minimum setup time for passive configuration mode to 6.5ns.</p> <p>Updated I/O bank names from TL_CORNER, BL_CORNER, TR_CORNER, and BR_CORNER to TL, BL, TR, and BR respectively.</p> <p>Updated LVDS electrical specifications note about RX differential I/O standard support, and duplicated the note in LVDS functional description topic.</p> <p>Added note to LVDS RX interface block diagram.</p> <p>Removed all instances of DDR3U.</p> |
| July 2020 | 1.0 | <p>Added note to recommended power-up sequence about MIPI power guideline.</p> <p>Updated the term DSP to multiplier.</p> <p>Updated power up sequence description about holding CRESET_N low.</p> <p>Updated floorplan diagram for FPGAs in BGA324 and BGA400 Packages.</p> <p>Added I/O bank information for BGA400 package.</p> <p>Updated PLLCLK pin name to PLL_CLKIN.</p> <p>Added PLL_EXTFB and MIPI_CLKIN as an alternative input in GPIO signals table for complex I/O buffer.</p> <p>Added PLL reference clock resource assignments for BGA400 package.</p> <p>Updated Memory CAS Latency (CL) choices in Advanced Options tab - Memory Mode register settings subtab.</p> <p>Updated Output Drive Strength choices for LPDDR2 in Advanced Options tab - Memory Mode register settings subtab.</p> <p>Corrected Enable Target 1 parameter notes in AXI 0 and AXI 1 tabs.</p> <p>Removed restriction on CLKOUT1 and CLKOUT2 when CLKIN is used to drive the DDR on CLKOUT0 in DDR DRAM PHY signals table.</p> <p>Added note stating that low core leakage current (6.7 mA typical) is applicable to BGA256 package only.</p> <p>Updated available GPIO, global clocks from GPIO pins, and global controls from GPIO pins for BGA400 package.</p> |

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| February 2020 | 0.3 | <p>Added JTAG timing specifications.</p> <p>In MIPI RX and TX interface description, updated maximum data pixels for RAW10 data type.</p> <p>Added MIPI reset timing information.</p> <p>Added Trion power-up sequence. MIPI power-up moved to this topic.</p> <p>VCC12A_MIPI_TX, VCC12A_MIPI_RX maximum recommended operating condition changed to 1.25 V.</p> <p>Added a note to the Supported Configuration Modes topic to clarify that T35 BGA324 FPGAs do not support multi-image configuration in SPI active x1 mode.</p> <p>Added the maximum PLL output clock speed for PLL BR0 CLKOUT0 (DDR PHY input clock).</p> <p>Corrected the read and write signal directions in the DDR block diagram.</p> <p>Corrected write strobe bus width.</p> <p>Added number of global clocks and controls that can come from GPIO pins to package resources table.</p> |
| December 2019 | 0.2 | <p>Updated DDR block description.</p> <p>Updated PLL Interface Designer settings.</p> <p>Removed MIPI data type bit settings. Refer to AN 015: Designing with the Trion MIPI Interface for the bit settings.</p> <p>Removed DIV1 and DIV2 active mode configuration frequencies; they are not supported.</p> <p>Added note to LVDS electrical specifications about RX differential I/O standard support.</p> |
| November 2019 | 0.1 | Initial release. |