Trion® DDR DRAM PCB Design User Guide

UG-PCB-DDR-v1.5
May 2023
www.efinixinc.com

Contents

Introduction

This user guide explains the recommended printed circuit board (PCB) layout design for the Trion® DDR DRAM interface signals. You should implement these best practices as well as understand your PCB layout options when designing applications that incorporate DDR DRAM modules. Good signal integrity (SI) is important because poorly transmitted signals can significantly lower the data valid margin at the receiver. Generally, you should place and route high-speed components and signals on the board first, and use the shortest trace lengths you can.

DDR Module Comparison

Table 1: DDR DRAM Module Features

Feature	DDR3/DDR3L	LPDDR2	LPDDR3
Core voltage VDD (mV)	1500, 1350	1200, 1800	1200, 1800
I/O voltage VDDQ/CA (mV)	1500, 1350	1200	1200
V_{REF} DQ (mV)	750, 675	600	600
V_{REF} CA (mV)	750, 675	600	600
Maximum frequency (DDR controller)	533 Mhz, DDR1066	533 Mhz, DDR1066	533 Mhz, DDR1066
Burst lengths	4, 8	4, 8, 16	8
Configuration	x8, x16	x16, x32	x16, x32
Address commands signals	27 Pins	14 Pins	15 Pins
CA bus data rate	Single	Double	Double
DQ bus data rate	Double	Double	Double
Output drive strength (Ω)	34.3, 40	34.3, 40, 48, 60, 80, 120	34.3, 40, 48
CA training	-	-	✓
Write leveling	✓	-	✓
Read leveling	✓	✓	✓
Pre-bank refresh	✓	✓	✓
Output driver	SSTL_15, SSTL135	SSTL_12	SSTL_12
ODT	✓	-	✓
Package option	Discrete	Discrete	Discrete

Trion® FPGAs with DDR DRAM

Table 2: DDR DRAM Widths Supported for FPGAs and Packages

FPGA	Package	DDR DRAM Support	DQ Widths
T20, T35	BGA324	1 block	x8 or x16
	BGA400	1 block	x8 or x16
T55, T85, T120	BGA324	1 block	x16
	BGA484	1 block	x16 or x32
	BGA576	1 block	x16 or x32

General Guidelines

Efinix recommends that you follow these general guidelines when laying out your board.

PCB Dielectric

The dielectric constant of PCB materials for most memory applications is 3.6 to 4.5, varying with frequency, temperature, material, and the resin-to-glass ratio.

FR-4, a commonly used dielectric material, averages 4.1 with signalling at 1 GHz. FR-4 is a copper-clad laminate that is adequate for most applications.

Power Design

- Route GND and VCC as planes.
- Route VTT as islands.

Decoupling Recommendations

- Use a high-accuracy capacitor to minimize inductance.
- Place every voltage supply decoupling close to pull-up resistors.
- Place address and control signals close to pull-up resistors.
- For the VDD and VDDQ power supplies, use > 0.1 μF decoupling capacitor to reduce noise.

Routing DDR Signals

- Minimize PCB layer propagation variance.
- Avoid T junctions for high-speed signals.
- Meet all delay matching requirements for PCB trace delays, different layer propagation velocity variances, and crosstalk.
- Surround the DRAM module's BGA pads with ground.
- To minimize the return path:
  - For the byte lanes, match all DQ and DQS traces to within ±50 mils.
  - Route data groups next to a VSS plane.
- Avoid placing high-speed DQ, DQS, address, and control signal across split planes. See **Split Planes and Reference Planes** on page 14 for details.
- Use a gradual trace angle to reduce parasitic effects (avoid 90° trace angles). See **Bending Traces** on page 12 for details.

Clock Signals

The DDR DRAM modules require different master CLK and nCLK clock inputs. All CA input signals are sampled on both the rising and falling edges of CLK. The address and control signals are only sampled on the rising edge of CLK. The CS and CKE input signals are sampled on the rising edge of CLK.

- Ensure the DDR DRAM modules have a clean differential clock input.
- Balance the output data so that each data word has the same valid time as all of the signals.
- Match the CK trace length to the CK# trace length ±20 mils. If multiple clock pairs are transmitted from the controller to components, all clock-pair traces should be equivalent within ±20 mils.
- Efinix recommends using a stripline design for high-speed signals. See **Microstrip and Stripline Skew** on page 16 for details.

Important: If you use the write leveling feature, the $CK_{(n-1)}$ trace length must be longer than the $DQS_{(n-1)}$ trace length. *n* is the number of DDR modules used. Refer to **Table 11: Skew Control Recommendations** on page 16 for more skew control recommendations.

Re-Ordering DQS, DQ, and DM Signals

When laying out your PCB, you may want to lay out the DQS, DQ, and DM bytes in a different order. The following sections describe the cases in which you can re-order these bytes for LPDDR3, LPDDR2, and DDR3.

Re-Ordering for LPDDR3 and LPDDR2

For LPDDR3 and LPDDR2, you can only re-order the signals for bytes 2 and 3.

Table 3: DQS, DQ, and DM Bytes

Byte	Signals	Re-Ordering Allowed?
0	DQS[0], DQ[7:0], DM[0]	No
1	DQS[1], DQ[15:8], DM[1]	No
2	DQS[2], DQ[23:16], DM[2]	Yes
3	DQS[3], DQ[31:24], DM[3]	Yes

When laying out your PCB, follow these guidelines:

Table 4: PCB Guidelines

Memory	Function	Guideline
LPDDR3, LPDDR2	MRR	Connect DQS[0], DQ[7:0], DM[0] to the FPGA's DQS[0], DQ[7:0], and DM[0] pins correctly.
LPDDR3, LPDDR2	CA training	Connect DQS[1], DQ[15:8], and DM[1] signals to the FPGA's DQS[1], DQ[15:8], and DM[1] pins correctly.
LPDDR3, LPDDR2	Write leveling	Connect the prime DQ to the FPGA's prime DQ.
LPDDR3	DQ calibration	Connect the prime DQ to the FPGA's prime DQ.

The following table shows examples of acceptable and unacceptable re-ordering. Examples A and B show DQ signal re-ordering in bytes 2 and 3, while Example C shows DQ re-ordering in bytes 0 and 1.

Table 5: Re-Ordering Examples

LPDDR3 DQ	Example A: Acceptable FPGA DQ	Example B: Acceptable FPGA DQ	Example C: UNACCEPTABLE FPGA DQ
0 Prime DQ	0 Prime DQ	0 Prime DQ	8 Prime DQ
1	1	1	9
2	2	2	10
3	3	3	11
4	4	4	12
5	5	5	13
6	6	6	14
7	7	7	15
8 Prime DQ	8 Prime DQ	8 Prime DQ	0 Prime DQ
9	9	9	1
10	10	10	2
11	11	11	3
12	12	12	4
13	13	13	5
14	14	14	6
15	15	15	7
16 Prime DQ	24 Prime DQ	16 Prime DQ	16 Prime DQ
17	25	19	17
18	26	18	18
19	27	20	19
20	28	17	20
21	29	23	21
22	30	22	22
23	31	21	23
24 Prime DQ	16 Prime DQ	24 Prime DQ	24 Prime DQ
25	17	31	25
26	18	30	26
27	19	29	27
28	20	28	28
29	21	27	29
30	22	26	30
31	23	25	31

Re-Ordering for DDR3

For DDR3, you can re-order the signals in the two bytes. To use write leveling, connect the DDR3's prime DQ to the FPGA's prime DQ.

The following table shows examples of acceptable and unacceptable re-ordering. All examples show DQ signals re-ordering in both bytes, but only Example C shows a DDR3 prime DQ not connecting to the FPGA's prime DQ.

Table 6: Re-Ordering Examples

DDR3 DQ	Example A: Acceptable FPGA DQ	Example B: Acceptable FPGA DQ	Example C: UNACCEPTABLE FPGA DQ
0 Prime DQ	0 Prime DQ	8 Prime DQ	7
1	2	9	6
2	4	10	5
3	6	11	0 Prime DQ
4	3	12	3
5	5	13	2
6	7	14	1
7	1	15	4
8 Prime DQ	8 Prime DQ	0 Prime DQ	8 Prime DQ
9	10	7	9
10	13	6	10
11	14	5	11
12	15	4	12
13	11	3	13
14	12	2	14
15	9	1	15

Terminating Signals

DDR Clock Termination

This section describes the recommended clock circuits to connect the RTT resistor to the DDR clock pin termination. Placing the RTT resistor close to the DRAM clock pins improves high-speed signaling and reduces the signal-to-noise (SNR) ratio.

Figure 1: Double Resistor Clock Termination

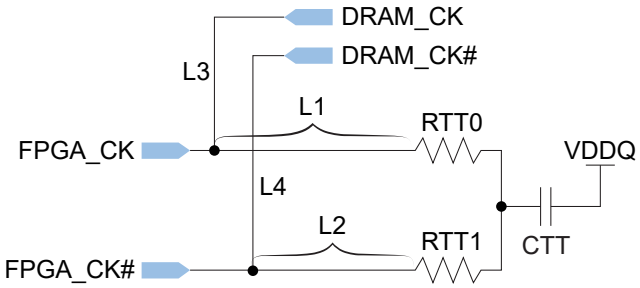


Table 7: Clock Design (CK, CK#) Requirements

PCB Design	Requirements
Differential impedance	100 Ω ± 10%
Routing spacing (other signals)	> 3 times the trace width
Trace width	> 4 mils
L1 + L3	< 7 inches (as short as possible)
L2 + L4	< 7 inches (as short as possible)
Maximum allowed vias	2
RTT0 and RTT1 resistors	50 Ω ± 5% recommended
CTT capacitor	0.1 µF recommended

Figure 2: Single Resistor Clock Termination

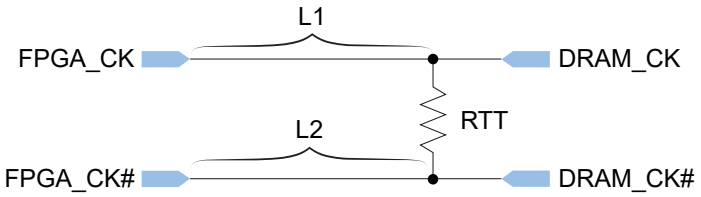


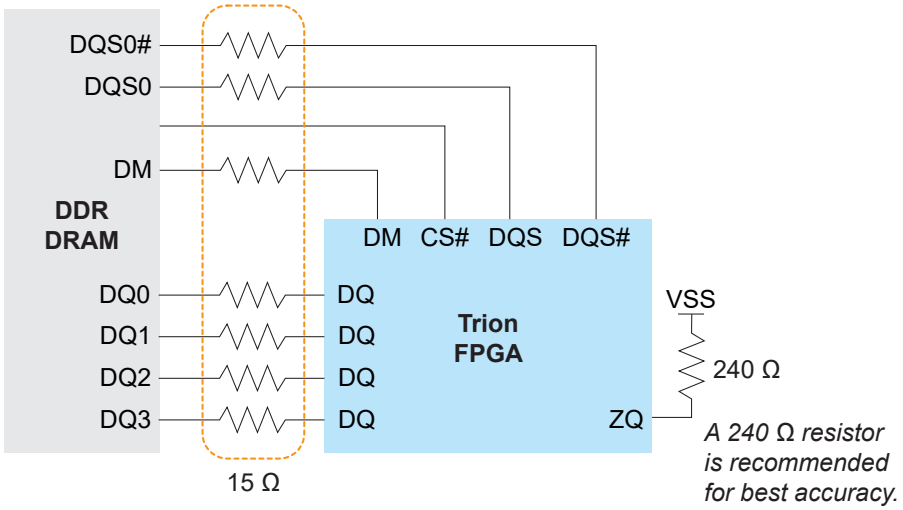
Table 8: Clock Design (CK, CK#) Requirements

PCB Design	Requirements
Differential impedance	100 Ω ± 10%
Routing spacing (other signals)	> 3 times the trace width
Trace width	> 4 mils
L1 and L2	Each < 7 inches (as short as possible)
Maximum allowed vias	2
RTT resistor	100 Ω recommended

DQ, DQS, DM Termination

This section describes the recommended circuit for the DQ, DQS, and DM signals.

Figure 3: DQ, DQS, and DM Connection between DRAM and FPGA



Note: Efinix recommends a serial termination be used if the trace length from the FPGA pad to the DRAM pad is more than (>) 5cm.

Figure 4: DQ, DQS, and DM Termination

Table 9: DQ, DQS, and DM Design Requirements

PCB Design	Requirements
Impedance (DQ, DM)	50 Ω ± 10%
Differential impedance (DQS)	100 Ω ± 10%
Routing spacing (other signals)	> 3 times the trace width
Trace width	> 4 mils
RTT0	15 Ω ± 5% (recommended)
L1 maximum length	DQ, DM: < 5 inches (as short as possible)
	DQS: < 7 inches (as short as possible)
Maximum allowed vias	4

DDR Address and Control Termination

The following terminations must be terminated on the circuit for the DDR address and control signals:

- *DDR3*—`A[15:0]`, `nCS`, `nRAS`, `nCAS`, `nWE`, `BA[2:0]`, `CKE`, and `ODT`
- *LPDDR3*—`A[9:0]`, `nCS`, `CKE`, and `ODT`

Efinix recommends the termination of LPPDDR2 `CK` and `ADDR` for better signal integrity.

- *LPDDR2*—`A[9:0]`, `nCS`, `CKE`

Figure 5: DDR Address and Control Signal Circuit

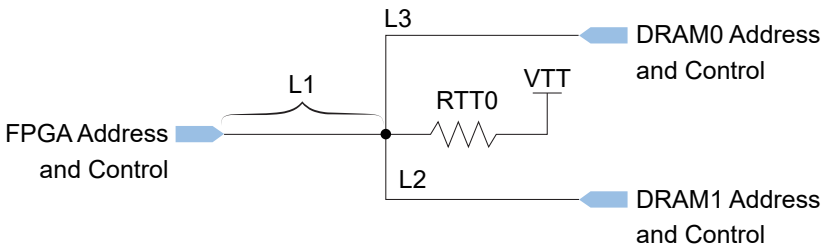


Table 10: DDR Address and Control Design Requirements

PCB Design	Requirements
Impedance	50 Ω ± 10%
Routing spacing (other signals)	> 3 times the trace width
Trace width	> 4 mils
RTT0	40 Ω ± 5% (recommended)
L1 + L3, L1 + L2 maximum length	< 7 inches (as short as possible)
Maximum allowed vias	4

Laying Out Traces

Maximum Trace Length

Efinix recommends using shorter traces, which results in better timing and makes it easy to deskew using DDR DRAM module leveling. Refer to these topics for specific requirements:

- DQ, DQS, DM Termination on page 10
- DDR Address and Control Termination on page 11
- DDR Clock Termination on page 9

Trace Spacing

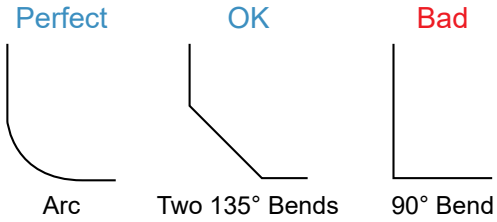
When planning your board's signal traces, maintain the correct spacing between traces. The minimum trace width for all DDR signals is 4 mils.

Figure 6: Trace Spacing Guidelines

Bending Traces

Avoid bending high-speed signal traces. When bending is required, use a bend angle greater than 135° to ensure that the bend is as loose as possible.

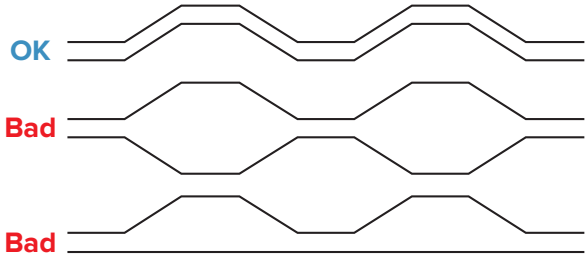
Figure 7: Examples of Trace Bends



Differential Pair Symmetry

Route all high-speed differential pairs together symmetrically and parallel to each other.

Figure 8: Pair Symmetry Examples



Match Trace Lengths

High-speed differential signals should be routed symmetrically. Always keep route signals in parallel with a constant distance between two traces. This distance is required to achieve the specified differential pair impedance. The following figures provide examples of correct and incorrect traces. The different trace colours indicate different PCB layers.

Figure 9: Route Differential Pairs Symmetrically and Always Keep Signals Parallel

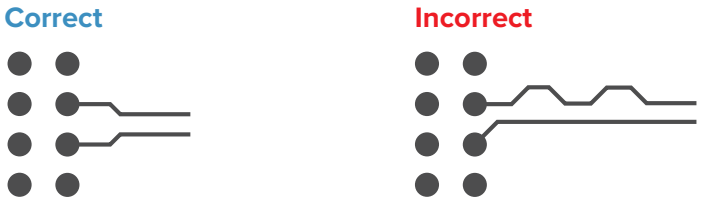


Figure 10: Do Not Place Components or Vias between Differential Pairs

Figure 11: Place Vias Symmetrically

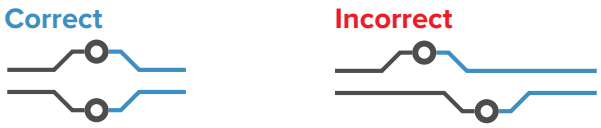
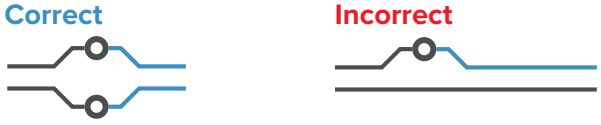
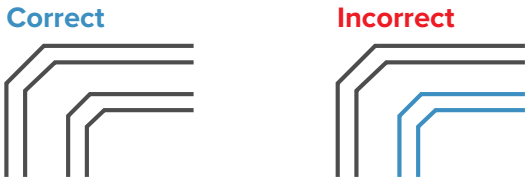


Figure 12: Route Pairs on the Same Layer with the Same Number of Vias



Signal speeds are different on different layers. For interfaces that require tight matching between signal pairs and the clock pair, route all the data and clock signals on the same layers.

Figure 13: Route Pairs from the Same Interface on the Same Layer



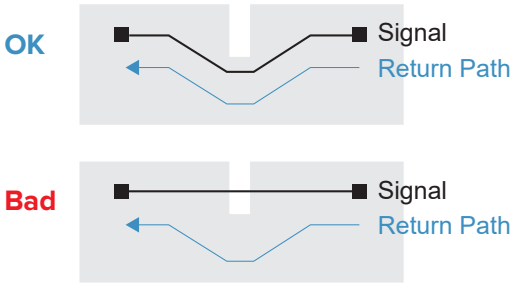
Add length correction near the mismatching point to ensure the differential pair signals are propagated synchronously over most of the connections.

Figure 14: Add Length Correction near the Mismatching Point

Split Planes and Reference Planes

High-speed signals should be routed over a ground plane. Do not route these traces across a split plane or reference plane, even when using microstrip or stripline methods. Routing across a plane split or a void in the reference plane forces the returned high-frequency current to flow around the split. The reflection increases impedance and the signal delay is increased by series inductance.

Figure 15: Split Plane Examples



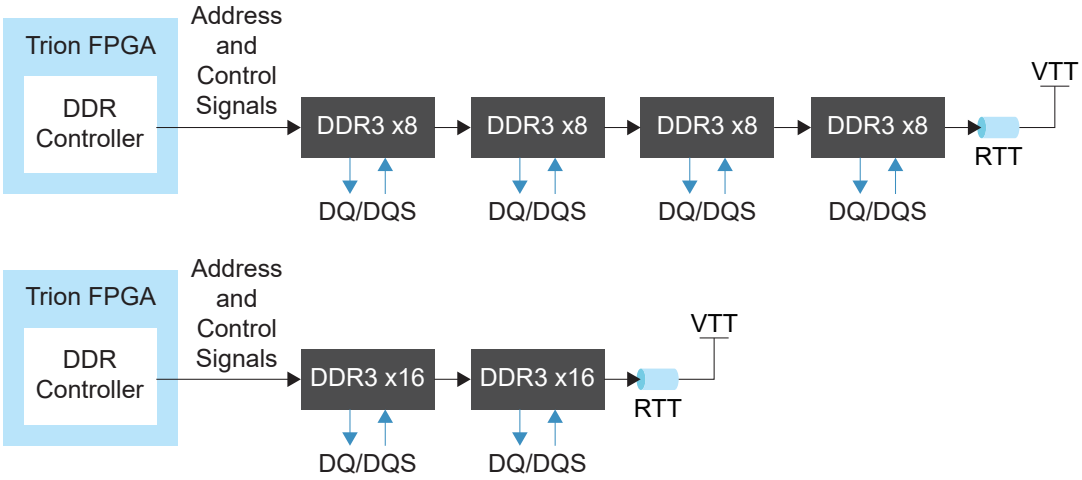
Fly-By Layout For Multiple DRAM Modules

If you plan to use two or more DDR DRAM modules on your board, Efinix recommends using a fly-by layout. This method:

- Avoids T-junctions on the PCB thereby improving the SNR.
- Reduces the trace lengths between the modules.
- The RTT provides the current and matches the impedance with the trace.

If you are only using one module, a fly-by design is not applicable.

Figure 16: Fly-By Example Layouts

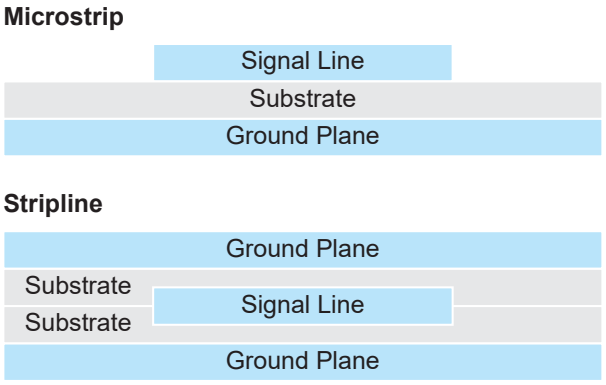


Controlling Skew

Microstrip and Stripline Skew

Two common methods to route high-speed lines are stripline, which sandwiches the signal line between ground planes, and microstrip, which lays the signal line on the board's surface. Efinix® recommends using stripline because it provides a better SNR for high-speed signals and helps to reduce skew.

Figure 17: Comparing Microstrip and Stripline Design



Skew is the timing delay difference between 2 or more signals. The following table shows skew control recommendations for double data rate and single data rate domains for various operating frequencies, as well as the recommended PCB skew for `CK` to `DQS` timing.

To help the design process, the skew (in picoseconds) is converted to an approximate physical length (in inches) for both the microstrip and stripline routing methods.

Note: The timing information provided here is for reference only. The layout, PCB, and components you use will affect the actual signal timing and skew.

Table 11: Skew Control Recommendations

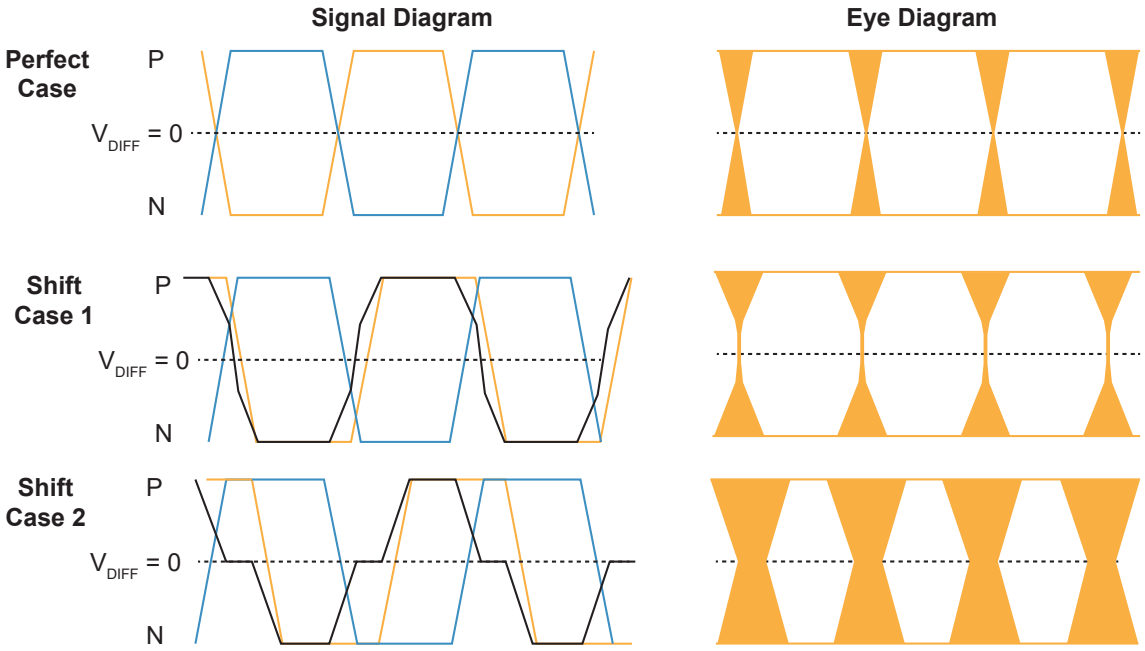
Speed (Bit Rate)		400 Mhz, DDR 800	533 Mhz, DDR 1066
DQ to DQS	Skew in ps	25	18
	Skew in inches of microstrip	0.17	0.12
	Skew in inches of stripline	0.14	0.1
Address, control, and CA to CK	Skew in ps	50	38
	Skew in inches of microstrip	0.33	0.25
	Skew in inches of stripline	0.28	0.21
DQS to CK	Skew in ps	188	141
	Skew in inches of microstrip	1.25	0.93
	Skew in inches of stripline	1.04	0.78

Differential Pair Skew

For correct DRAM operation, the timing of the DQS and CK differential pairs is critical. Efinix® strongly recommends that you match the electrical length between these legs and keep any differences to less than 5 ps.

Skew between the differential pair lines (intra-pair skew) impacts the monotonicity of the CK/CK# and DQS/DQS# signals, which are critical to the timing. Skew on these signals causes signal distortion and increases the bit error rate.

Figure 18: Effect of Intra-Pair Skew on Eye Diagram



Note: The Trion® DDR DRAM controller cannot deskew the differential signals. The zero crossing of the differential signals can seriously impact timing margins, leading to high jitter, high SNR, and increased sample errors.

Table 12: Trace Length's Effect on Signal Integrity

Property	Pin Match	Pin Mismatch
Length	< ±5% of trace length	> ±5% of trace length
Skew	< ±5ps	> ±5 ps
Delay	No skew	Skew
Jitter	Low	High
Sample error	Low	High
SNR	Low	High
Distortion	Low	High

Controlling Impedance

An ideal transmission line has a characteristic impedance along the entire trace. If the characteristic impedance of the matched transmission line is perfectly maintained, the full signal exists at the end of the trace without reflection or signal attenuation.

To control impedance, you need to control three features of the circuit's geometry:

- The trace width.
- The spacing between the signal return path and the signal trace.
- The dielectric coefficient of the material surrounding the trace.

You can calculate these values using a trace impedance calculator. Work with your PCB manufacturer during your PCB layout design for these impedance calculations.

Additionally:

- Use 50 to 60 Ω ±10% for all single-ended signals.
- Use 100 Ω ±10% for all differential signals.
- Route high-speed signals using a minimum number of vias and corners to reduce signal reflections and impedance changes.
- To route a 90° turn, use two 135° turns or an arc instead of a single 90° turn. This method reduces reflections on the signal by minimizing impedance discontinuities.

Revision History

Table 13: Document Revision History

Date	Version	Description
May 2023	1.5	Added descriptions to re-ordering example tables. (DOC-1273)
February 2023	1.4	Added in statements for DDR3, LPDDR3 and LPDDR2. (DOC-1140) Added a note regarding the trace length from FPGA pad to DRAM pad in topic DQ, DQS, DM termination. Update feature - Read levelling for LPDDR2 in topic DDR Module Comparison.
July 2022	1.3	The section on re-ordering DDR3 incorrectly mentioned LPDDR3. (DOC-852)
July 2022	1.2	Added note about write leveling trace requirement.
June 2022	1.1	Added information on which signals can be re-ordered. (DOC-799)
May 2020	1.0	Initial release.