

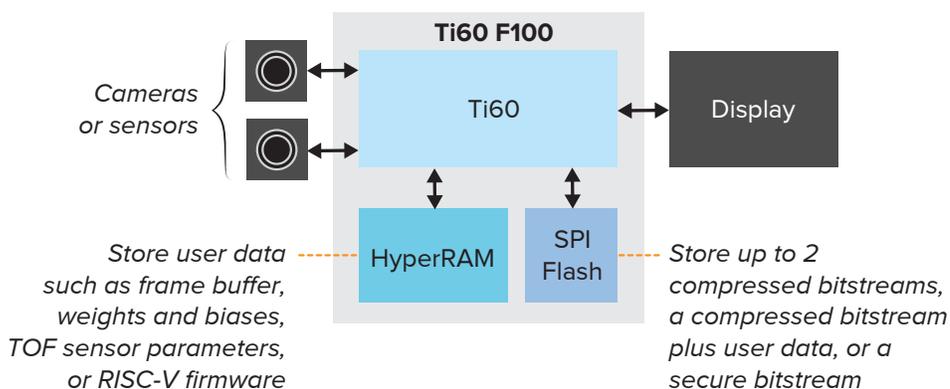
# Ti60 F100: Ready for Vision

More and more products are using cameras and sensors these days, collecting a wealth of data. How do you aggregate and process it all? The Titanium Ti60 in the F100 package is here to help. This FPGA packs 60K worth of logic, high-speed I/O that are configurable for a variety of protocols, plus integrated SPI flash and HyperRAM, all wrapped into a tiny 5.5 mm square package with a 0.5 mm ball pitch.

The combination of FPGA logic and data storage makes the Ti60 F100 a great solution for a variety of camera and sensor systems such as IoT, thermal cameras, industrial cameras, robotics, and smart devices. With the SPI flash, you can eliminate the need for a separate configuration device, while the HyperRAM memory can store user data. For example, you can use the HyperRAM as a frame buffer for video, to store weights and biases for AI, to store parameters for time-of-flight (TOF) sensors, or to hold firmware for a RISC-V SoC.



**Figure 1 Complete Camera System**



*Designed for highly integrated mobile and edge devices that need low power, a small footprint, and video and display interfaces such as IoT, thermal cameras, industrial cameras, robotics, and smart devices.*

## Configurable High-Speed I/O

The Ti60 high-speed I/O (HSIO) pins support numerous single-ended and differential I/O standards. You can use them as regular GPIO or LVDS pairs. And, you can use them as MIPI RX or TX lanes running at speeds up to 1.5 Gbps. These HSIO pins are fully user configurable, so you can mix and match them to fit your system needs.

Use the HSIO pins with the MIPI-CSI-2 protocol to gather data from cameras or sensors and then send it to an application processor. Or, use the DSI protocol to send imaging to a display. The Efinity® software includes a suite of D-PHY, CSI-2, and DSI IP to help you create MIPI-based systems more easily.

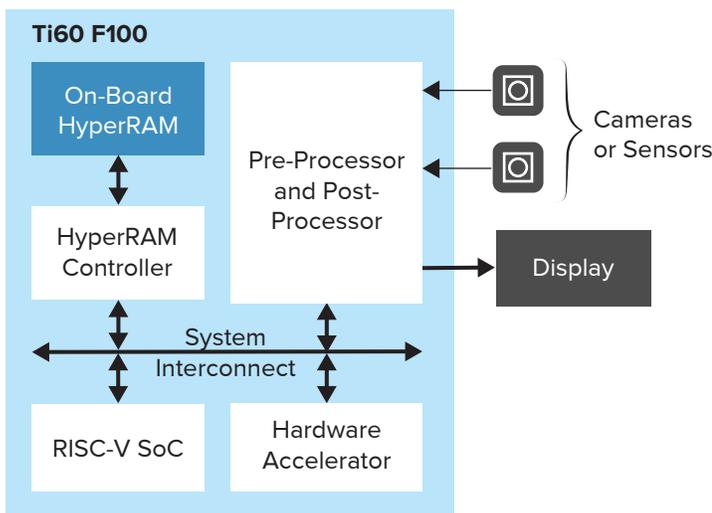
Figure 2 Flexible HSIO Pins



## HyperRAM Memory for Data Storage

The HyperRAM memory in the F100 package has a density of 256 Mbits, a clock rate of up to 200 MHz, features a HyperBus interface for high-speed communications, and supports double-data rates of up to 400 Mbps. Additionally, the HyperRAM is designed for ultra-low power consumption, so it gets the job done without using a lot of your power budget. Having the memory integrated in the package lets you store video frame data or sensor data and then process it with the FPGA logic without having to dedicate board space to another memory device.

Figure 3 Ti60 F100 RISC-V Application Example



## SPI Flash Memory for “Instant” On

FPGAs are volatile, and typically require a separate device to store a configuration (bitstream) file. The F100 package has a 16 Mbit SPI NOR flash memory so you do not have to dedicate space on your board for a configuration device. With a clock rate of up to 85 MHz, the Ti60 is awake and ready to go quickly.

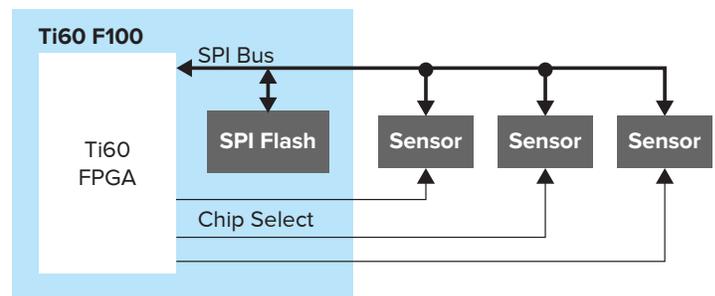
The flash can do more than just hold a bitstream though. The Efinity software supports bitstream compression for Titanium FPGAs, and the compressed Ti60 bitstream typically uses less than half of the flash. You can use the rest of the flash to store non-volatile user data, a second bitstream image, or even to store a RISC-V application binary. Additionally, if security is important, you can fit one bitstream secured using authentication, encryption, or both.

The flash’s SPI pins are bonded to the F100 package pins. This arrangement lets you use the Ti60 FPGA as a SPI master connected to one or more slaves (on-board flash and external SPI-capable devices). For example, you can use the SPI bus to gather data from SPI sensors for processing.

Figure 4 SPI Flash Uses



### SPI Bus Support



## Value-Added System Integration

The Ti60 F100 is a validated, hardware-proven system, ready for your high-volume production applications. With the integrated HyperRAM and SPI flash devices, you can reduce the time it takes to get from prototype to volume production, making your board design easier and lowering the total board and BOM costs.