# Titanium Reliability Report

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# Contents

# Introduction

The Titanium Ti60 & Ti180 FPGA features the high-density, low-power Efinix® Quantum™ compute fabric wrapped with an I/O interface in a small footprint package for easy integration.

Ti60 FPGAs are designed for highly integrated mobile and edge devices that need low power, a small footprint, and a multitude of I/Os. With ultra-low power Ti60 FPGAs, designers can build products that are always on, providing enhanced capabilities for applications such as mobile, edge, AI IoT, and sensor fusion.

Ti180 FPGAs include hardened MIPI D-PHY which can be used with Efinix® MIPI CSI-2 and DSI controller IP cores to create multi-camera, high-definition vision systems, edge computing, and hardware acceleration systems. Additionally, these FPGAs have a hardened DDR DRAM controller block that supports LPDDR4 DRAM interface. With ultra-low power Ti180 FPGAs, designers can build products that are always on, providing enhanced capabilities for applications such as vision systems, edge computing, hardware acceleration, and machine learning.

The Titanium platform consists of ten devices, built on TSMC's 16nm process, with a logic density range from 35K to 1M logic elements (LEs) and standard interfaces such as GPIO, PLLs, oscillators, MIPI, DDR, LVDS, PCI Express, etc. Titanium FPGAs target general-purpose custom logic markets (mobile, IoT, general consumer, industrial, and medical) as well as fast-growing markets such as compute acceleration and deep learning in edge devices.

This reliability report provides the reliability results for Titanium FPGAs. Efinix ensures standards compliance with this report.

# Efinix Product Qualification Program

Efinix qualifies FPGAs using various reliability conditions.

## Reliability Qualification Requirements

***Table 1: Reliability Qualification Requirements***

Refer to the data in the following sections for the sample size for each condition.

| Reliability Condition | JEDEC Standard | Test Condition |
|---|---|---|
| Electrostatic Discharge – Human Body Model (HBM) | JS-001<br>AEC-Q100-002 | Class 2 ≤2,000 V |
| Electrostatic Discharge – Charged Device Model (CDM) | JS-002<br>AEC-Q100-011 | Class C2a ≤500 V |
| Latch-Up (LU) | JESD78<br>AEC-Q100-004 | Class II, ±100 mA trigger current<br>VCC +50% on power supplies |
| Preconditioning (PC) | J-STD-020,<br>JESD22-A113 | Bake at 125 °C, 24 hours |
| | | MSL 1: 85 °C/85% RH, 168 hours<br>MSL 3: 30 °C/60% RH, 192 hours |
| | | 3 reflow cycles at 260 °C |
| High Temperature Operating Life (HTOL) | JESD22-A108 | 125 °C, 168 hours |
| | | 125 °C, 500 hours |
| | | 125 °C, 1,000 hours |
| Temperature Cycling (TC) | JESD22-A104 | -55 °C/125 °C, 500 cycles or<br>-65 °C/150 °C, 500 cycles |
| | | -55 °C/125 °C, 1,000 cycles or<br>-65 °C/150 °C, 1,000 cycles |
| High Temperature Storage Life (HTSL) | JESD22-A103 | 150 °C, 168 hours |
| | | 150 °C, 500 hours |
| | | 150 °C, 1,000 hours |
| Unbiased Highly Accelerated Stress Test (uHAST) | JESD22-A118 | 130 °C/85% RH, 96 hours |
| | | 130 °C/85% RH, 192 hours |
| Temperature Humidity Without Bias (TH) | JESD22-A101 | 85 °C/85% RH, 500 hours |
| | | 85 °C/85% RH, 1000 hours |
| Temperature Humidity Bias (THB) | JESD22-A101 | 85 °C/85% RH, $V_{cc}$ max, 500 hours |
| | | 85 °C/85% RH, $V_{cc}$ max, 1000 hours |
| Nonvolatile Memory Uncycled High Temperature Data Retention (UCHTDR) | JESD22-A117 | 150 °C, 168 hours |
| | | 150 °C, 500 hours |
| | | 150 °C, 1,000 hours |

## Extension Reliability Test and Result by Similarity

The generation and use of generic data applied across a family of packages emanating from one base assembly process is a family qualification, or Qualification-by-Similarity (QBS). The package stresses uHAST and HTSL are considered generic for a given package technology. TC is considered generic up to an evaluated die size + package size + 10% for a given package technology. Pre-Conditioning (PC) is considered generic up to an evaluated peak reflow temperature for a given package technology.

# ESD and Latch Up Qualification Data

The following sections describe the electrostatic discharge and latch-up test results.

## Electrostatic Discharge - Human Body Model (ESD-HBM)

The Titanium product family was tested per the JS-001 Electrostatic Discharge (ESD) Sensitivity Test – Human Body Model – Component Level JEDEC Standard procedure or AEC-Q100-002 Human Body Model Electrostatic Discharge Test standard.

- *Test room ambient conditions*—Room temperature, humidity <60% RH
- *Test condition*—Class 2, ≤2,000 V

*Table 2: ESD-HBM Data*

| Device | Package | Sample Size | Result |
|---|---|---|---|
| Ti60 | FBGA SIP 100 | 9 units x 1 lot | Pass |
| | FBGA 225 | 9 units x 1 lot | Pass |
| | WLCSP 64 | - | QBS |
| Ti35 | FBGA SIP 100 | - | QBS |
| | FBGA 225 | - | QBS |
| Ti180 | FCCSP 484 | 9 units x 1 lot | Pass |
| | FCCSP 361 | - | QBS |
| | HFCBGA529 | - | QBS |
| Ti120 | FCCSP 484 | - | QBS |
| | FCCSP 361 | - | QBS |
| | HFCBGA529 | - | QBS |
| Ti90 | FCCSP 484 | - | QBS |
| | FCCSP 361 | - | QBS |
| | HFCBGA529 | - | QBS |

# Electrostatic Discharge - Charged Device Model (ESD-CDM)

The Titanium product family was tested per the JS-002 Electrostatic Discharge (ESD) Sensitivity Testing – Charged Device Model (CDM) – Device Level JEDEC Standard procedure or AEC-Q100-011 Charged Device Model Electrostatic Discharge Test standard.

- *Test room ambient conditions*—Room temperature, humidity <60% RH
- *Test condition*—Class C2a, ≤500 V

*Table 3: ESD-CDM Data*

| Device | Package | Sample Size | Result |
|---|---|---|---|
| Ti60 | FBGA SIP 100 | 6 units x 1 lot | Pass |
| | FBGA 225 | 6 units x 1 lot | Pass |
| | WLCSP 64 | - | QBS |
| Ti35 | FBGA SIP 100 | - | QBS |
| | FBGA 225 | - | QBS |
| Ti180 | FCCSP 484 | 6 units x 1 lot | Pass |
| | FCCSP 361 | - | QBS |
| | HFCBGA529 | - | QBS |
| Ti120 | FCCSP 484 | - | QBS |
| | FCCSP 361 | - | QBS |
| | HFCBGA529 | - | QBS |
| Ti90 | FCCSP 484 | - | QBS |
| | FCCSP 361 | - | QBS |
| | HFCBGA529 | - | QBS |

# Latch-Up (LU)

The Titanium product family was tested per the JESD78 Latch-up JEDEC Standard procedure or AEC-Q100-004 Latch-up Test standard.

- *Test room ambient conditions*—Room temperature, humidity <60% RH
- *Test condition*—±100 mA trigger current, $V_{CC}$ +50% on power supplies, 125 °C

*Table 4: LU Data*

| Device | Package | Sample Size | Result |
|---|---|---|---|
| Ti60 | FBGA SIP 100 | 6 units x 1 lot | Pass |
| | FBGA 225 | 6 units x 1 lot | Pass |
| | WLCSP 64 | - | QBS |
| Ti35 | FBGA SIP 100 | - | QBS |
| | FBGA 225 | - | QBS |

| | | | |
|---|---|---|---|
| Ti180 | FCCSP 484 | 6 units x 1 lot | Pass |
| | FCCSP 361 | - | QBS |
| | HFCBGA529 | - | QBS |
| Ti120 | FCCSP 484 | - | QBS |
| | FCCSP 361 | - | QBS |
| | HFCBGA529 | - | QBS |
| Ti90 | FCCSP 484 | - | QBS |
| | FCCSP 361 | - | QBS |
| | HFCBGA529 | - | QBS |

# Life Data

This section describes the results of life testing.

## High-Temperature Operating Life (HTOL)

The Titanium product family was tested per the JESD22-A108 High Temperature Operating Life (HTOL) JEDEC Standard procedure.

- *Stress duration*—168, 500, and 1,000 hours
- *Stress condition*—Tj = 125 °C, maximum operating voltage

*Table 5: HTOL Data*

| Device | Package | Sample Size | Result |
|---|---|---|---|
| Ti60 | FBGA SIP 100 | – | QBS |
| | FBGA 225 | 77 units x 3 lots | Pass |
| | WLCSP 64 | – | QBS |
| Ti35 | FBGA SIP 100 | – | QBS |
| | FBGA 225 | – | QBS |
| Ti180 | FCCSP 484 | 77 units x 3 lots | Pass |
| | FCCSP 361 | - | QBS |
| | HFCBGA529 | - | QBS |
| Ti120 | FCCSP 484 | - | QBS |
| | FCCSP 361 | - | QBS |
| | HFCBGA529 | - | QBS |
| Ti90 | FCCSP 484 | - | QBS |
| | FCCSP 361 | - | QBS |
| | HFCBGA529 | - | QBS |

# Package Qualification Data

The following sections describe the results of package qualification testing.

## Preconditioning (PC)

The Titanium product family was tested per the J-STD-020 and JESD22-A113 JEDEC Standard procedure with Moisture Sensitivity Level 1 (MSL 1) or Level 3 (MSL 3). All devices stressed through temperature cycling, unbiased HAST and temperature humidity bias were preconditioned.

***Table 6: PC Data (FBGA)***

MSL 3: 24 hours bake at 125 °C, 30 °C/60% RH, 192 hours, 3 reflow cycles at 260 °C

| Device | Package | Sample Size | Result |
|---|---|---|---|
| Ti60 | FBGA SIP 100 | 77 units x 6 lots | Pass |
| | FBGA 225 | 77 units x 9 lots | Pass |
| Ti35 | FBGA SIP 100 | - | QBS |
| | FBGA 225 | - | QBS |
| Ti180 | FCCSP 484 | 77 units x 9 lots | Pass |
| | FCCSP 361 | 77 units x 6 lots | Pass |
| | HFCBGA529 | 77 units x 6 lots | Pass |
| Ti120 | FCCSP 484 | - | QBS |
| | FCCSP 361 | - | QBS |
| | HFCBGA529 | - | QBS |
| Ti90 | FCCSP 484 | - | QBS |
| | FCCSP 361 | - | QBS |
| | HFCBGA529 | - | QBS |

***Table 7: PC Data (WLCSP)***

MSL 1: 24 hours bake at 125°C, 85 °C/85% RH, 168 hours, 3 reflow cycles at 260 °C

| Device | Package | Sample Size | Result |
|---|---|---|---|
| Ti60 | WLCSP 64 | 77 units x 6 lots | Pass |

# Temperature Cycling (TC)

The Titanium product family was tested per the JESD22-A104 JEDEC Standard procedure. The stress duration was 500 and 1,000 cycles.

*Table 8: TC Data (FBGA)*

Stress condition: -55 °C, 125 °C

| Device | Package | Sample Size | Result |
|---|---|---|---|
| Ti60 | FBGA SIP 100 | 77 units x 3 lots | Pass |
| | FBGA 225 | 77 units x 3 lots | Pass |
| Ti35 | FBGA SIP 100 | - | QBS |
| | FBGA 225 | - | QBS |
| Ti180 | FCCSP 484 | 77 units x 3 lots | Pass |
| | FCCSP 361 | 77 units x 3 lots | Pass |
| | HFCBGA529 | 77 units x 3 lots | Pass |
| Ti120 | FCCSP 484 | - | QBS |
| | FCCSP 361 | - | QBS |
| | HFCBGA529 | - | QBS |
| Ti90 | FCCSP 484 | - | QBS |
| | FCCSP 361 | - | QBS |
| | HFCBGA529 | - | QBS |

*Table 9: TC Data (WLCSP)*

Stress condition: -65 °C, 150 °C

| Device | Package | Sample Size | Result |
|---|---|---|---|
| Ti60 | WLCSP 64 | 77 units x 3 lots | Pass |

# Unbiased HAST (uHAST)

The Titanium product family was tested per the JESD22-A118 JEDEC Standard procedure.

- *Stress duration*—96 and 192 hours
- *Stress condition*—130°C/85% RH

*Table 10: uHAST Data*

| Device | Package | Sample Size | Result |
|---|---|---|---|
| Ti60 | FBGA SIP 100 | 77 units x 3 lots | Pass |
| | WLCSP 64 | 77 units x 3 lots | Pass |
| Ti35 | FBGA SIP 100 | - | QBS |
| Ti180 | FCCSP 484 | 77 units x 3 lots | Pass |
| | FCCSP 361 | 77 units x 3 lots | Pass |
| | HFCBGA529 | 77 units x 3 lots | Pass |
| Ti120 | FCCSP 484 | - | QBS |
| | FCCSP 361 | - | QBS |
| | HFCBGA529 | - | QBS |
| Ti90 | FCCSP 484 | - | QBS |
| | FCCSP 361 | - | QBS |
| | HFCBGA529 | - | QBS |

# Temperature Humidity Without Bias (TH)

The Titanium product family was tested per the JESD22-A101 JEDEC Standard procedure.

- *Stress duration*—500 and 1000 hours
- *Stress condition*—85°C/85% RH

*Table 11: TH Data*

| Device | Package | Sample Size | Result |
|---|---|---|---|
| Ti60 | FBGA 225 | 77 units x 3 lots | Pass |
| Ti35 | FBGA 225 | - | QBS |

# High-Temperature Storage Life (HTSL)

The Titanium product family was tested per the JESD22-A103 JEDEC Standard procedure.

- *Stress duration*—168, 500, and 1,000 hours
- *Stress condition*—$T_a$ = 150 °C

*Table 12: HTSL Data*

| Device | Package | Sample Size | Result |
|---|---|---|---|
| Ti60 | FBGA SIP 100 | 77 units x 3 lots | Pass |
| | FBGA 225 | 77 units x 3 lots | Pass |
| | WLCSP 64 | 77 units x 3 lots | Pass |
| Ti35 | FBGA SIP 100 | - | QBS |
| | FBGA 225 | - | QBS |
| Ti180 | FCCSP 484 | 77 units x 3 lots | Pass |
| | FCCSP 361 | 77 units x 3 lots | Pass |
| | HFCBGA529 | 77 units x 3 lots | Pass |
| Ti120 | FCCSP 484 | - | QBS |
| | FCCSP 361 | - | QBS |
| | HFCBGA529 | - | QBS |
| Ti90 | FCCSP 484 | - | QBS |
| | FCCSP 361 | - | QBS |
| | HFCBGA529 | - | QBS |

# Temperature Humidity Bias (THB)

The Titanium product family was tested per the JESD22-A101 JEDEC Standard procedure.

- *Stress duration*— 500, and 1,000 hours
- *Stress condition*— 85 °C/85% RH, $V_{cc}$ max

*Table 13: THB Data*

| Device | Package | Sample Size | Result |
|---|---|---|---|
| Ti60 | FBGA 225 | 77 units x 3 lots | Pass |
| Ti35 | FBGA 225 | - | QBS |
| Ti180 | FCCSP 484 | 77 units x 3 lots | Pass |
| Ti120 | FCCSP 484 | - | QBS |
| Ti90 | FCCSP 484 | - | QBS |

# Nonvolatile Memory Data

This section describes the results of nonvolatile memories data retention testing.

## Uncycled High Temperature Data Retention (UCHTDR)

The Titanium product family was tested per the JESD22-A117 Electrically Erasable Programmable ROM (EEPROM) Program/Erase Endurance and Data Retention Stress Test JEDEC Standard procedure.

- *Stress duration*—168, 500, and 1,000 hours
- *Stress condition*—$T_a$=150°C

*Table 14: UCHTDR Data*

| Device | Package | Sample Size | Result |
|---|---|---|---|
| Ti60 | FBGA SIP 100 | 77 units x 3 lots | Pass |
| Ti35 | FBGA SIP 100 | - | QBS |

# Revision History

| Date | Version | Description |
|---|---|---|
| February 2024 | 3.0 | Add qualification data for Ti35 FBGA225, Ti90/Ti120/Ti180 FCCSP484, Ti90/Ti120/Ti180 FCCSP361 and Ti90/Ti120/Ti180 HFCBGA529 devices.<br>Add THB data for Ti60/Ti35 FBGA225 devices. |
| March 2023 | 2.0 | Add qualification data for Ti60 FBGA225 and Ti60 WLCSP64 devices.<br>Add UCHTDR data for Ti60 FBGA SIP100 device. |
| January 2022 | 1.0 | Initial release. |